WL-CSP
（Wafer Level Chip Scale Package）

Application Notes

Rev 1.00 October 2024

Table of Contents

Section 1 Preface

Section 2 Devices in this Document

Section 3 PCB and Solder Stencil Designs
3.1 Solder Resist Design
3.2 Land Pattern Design
3.3 Solder Stencil Design

Section 4 PCB Mounting Conditions
4.1 Solder Paste
4.2 Loading Process
4.2.1 ESD Control
4.2.2 Loading Control by Adsorption Collet
4.3 Reflow
4.3.1 Methods of Reflow
4.3.2 Reflow Temperature and Limit Count of Reflow Runs
4.3.3 Temperature Profile
4.3.4 After Reflow

Section 5 Solder Joint Failure and Solution
5.1 Examples of Good or Defective Solder Joints
5.2 Common Abnormalities
5.2.1 Voids
5.2.2 Solder Balls
5.2.3 Non-Wetting

Section 6 Other failure cases
6.1 Short Circuiting with WL-CSP Side Surface
6.2 Chip Crack
6.3 Solder release characteristics
6.4 Soldering issue caused by Exterior Pads on Devices

■Section 1 Preface

In recent years, mobile electronic products such as smartphones and tablet devices are constantly improving with more functions and applications squeezed into thin, compact and lightweight designs. Such features mean all components also needs to enhance their performance as well as downsizing.

In order to respond to these demands, Nuvoton has ramped up production of Dual MOSFET(metal-oxide-semiconductor field-effect transistor). This adopted Wafer Level Chip Scale Package(WL-CSP) for Lithium-Ion battery protection circuit, and has been evolving its technology since mass production in 2011.

During that time we have expanded our product portfolio such as Single type MOSFET for Load Switch circuit, small size product such as 0.6mm×0.6mm and low on-resistance products for high current and contributed in improving applications for more smaller, lighter, more multifunctional, higher performance applications with varieties of WL-CSP solutions.

In general, it can be said that smaller devices, therefore narrower pitches of lands and pads, would require even more high-tech mounting technology to get a sufficient bonding or junction. Based on the vast know-how and experience of mounting technology, this application note has been compiled to support design of solder stencil and land pattern to help improve and maintain assembly productivity and reliability.

*The design examples and recommendations stated in this application note are for reference and may/will need adjustments, depending on the environment/equipment of the assembly line.

Figure1 WL-CSP and application samples

■ Section 2 Devices in this Document

Figure2 is a list of WL-CSP model products. Nuvoton WL-CSP is classified into three types depending on mounting conditions. Please check the classification of products you are using in this list and refer to the explanation for each classification in this Document.

Products	Type	Products	Type	Products	Type
FC6B21100L	A	KFC6B22220L	A	KFJ4B01110L	B
FCAB21910L	A	KFC6B22500L	A	KFJ4B01120L	A
FCAB21A60L	A	KFC7P23440L	A	KFK4B12034NL	B
FCAB22710L	A	KFCAB30029NL	C	KFK4A12035NL	A
FK4B01100L	A	KFCAB21260L	A	KFK4B02910L	A
FK4B01110L	B	KFCAB21350L	A	KFK4A25019NL	A
FK4B01120L	A	KFCAB21490L	A	KFK4B40028NU	A
FK9B0439ZL	A	KFCAB21520L	A	KFK9B0463ZL	A
KFC4A21300L	B	KFCAB21740L	A	KFJ9B0466ZL	A
KFC4B21080L	A	KFCAB21770L	A		
KFC4B21210L	A	KFCAB21830L	A		
KFC4B21220L	A	KFCAB21860L	C		
KFC4B21280L	A	KFCAB21890L	A		
KFC4B21300L	B	KFCAB21A50L	A		
KFC4B21320L	A	KFCAB21B10L	C		
KFC4B21330L	A	KFCAB21B30L	C		
KFC4B22070L	A	KFCAB21B50L	A		
KFC4B22180L	A	KFCAB21C00L	C		
KFC4B22270L	A	KFCAB12004NL	A		
KFC4B22670L	A	KFCAB21C30L	A		
KFC4B22690L	A	KFCAB22370L	A		
KFC4B22830L	A	KFCAB22510L	A		
KFC4B21A30L	A	KFCAB22620L	C		
KFC6B21150L	A	KFCAB22630L	C		
KFC6B21810L	A	KFCAB22680L	C		
KFC6B21810L	A	KFCAB22014NL	C		
KFC6B21B70L	A	KFCAB22020NL	C		
KFC6B22090L	A	KFCAB22860L	A		
KFC6B22100L	A	KFCAB22900L	C		
KFC6B22160L	A	KFJ4B01100L	A		

Figure2 Nuvoton WL-CSP List of model products

■ Section 3 PCB and Solder Stencil Designs

In this section, design information on (1) Solder Resist, (2) Land Pattern, and (3) Solder Stencil as shown in Figure3 is provided.

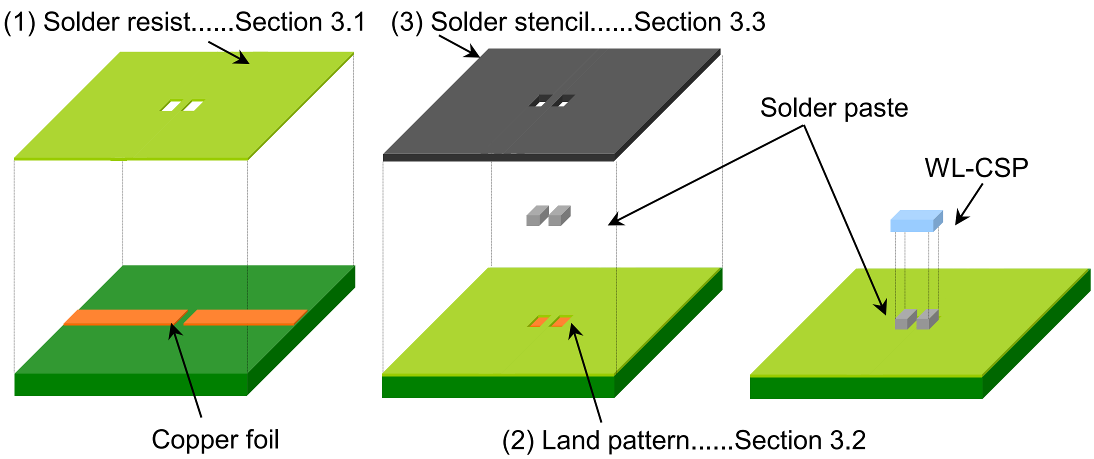


Figure3 Materials used for mounting process

3.1 Solder Resist Design

There are two types of solder resist design. Solder Mask Defined (SMD) and Non Solder Mask Defined (NSMD). As shown in Figure4, for SMD the solder resist overlays the wiring pattern of the PCB, whereas for NSMD the solder resist doesn't overlay the wiring pattern of the PCB.

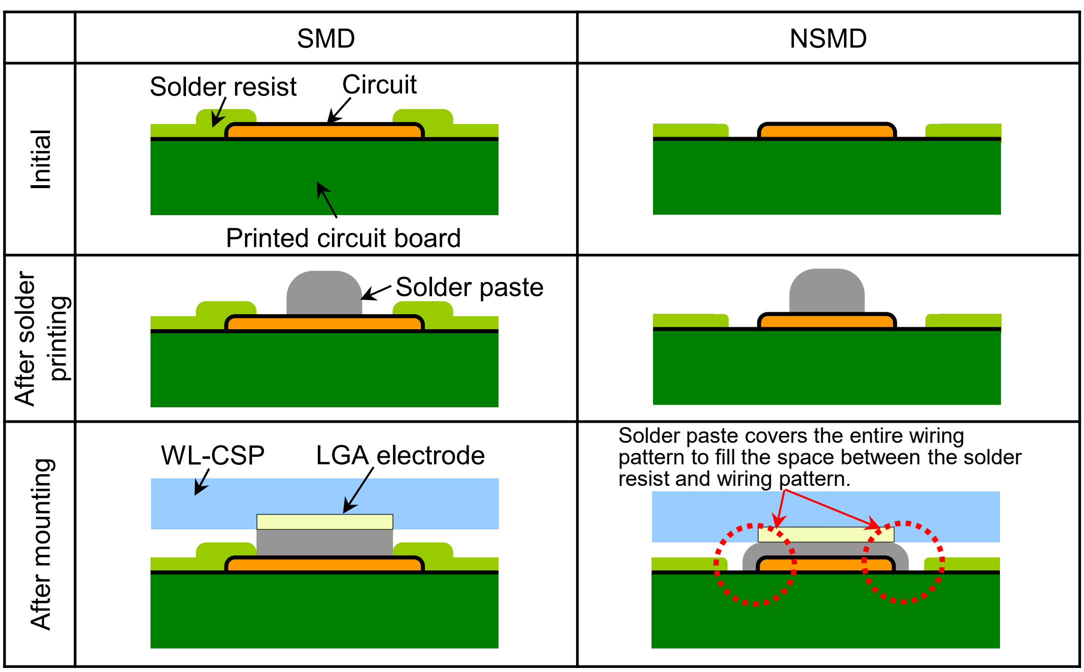


Figure4 Comparison of SMD and NSMD

As shown in Figure4, NSMD allows the solder paste to cover the entire land pattern of the PCB and it helps to make solder joint stronger and temperature life cycle longer, compared to SMD.

However, for NSMD designs, as shown in Figure5, uncovered portions of the wiring pattern, especially edge and corner part, we called “neck part”, can be peeled off by lower mechanical stress than SMD types. In addition, if land pattern is designed larger than the device pad, and have not placed solder resist on the circuit pattern connected to WL-CSP pad, solder might stick out to the side of device, causing short circuit between pad electrode and device surface.(*1)

Therefore Nuvoton recommends SMD as the solder resist for WL-CSP mounting board.

*1：Please refer to Section6 for short circuiting.

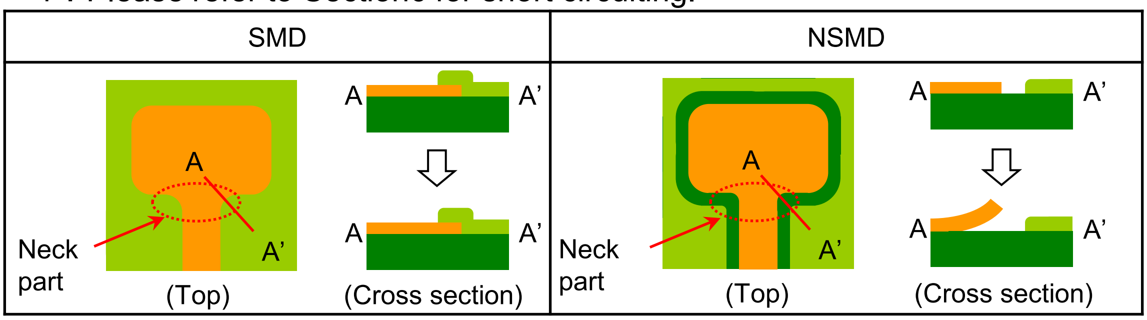


Figure5 Pad/Circuit peeling

3.2 Land Pattern Design

All WL-CSP with pads on the bottom side of the device, will require reflow soldering (*2) to bond to the PCB. Upon reflow soldering, devices might be placed on unexpected location on PCB due to misalignment of placement machine and solder printing. Such misalignments can be reset by self alignment during reflow process, with optimized design of PCB land pattern. In case of type A, the risk can be reduced by design same land pattern with the device pad layout as shown in Figure 6-1(b). In case of type B, Larger designed land pattern is also another way to avoid solder release characteristics worsening(*3). More specifically, designing PCB land pattern of φ0.2mm to device pad size of φ0.15mm is recommended as shown in Figure6-2(b). In case of type C, It is recommended to design enlarged land pattern of gate as shown in Figure6-3(b) land pattern figure surrounded by red thick line, in order to avoid soldering issue caused by exterior pads on devices (*4). Additionally there are some products to enlarge source pattern. Therefore please confirm optimized land pattern for each product with individual Datasheet (separate paper).

The land pattern distances in Figure6 are defined as shown in Figure7.

*2：Please refer to Section4 for reflow method.

*3：Please refer to Section6.3 for solder release characteristics worsening.

*4：Please refer to Section6.4 for soldering issue caused by exterior pads on devices.

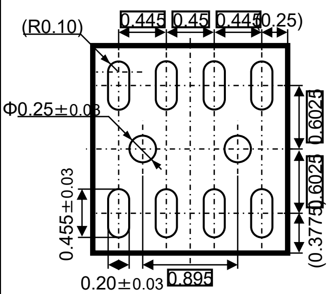
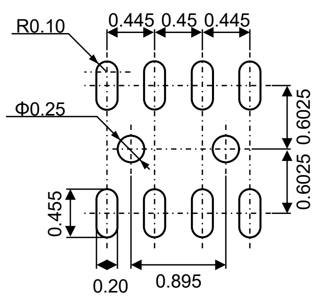
3.3 Solder Stencil Design

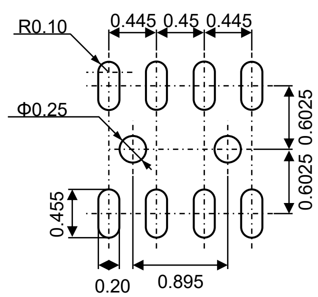
Design solder stencil is very important to maintain high mounting quality such as sufficient solder joint and no solder ball (*5). Excessive solder paste increases the risk of causing solder balls, and deficiency of solder paste also increases the risk of causing no solder connection.

Nuvoton has studied a variety combination of PCB's solder stencil designs and the materials, and recommends some combinations confirmed to maintain high mounting quality. For example, in case of type A or type C, 80μm thickness of solder stencil, and solder stencil pattern of 1:1 ratio with device pad size as shown in Figure6-1(C),6-3(c). In case of type B, 80μm thickness of solder stencil and device pad size of φ0.15mm to solder stencil pattern of φ0.2mm as shown in Figure6-2(c).

These reference designs should be evaluated together with actual assembly environment and solder paste.

*5：Refer to Section 5.2.2 for solder balls.

<table>
<tr><td colspan="3">e.g. KFCAB21B50L</td></tr>
<tr><td>(a) Device Outline</td><td>(b) Land Pattern</td><td>(c) Solder Stencil Pattern</td></tr>
<tr><td>
</td><td>

Land pattern and device pad size ratio is 1:1</td><td>

Solder stencil pattern and device pad size ratio is 1:1</td></tr>
</table>

Figure6-1 Design recommendations of land pattern and stencils (Unit：mm)
*Device outline describes electrode pad surface

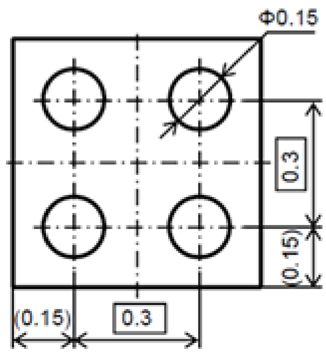
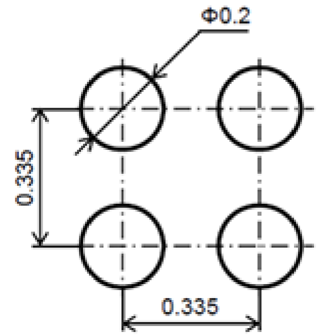
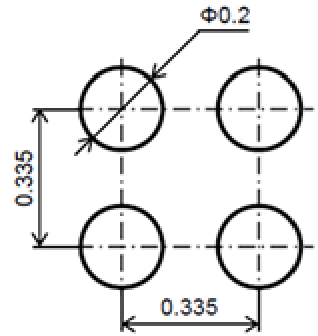
e.g. KFC4B21300L		
(a) Device outline	(b) Land pattern	(c) Solder stencil pattern
		
Device pad dia. φ0.15	Land pattern dia. φ0.2	Solder stencil pattern dia. Φ0.2

Figure6-2 Design recommendations of land pattern and stencils (Unit：mm)
*Device outline shown from pad side view

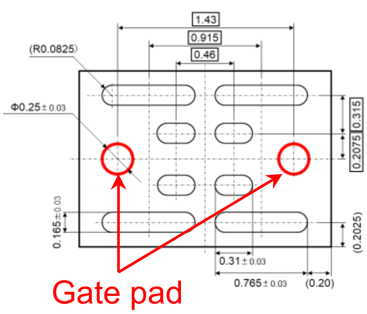
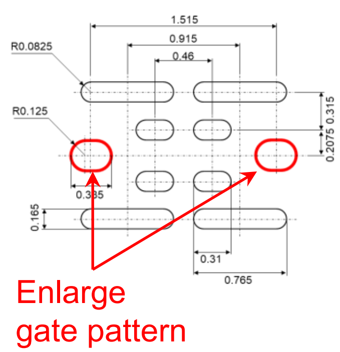
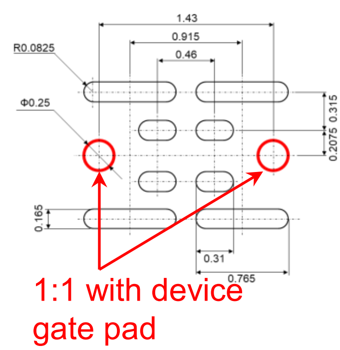
e.g. KFCAB21B30L		
(a) Device outline	(b) Land pattern	(c) Solder stencil pattern
		
	Refer to separate Datasheet for recommended land pattern	Size ratio of solder stencil pattern and device pad are 1:1 (Including gate pad)

Figure6-3 Design recommendations of land pattern and stencils (Unit：mm)
*Device outline describes electrode pad surface

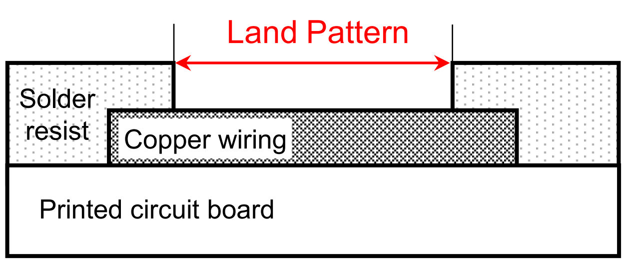


Figure7 Definition of land pattern (Cross section)

■Section 4 PCB Mounting Conditions

In this section, mounting process conditions we recommend are provided, based on our study results. The process includes solder printing, mounting and reflow process. Figure8 shows an overview of the process.

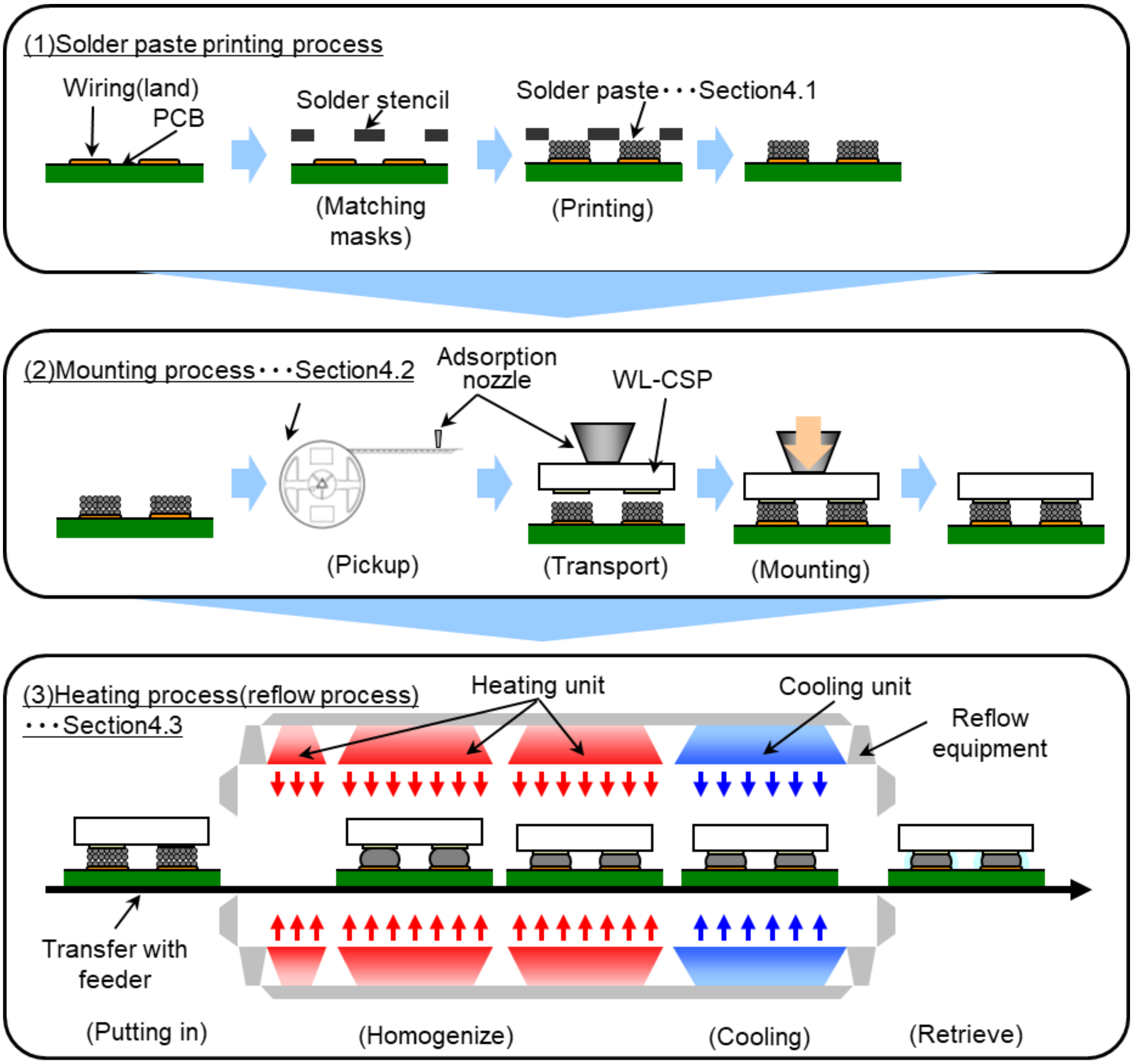


Figure8 Overview of chip bonding process

4.1 Solder Paste

The main substances of solder paste are solder powder and flux. The most general type of solder paste contains approximately 80 to 95wt% of solder powder. The ratio of solder powder determines the viscosity of the paste, and the viscosity directly affects the thickness and solder wetting after reflow. And there are variety types of grain size of solder powder, which is shown in Figure9. If the grain size is too large, high mounting quality may not be maintained. On the other hand, the smaller the grain size is, the more amount of solder powder unit area in solder paste. Therefore, in case of excessive amount of solder paste with small grain size, there is a higher possibility that solder ball occurs, compared to large grain size. Type4(20μm～38μm) solder grain size is recommended.

Please be noted that surface oxidation of solder powder might cause solder ball, solder void and also no solder joint due to the paste wetting. Especially with smaller grain size, it tends to have larger influence caused by surface oxidation. Thus, you should handle and store the paste carefully. For this reason, it can be said that selecting solder paste is also important as to maintain high mounting quality as well as designing solder stencil.

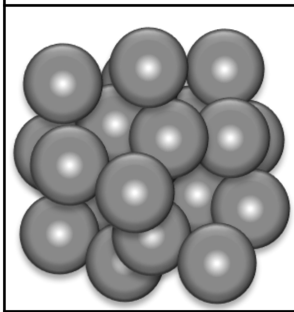
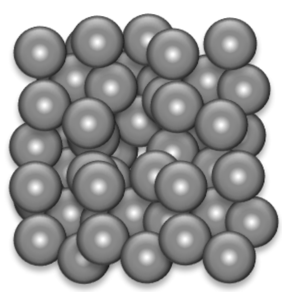
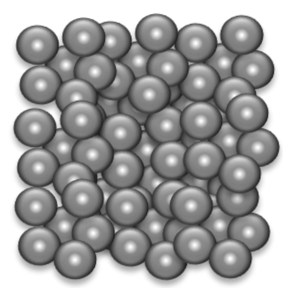
Grain size of Solder Powder		
Type3	Type4 (Recommended)	Type5
25μm～45μm	20μm～38μm	15μm～25μm
		

Figure9 Solder powder grain size image in solder paste

4.2 Loading Process

4.2.1 ESD Control

It's required to prevent from sticking to top tape during loading process. Figure10 shows the case where devices sticks to the peeled top tape due to an adsorption caused by static electricity, so please prevent this with electrical neutralization process and temperature/humidity control.

More specifically, avoiding static electricity effects for equipment and product storage, grounding workbenches, loading work on antistatic sheets, wearing a grounding band when touching reel/embossing, electrical neutralization with an ionize, and more. Vacuum suction from the back side of embosser in the feeder section can as well prevent sticking devices.

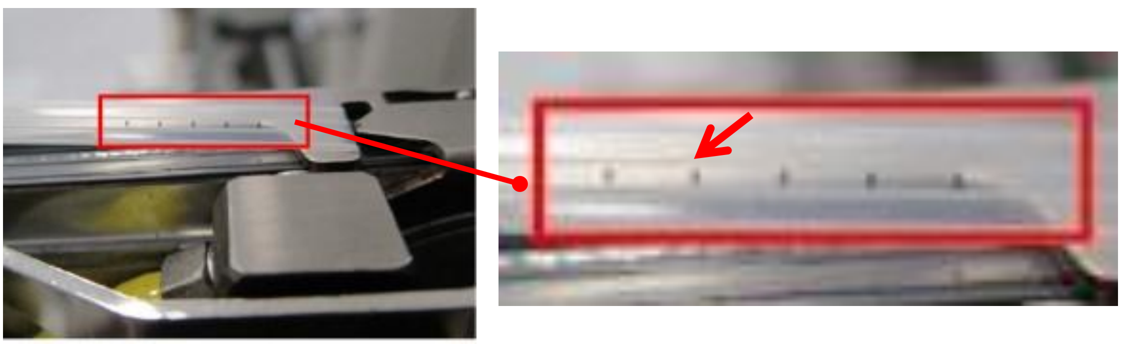
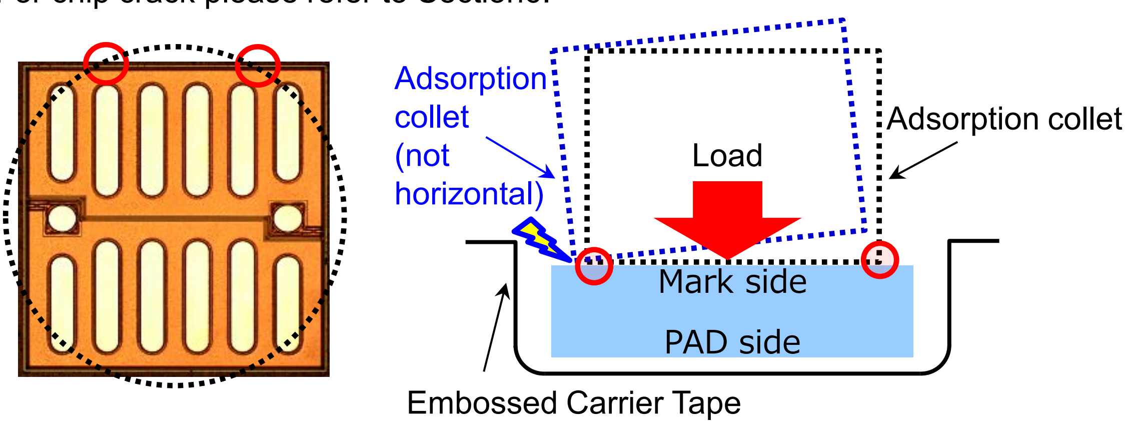


Figure10 Sticking to top tape

4.2.2 Loading Control by Adsorption Collet

As shown in Figure11, during loading process, optimizing adsorption collet load control during pickup and setting adsorption collet horizontal to WL-CSP can reduce the possibility of chip crack(*6). As a general guideline for load control, the recommended condition is smaller than 1N.

*6：For chip crack please refer to Section6.



(a)Adsorption Collet and Device top view

(b)Cross-section view of Embossed Carrier Tape

Figure11 Adsorption collet stress

4.3 Reflow

4.3.1 Methods of Reflow

Reflow is the process to bond the device to PCB. The device is first placed on the PCB and then put in furnace to form solder joint between the device pad and land on PCB Furnace is carefully tuned where the temperature is controlled depending on the stage of the process from pre-heating to cooling, as shown in Figure8(3). There are two main methods of reflow, Infrared reflow method and Convection reflow method, which is shown in Figure12 as well as the differences of the methods.

For Infrared Reflow, devices are heated by infrared radiant heat. The advantages are lower operating cost and easier maintenance than Convection reflow. However, it is hard to control temperature in furnace, because the radiant heat is affected by material and shape of the heated devices and the pads aren't directly heated but through the PCB by conductive heat. It causes uneven temperature in furnace, so may make solder joint strength weak and uneven.

For Convection Reflow, devices are heated in air and/or nitrogen atmosphere. Compared to Infrared Reflow, it takes longer heating time. However, the devises and solder pastes in furnace can be heated at more even temperature, because both convection and conductive heat help materials in the furnace keep the even temperature. Thus, we recommend Convection Reflow method for WL-CSP devices.

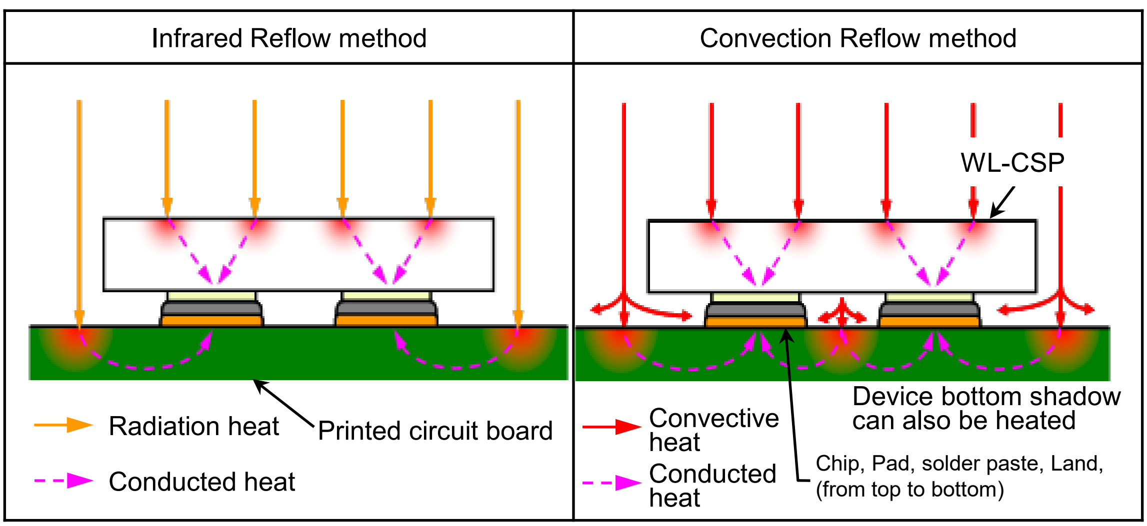


Figure12 Heat transmission path of infrared reflow method and convection reflow method

4.3.2 Reflow Temperature and Limit Count of Reflow Runs

Reliability test has been performed for all Nuvoton WL-CSP products, based on IPC/JEDEC J-STD-020 specifications. The test samples are exposed to moisture and reflowed 5 times at the maximum temperature of 260°C , then we confirm the samples pass the tests. So the products can withstand heat stress which deserves to five reflow operations, however according to the specifications, it is preferred to perform within 3 times reflow operations. The number of reflow cycles must be set considered to solder paste and manufacturing environment and/or equipment if the product applied additional heat stress such as rework operation and double-sided mounting.

4.3.3 Temperature Profile

We have performed several evaluations with variety types of solder paste. Figure13 shows the temperature profile we recommend, based on the evaluation results. The profile can be used for reference when you set reflow temperature.

Preheating

Thermal capacity of each device on PCB is different due to each size and the difference causes uneven temperature during reflow. To prevent this, the furnace temperature must be preheated to equalize temperatures of each device on the PCB before ramping up to peak temperature. The preheat also help to prevent solder voids, by evaporating volatile material in flux and reducing surface oxidation of solder powder.

In addition to temperature, time is also an important factor in preheating process. If the temperature is set too low or the time is set too short, the flux material may remain until the heating time and causes voids and/or solder balls. On the other hand, when the preheating temperature is too high or the time is too long, the solder wetting is affected and may cause making poor and weak solder joint.

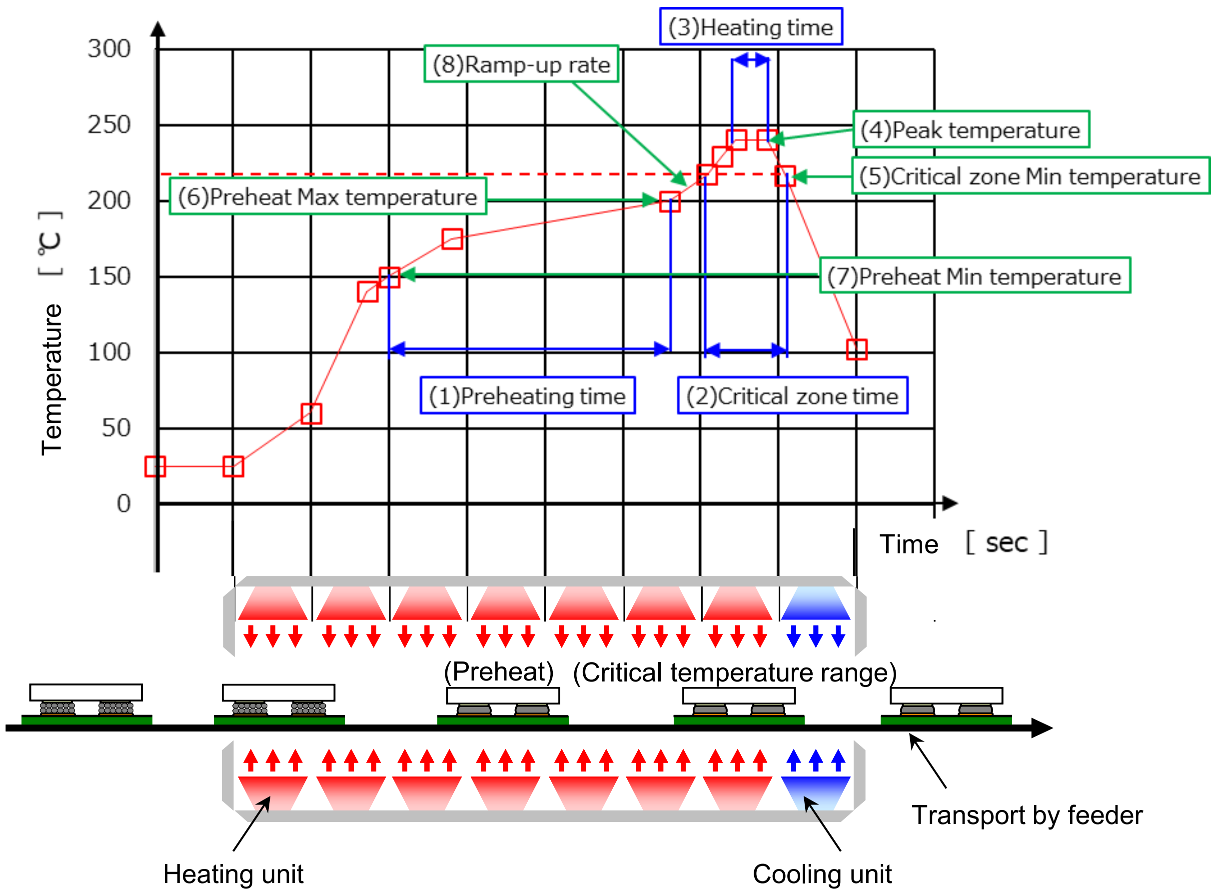
When mounting Nuvoton WL-CSP products, the preheating time should be set in between 60 to 120 sec (90 sec is recommended) and the average temperature at 175°C. In this case, the “Preheating time” is defined as the time span the temperature rises from 150°C to 200°C.

Critical Zone

The Critical Zone is a temperature zone where Sn (tin) - Ag (silver) lead-free solder melts. It is generally over between 210°C to 221°C. We define critical zone time as time the temp reaches over 217°C. Since excessively long and high temperature exposure causes weak solder joint and/or connection failures as stated in 4.3.2., processing time in the critical zone should be approximately 105 sec or less and the peak temperature should be approximately 240°C.

Temperature Ramp Rate

The temperature ramp rate from the Preheat zone to the Critical zone must also be controlled. Based on our experiments, the ramp rate should be set around between 2 to 3 °C/sec (2.5°C/sec is recommended). An immediate and sudden temperature rise applies thermal shock to the device and it may cause cracks, flux boiling, solder voids and solder balls.



(1)	Preheating time	90 [sec]	(5)	Critical zone Min temperature	217 [℃]
(2)	Critical temperature zone time	105 [sec]	(6)	Preheat Max temperature	200 [℃]
(3)	Heating time	10 [sec]	(7)	Preheat Min temperature	150 [℃]
(4)	Peak temperature	240 [℃]	(8)	Ramp rate	2.5 [℃/sec]

Figure13 Temperature profile example of reflow processing

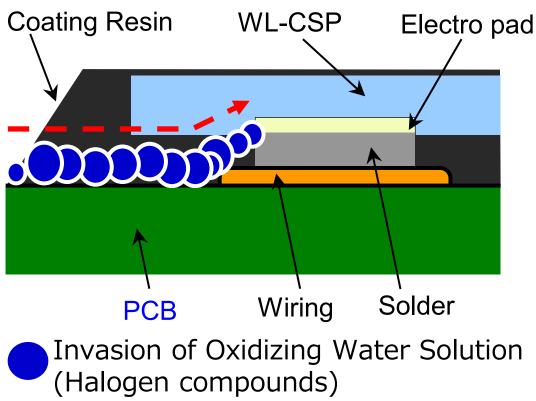
4.3.4 After Reflow

After the reflow process shown in Figure8, cleaning flux on solder is recommended in order to prevent electrode corrosion.

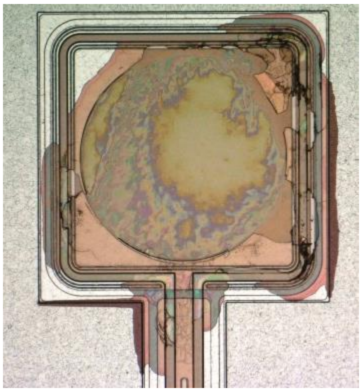
Figure14 shows an example of electrode corrosion. As shown in Figure14(a), solders and coating resin contains halogen compounds(acid-based substance). Acidic substance reacts with moisture and forms oxidizing water solutions, which may cause electrode corrosion, as shown in Figure14(b).

Even without cleaning, using rosin free solder which does not contain chlorine, halogen compound, and/or organic acid helps reduce the risk of electrode corrosion.

Please perform proper verification to prevent mounting failures, including the corrosion described above.



(a)Invasion of oxidizing water solution(Cross-section view)



(b)Picture of electrode corrosion (Pad side)

Figure14 Electrode corrosion

■ Section 5 Solder Joint Failure and Solution

As discussed up to this point, optimizing the land pattern, solder stencil design, and evaluating reflow conditions with the combination of solder pastes will lead to ideal solder joints. However, before reaching such conditions, it is possible to encounter other problems or abnormalities through evaluations. In this section, some abnormalities and most common failures will be described to provide a better understanding of perfecting the process. In addition, the X-ray inspection system is the most effective method for solder joint inspection after mounting process.

5.1 Examples of Good or Defective Solder Joints

Shown in Figure15 is an X-ray photo of a good sample. The square in red dotted line indicates the outline of the WL-CSP, and the black circular objects indicate solder joints of the device and PCB. The gray area is the circuit pattern of the PCB. Listed in Figure16 are some samples of solder joints that are good and abnormal.

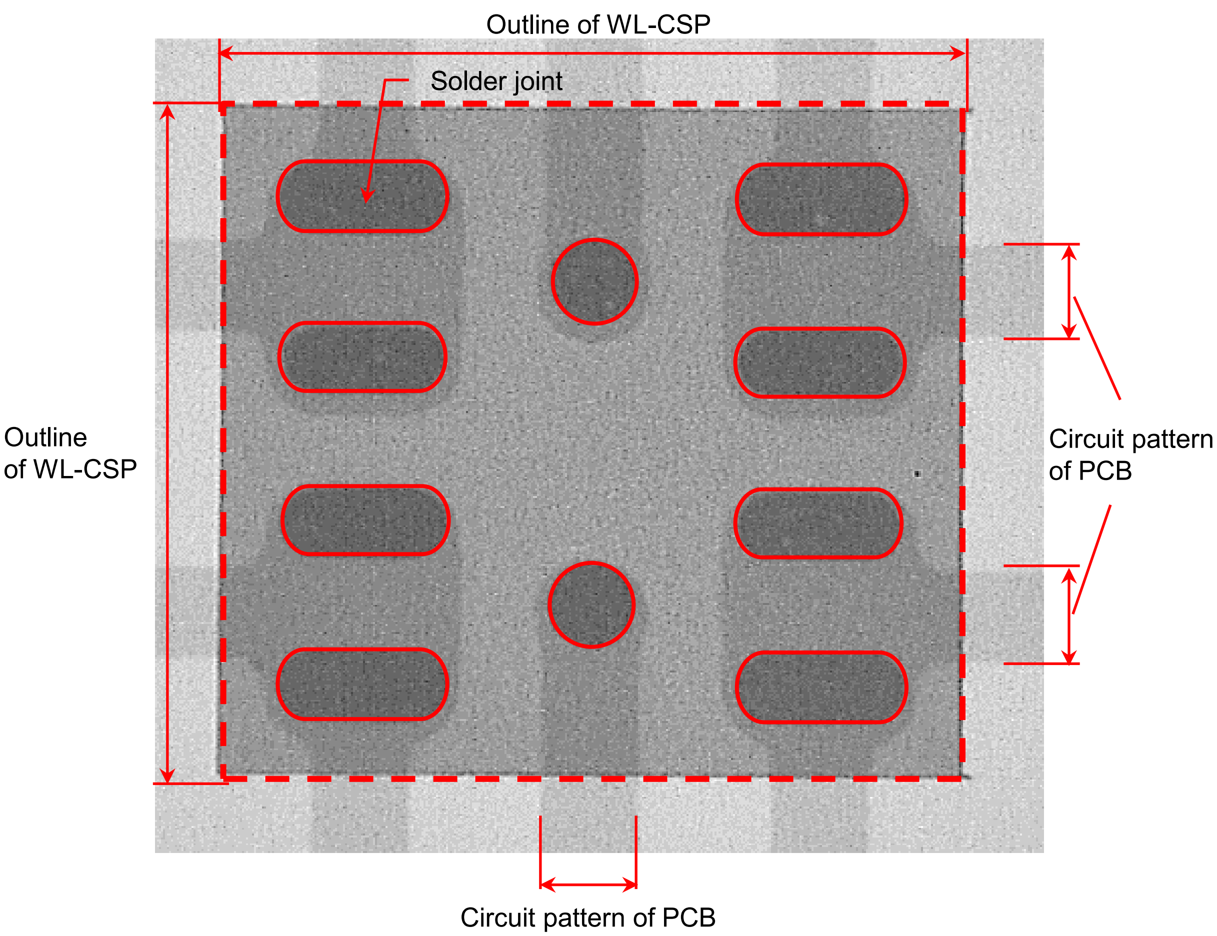


Figure15 Good sample

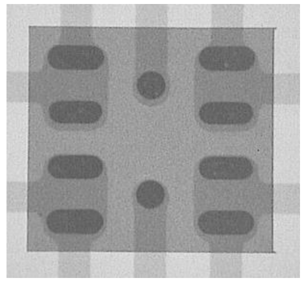
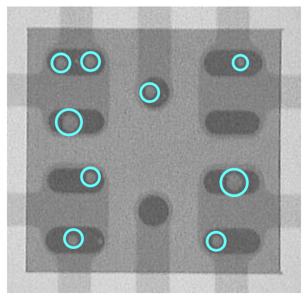
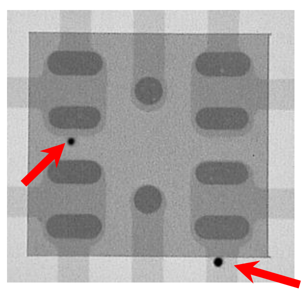
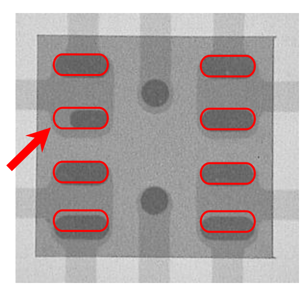
Condition	Example	Reference
Good sample		Figure15
Void		Section 5.2.1
Solder ball		Section 5.2.2
Non-wetting		Section 5.2.3

Figure16 Examples of good and failure solder joints

*Note: Failure samples were made intentionally strictly for explanatory purposes in the note.

5.2 Common Abnormalities

5.2.1 Voids

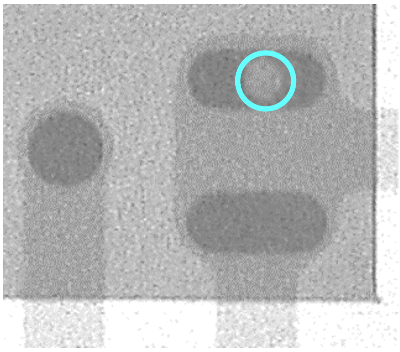


Figure17 Solder void

As shown in Figure17 with light blue circle, a void seen in the solder joint is called solder void.
In most cases, the voids are caused by flux-gas trapped inside the solder paste after mounting process. These type of solder voids happen randomly but can be minimized by optimizing the reflow temperature profile (Refer to “4.3.3 Temperature Profile” and following for details).

Figure18 is the result of intentionally repeating reflow in order to accelerate void growth.

Void after 1st cycle of reflow process is fairly small and it continues to grow until 3rd cycle. However after the 4th cycle, the void cannot be seen, and has basically disintegrated. No void is also confirmed after 5th cycle. The mechanism of this phenomenon is shown in Figure19. As the diameter of the void grows during 3 cycles of reflow process, the edge of the void eventually reaches the end of the pad, which allows the flux-gas to be released from the solder paste. According to the evaluation result, deflating flux gas in solder paste is important to avoid the solder void thus you should preheat with appropriate condition and carefully design circuit pattern.

According to many industry standards such as IPC-A-610, the tolerance for void is stated as “less than 25%” of each solder joint area. Based on such standard, we have made various void size samples then have performed evaluations of electrical characteristics, thermal characteristics, and reliability. After all the evaluations we confirm ones with less than 25% void sized samples to pass all evaluations. When inspecting with X-ray visual, the defect limit should be, as stated above, all solder voids to be smaller than 25% of solder joint area of each pad.

In addition to flux gas remainders, there are other possibilities to cause solder voids, such as PCB pattern contamination and solder paste oxidization. In some cases, restored gas from the oxidization of solder remains in solder paste and causes solder void. Thus, you should avoid contamination on PCB and oxidization of solder paste surface to prevent from causing the solder void.

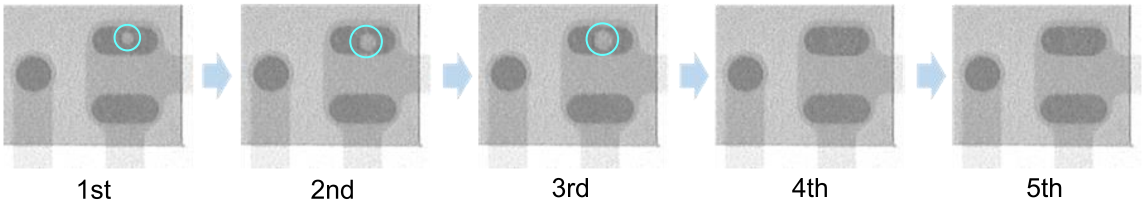


Figure18 X-ray photos of samples with each reflow cycle

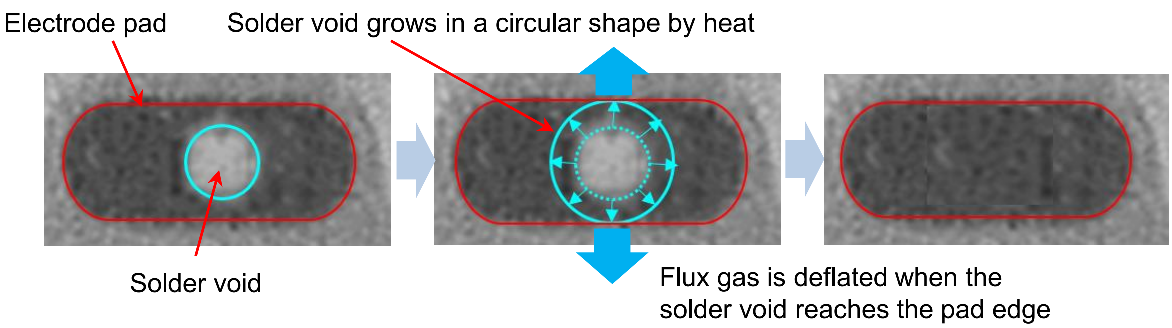


Figure19 Mechanism of solder voids and void growth

5.2.2 Solder Balls

As shown in Figure20 on X-ray image with red circles, these circular solder objects outside electrode pads are called Solder Balls. In many cases solder balls occur from Case(1) - (3) shown in Figure21 - 23.

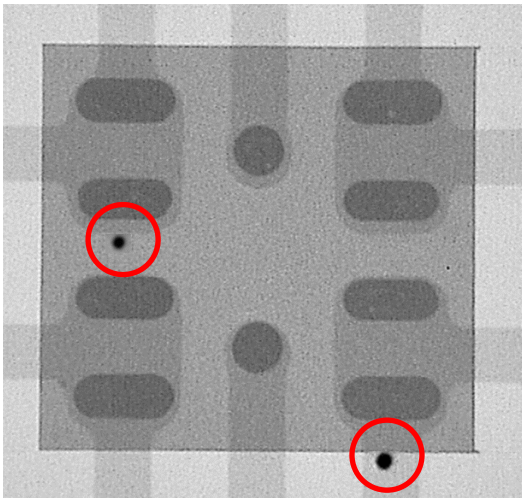


Figure20 X-ray photos of solder ball example

Case(1)

In case there is excessive amount of solder paste, extra solder paste will be pushed out of the pad during reflow process by the weight of device itself and harden into a spherical shape near the land pattern.

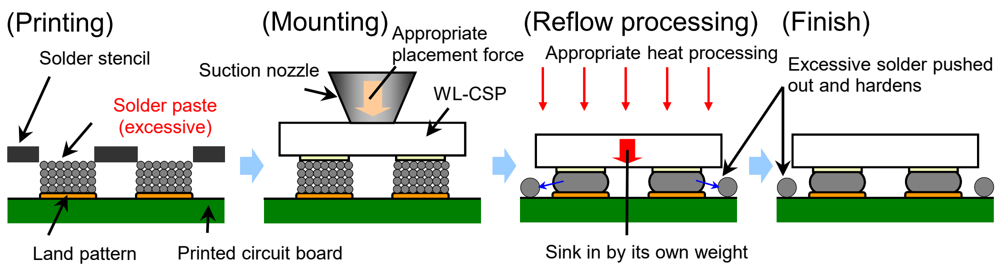


Figure21 Solder ball occurrence mechanism (1)

Case(2)

When the placement force during mounting process is too strong. The outcome is the same as in Case (1).

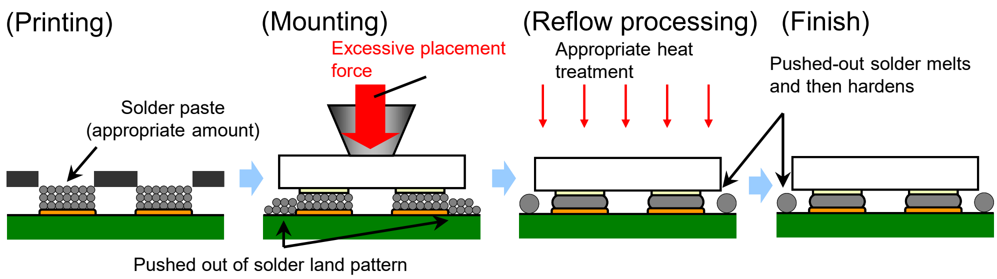


Figure22 Solder ball occurrence mechanism (2)

Case(3)

In case the temperature profile is inappropriate. As explained previously, extreme high temperature at preheat and/or excessively high ramp-up rate may cause a boiling or explosion of flux and other gases. The outcome is the same as in Case (1).

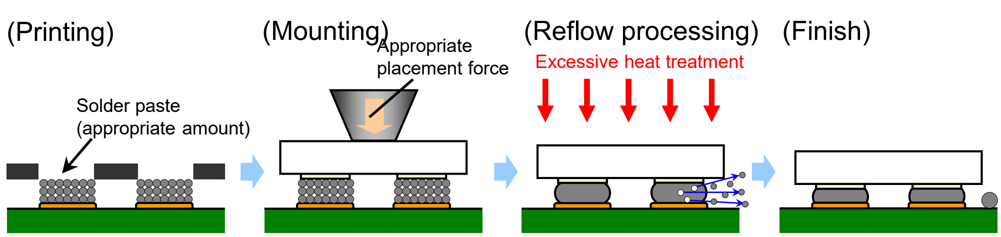


Figure23 Solder ball occurrence mechanism (3)

Although solder balls do not always affect the function and reliability in a critical way, they are not desirable and should be controlled as much as possible. In the worst case, solder balls can form a bridge between the pads, causing short-circuits. Electrical characteristic tests are recommended to screen out such bridge form.

5.2.3 Non-Wetting

In Figure24, red line indicates the pad size. If properly processed, should be covered with solder and look entirely black on the X-ray photo. Although all pads have a sufficient finish, the pad on the left side second from the top has a smaller black area, covering only a portion of the pad.

This is called Non-wetting. Non-wetting will most likely cause poor reliability performance, as well as increase the risk of open failures.

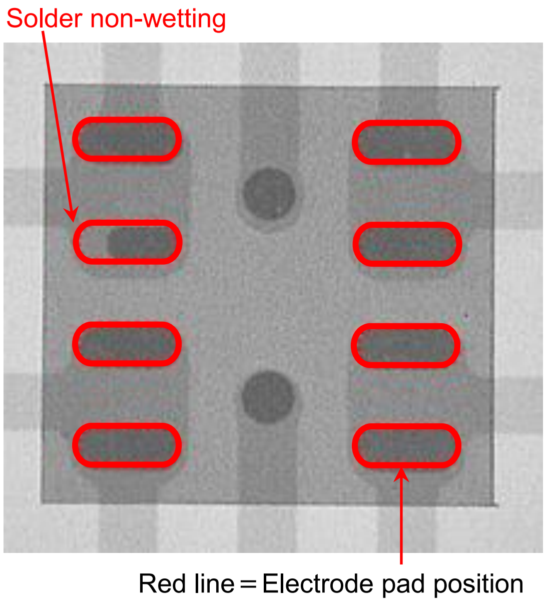


Figure24 Solder non-wetting

Non-wetting can occur from multiple cases such as excessive low amount of solder paste, clogged up solder stencil opening, and/or printing failure that lacks proper amount of solder. For corrective action please refer to Section 3.3 for solder stencil design recommendation, Section 4.1 for solder powder grain size, and consider reevaluating solder stencil. Clogged up solder stencil could also be the case, so it requires proper maintenance and management.

■Section 6 Other failure cases

Section5 described common abnormalities caused during mounting process. This section will cover other failure cases.

6.1 Short Circuiting with WL-CSP Side Surface

If land patterns are designed larger than device pad, and have not placed solder resist in wiring pattern connected to WL-CSP pad, solder might stick out to the sides of the device, causing short circuit between pad electrode and device side surface. Side surface of the device are equipotential with drain(*7), so if pad electrode and side surface connects through solder, it will be short circuited.

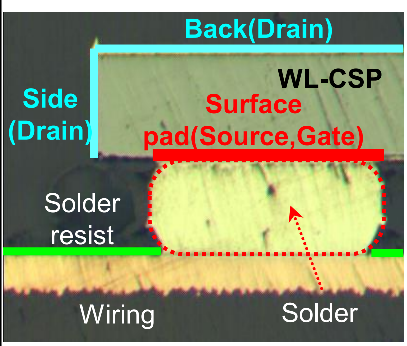
Figure25 shows good and abnormal samples. Areas surrounded by red dotted line is the solder connecting WL-CSP and wiring. Green line is the solder resist. (a)Good sample has solders contained correctly since land pattern/solder stencil pattern is properly designed. On the other hand (b)Abnormal sample's land pattern/solder stencil pattern are designed larger than device pad, resulting solder to reach device side surface shown in Figure25 with light blue line. In such situation where solder contacts side surface of device, the worst possible case is to cause short circuit with drain.

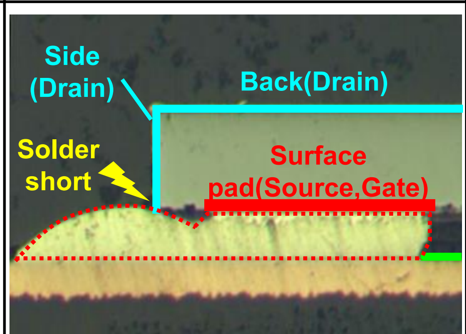
*7：Common drain dual type device

The dual type device, as shown in Figure25(c), is structured with 2 FET devices in 1 chip. Here, chip surface has source and gate pad, but drain pad does not exist. However, drain is common on chip backside.

Also, the drain on device sides and back has the same potential.

(a)Good sample	(b)Abnormal sample	(c)Equivalent circuit (Dual type)





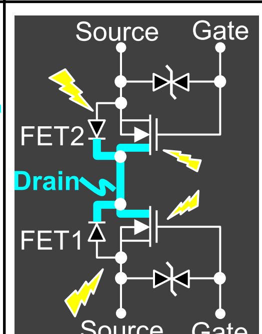


Figure25 Good sample and typical anomalies

6.2 Chip Crack

Cracks can occur when abnormal stress or weight is applied to the device during mounting process.

When cracks occur, process-by-process examination will be required to identify the root-cause of crack.

One of the method of the root-cause identify is to estimate by crack location. Figure26 shows the model case. In some cases(*8) occurrence situation can be identified by categorize crack.

*8 : Identifying crack initiation factors

Nuvoton performed load-bearing test for (1)point, surface /(2)board bending(including linear stress) shown in Figure26. Please refer to the separate “technical note” when identifying initiation factors.

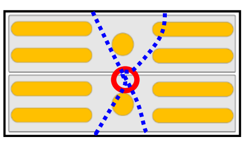
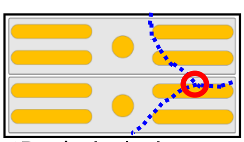
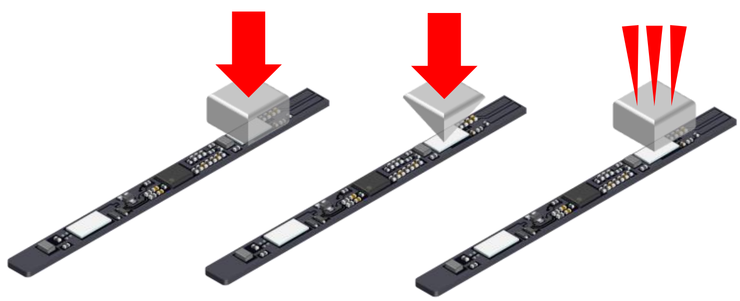
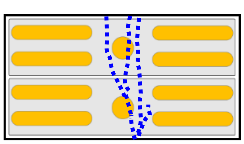
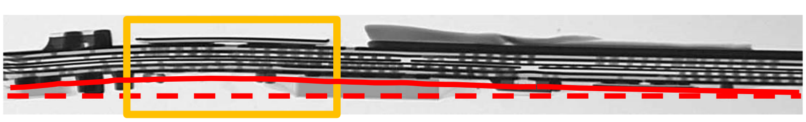
Crack category	Estimated Factor
  ※Red circle is start point(estimate)	(1)Stress application on point, surface : direct stress on device was the cause. 
	(2)Bending stress application : abnormal bending stress on board was the cause.  ※Linear stress application can also be the cause.

Figure26 Model case of crack

6.3 Solder release characteristics

This section covers solder release characteristics during solder paste printing process in Section4 Figure8(1).

Solder release characteristics worsens in situation where the force for solder paste to remain on the solder stencil aperture wall is larger than the force to remain on land pattern, when removing solder stencil from mounting board as shown in Figure27.

Figure28 is the image of solder paste condition after printing seen from above. If (a)Solder release characteristics is within preferable range, solder paste area is almost equal to land pattern area. If (b)Solder release characteristics is worse, solder paste area is smaller than land pattern area, lowering mounting reliability.

Device of type B has small pad size of φ0.15mm. Therefore it requires caution, as its force to remain on wiring(land) is easier to become less. More specifically, it is important to design land pattern/solder stencil pattern with device pad size of φ0.2mm larger than φ0.15mm, and selecting thinner solder stencil for example with thickness of 80μm as mentioned in Section3.2 and Section3.3. Additionally, selecting smaller solder grain size as mentioned in Section4.1 will be another counter measure. Ultimately, please confirm there is no solder release characteristics worsening, including other factors such as actual solder paste printing conditions.

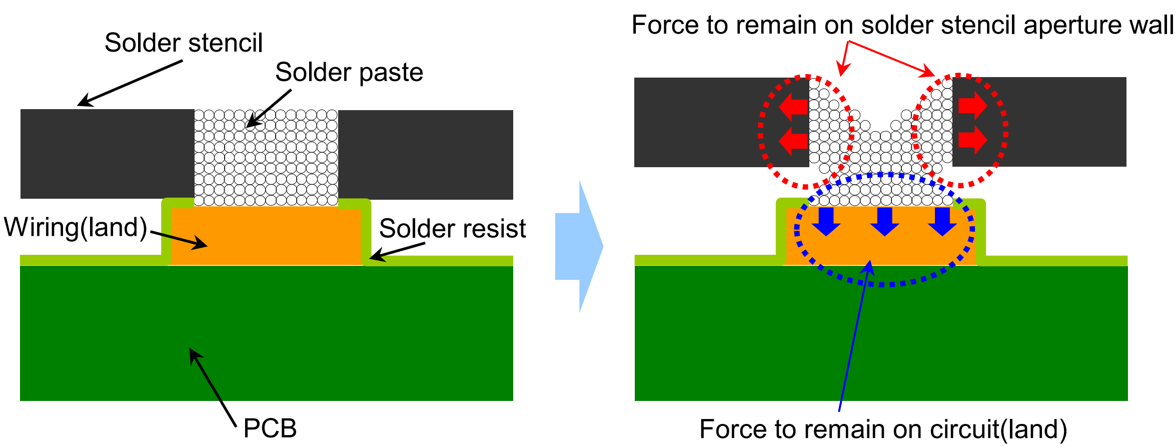
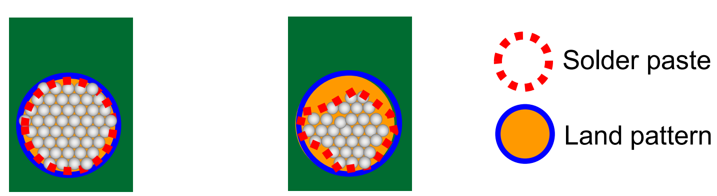


Figure27 Solder paste printing process



Land pattern area≒ Solder paste area | Land pattern area＞ Solder paste area

(a)Preferable degree of solder release-ability | (b)Solder release characteristics worsening

Figure28 Solder paste comparison with release characteristics

Important Notice

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

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