

KA49701A

Application Notes

Battery Monitoring IC (BMIC) for Industrial Application

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Chapter 1 Overview

1.1 Description

This is the application note for using KA49701A, which is a battery monitoring IC with protection function.

All the materials in this application notes are provided as design references only and not mass production guaranteed.

Sufficient evaluation and verification is required prior to mass production.

Chapter 2 Input RC and components setting for Cell Balance operation

2.1 RC external Cell Balancing

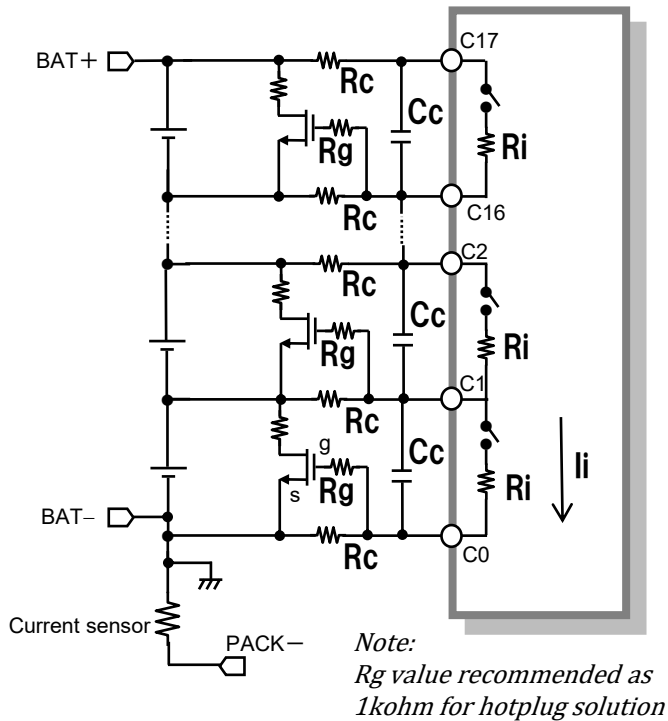


Fig. 2.1.1 Parameter for external cell balance

1) Calculate Rc

$$V_{gs} = \frac{V_{cell} * R_c}{2R_c + R_i} \quad R_i = 20\text{ohm}$$

$$V_{gs} \geq V_{th} (\text{in order to turn on FET})$$

$$\text{Suppose } V_{th} = 1.5V \quad V_{cell} = 3.7V$$

$$R_c \geq R_i * \frac{V_{th}}{V_{cell} - 2V_{th}} = 43\text{ohm}$$

and $R_c < 5\text{kohm}$ (for input impedance limitation)

$R_c = 1\text{kohm} \sim 4\text{kohm}$ is recommended

2) Calculate Cc

$$f_c = \frac{1}{2\pi * 2R_c * C_c} \leq \frac{f_s}{2}$$

f_c depends on the sampling time of our system

$$\left(\text{MAX}(f_c) = \left(\frac{f_s}{2} \right) = \frac{1}{50\mu s * 2} = 10\text{kHz} \right)$$

eg. when $f_s = 20\text{kHz}$, $R_c = 1\text{kohm}$

$$C_c \geq \frac{1}{f_s * \pi * 2R_c} = 0.008\mu F$$

Using $10 * C_c$ is recommended

2.2 RC internal Cell Balancing

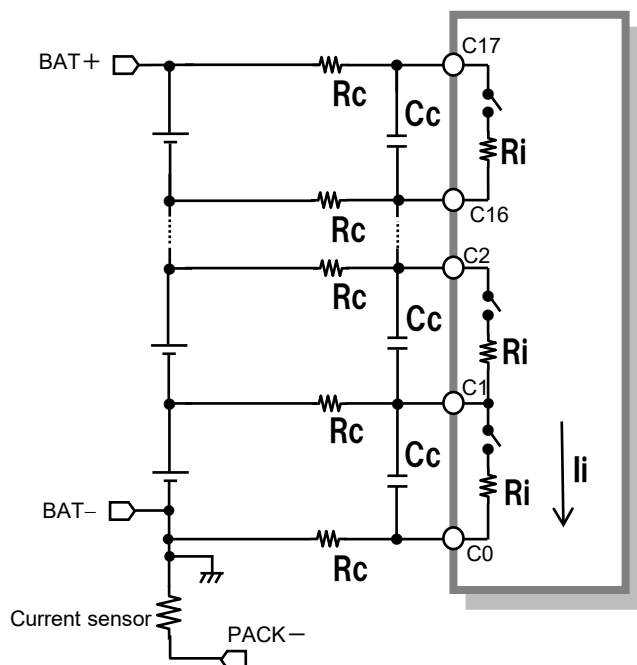


Fig. 2.2.1 Parameter for internal cell balance

1) Calculate Rc

$$I_i = \frac{V_{cell}}{2R_c + R_i}$$

I_i depends on the design target of your system
($\text{Max}(I_i) = 50\text{mA}$)

$$\text{Suppose } V_{cell} = 4.2V \quad I_i = 50\text{mA}$$

$$R_c \geq \frac{1}{2} * \left(\frac{V_{cell}}{I_i} - R_i \right) = 32\text{ohm}$$

2) Calculate Cc

$$f_c = \frac{1}{2\pi * 2R_c * C_c} \leq \frac{f_s}{2}$$

f_c depends on the sampling time of our system

$$\left(\text{MAX}(f_c) = \left(\frac{f_s}{2} \right) = \frac{1}{50\mu s * 2} = 10\text{kHz} \right)$$

eg. when $f_s = 20\text{kHz}$, $R_c = 40\text{ohm}$

$$C_c \geq \frac{1}{f_s * \pi * 2R_c} = 0.2\mu F$$

Using $10 * C_c$ is recommended

Chapter 2 Input RC and components setting for Cell Balance operation

2.3 NMOS for external cell balancing

When applying VBAT, high voltage may occur transiently between the external FET pins for cell balance because normally there is RC filter at VBAT line.

External Cell balance FET with high voltage tolerance is highly recommended to withstand this transient spike.

In case high voltage tolerance FET cannot be used in the system, user can consider to separate VBAT from C17 as shown in Fig.2.3.2.

Battery cells connection sequence is documented on page 20

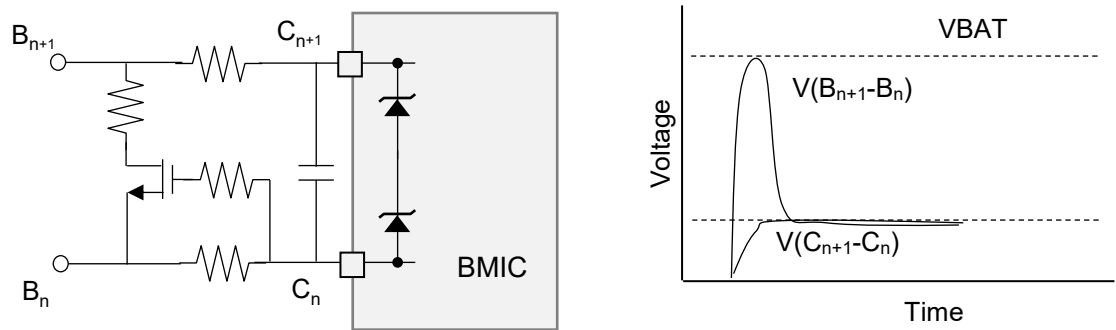


Fig. 2.3.1 Transient High Voltage

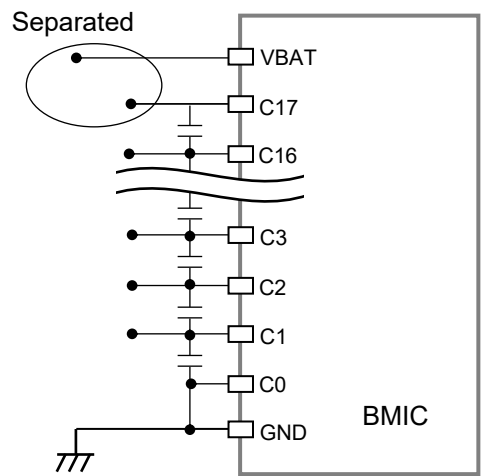


Fig. 2.3.2 Separated VBAT

Chapter 2 Input RC and components setting for Cell Balance operation

2.4 BJT for external cell balancing

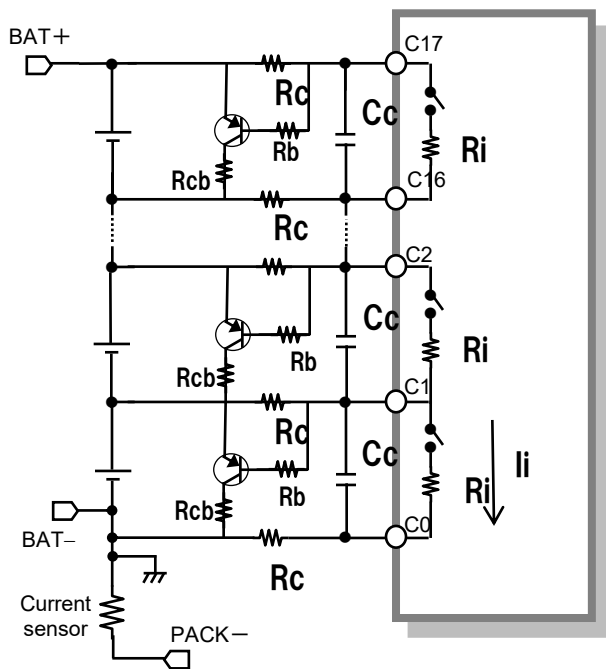


Fig. 2.4.1 Cell balance PNP

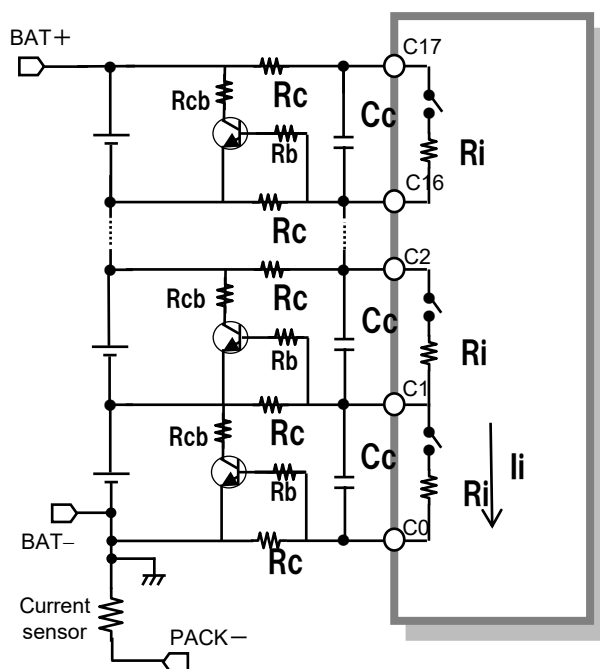


Fig. 2.4.2 Cell balance NPN

Example for parameter selection :

$R_c=1\text{kohm}$, $R_{cb}=75\text{ohm}$, $R_b=100\text{ohm}$

PNP BJT BC856 ($V_{eb}=0.8\text{V}$, $V_{ce(sat)}=-0.1\text{V}$)

$I_{cb} = (V_{cell} - V_{ce(sat)}) / R_{cb} = 48\text{mA}$ when $V_{cell} = 3.7\text{V}$

Chapter 3 Regulators Components and setting

3.1 VDD50 RC and BJT components

VDD50 BJT and RC devices must be connected as shown in Fig. 3.1.1.

C_{REGB} , R_{REGB} , C_{VDD50} , R_{VDD50} should be selected according to the loop characteristic of the regulator design with the select NPN BJT. The recommended RC values with the accompany BJT devices are shown in Table. 3.1.2 below. These devices are to be used together with the recommended NPN BJT to ensure the best stability and load transient performance for VDD50 regulator. In case NPN BJT is changed from the recommended list, it is necessary to perform enough evaluation check and optimize the RC value again.

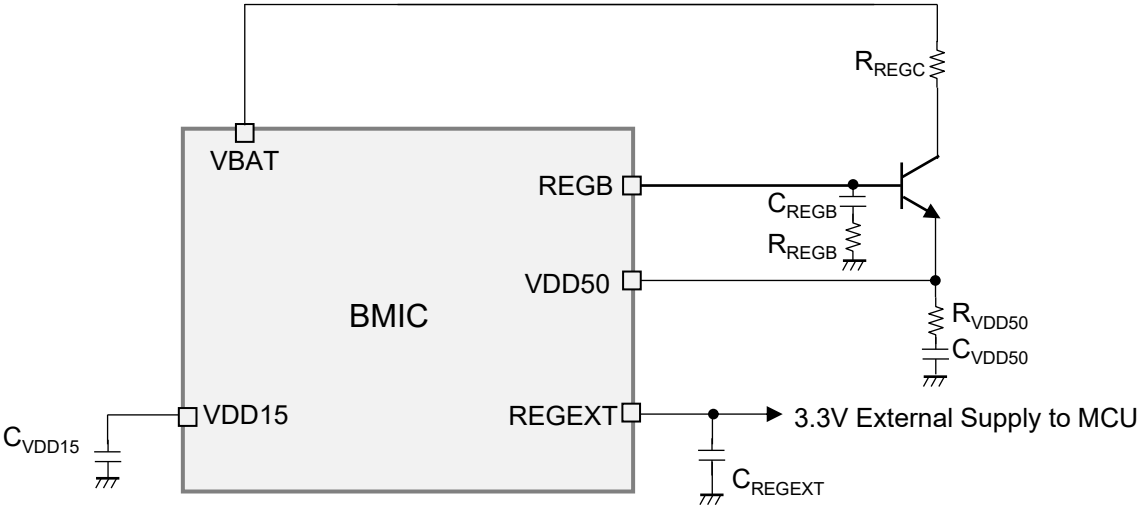


Fig. 3.1.1 VDD50 circuit

Component \ NPN	Recommended Component Value	Remark
	FZT458TA PZTA42T	
C_{REGB}	0.1uF	< ±50% for stability.
R_{REGB}	10kΩ	
C_{VDD50}	10uF	< ±30% for stability.
R_{VDD50}	0.33Ω	
R_{REGC}	390Ω	Min VBAT > 30V for 50mA max load condition. Choose resistor with suitable power dissipation ability.
C_{REGEXT}	1uF	
C_{VDD15}	2.2uF	
$C_{VDD50} / (C_{REGEXT})$ Ratio	> 5	Meet ratio requirement in tolerance condition.

Table. 3.1.2 Recommended BOM for VDD50 regulator

Chapter 3 Regulators Components and setting

VDD50 BJT and RC devices must be connected as shown in Fig. 3.1.1.

When selecting the NPN BJT, it is recommended to consider the following key factor as listed in Table. 3.1.3 below. Recommended BJT are listed in Table. 3.1.2.

BJT Parameters	Minimum	Maximum	Notes.
DC current gain (h_{FE})	Depends on output current needed	Depends on stability of regulator.	$h_{FE} = I_C / I_B$ (I_B is base current from REGB pin. I_C is output collector current.) Do ensure to use NPN beta > 40
Continuous collector current (I_C)	Internal IC loading (2mA) + REGEXT loading needed (max 50mA)	Depend on NPN current rating as well as thermal performance	REGEXT can be used as power supply for external circuit. OCP of REGEXT is up to 100mA. Do ensure to use NPN beta > 40 to keep $I_{VDD55} > I_{REGEXT}$
Collector emitter voltage (V_{CEO})	> Charger input or $> VBAT_{max}$ with sufficient margin	--	Maximum battery level $VBAT_{max}$ or charger input voltage will be seen at V_{CE} of the NPN. It is necessary for selected NPN to be able to withstand this voltage applied to it with sufficient margin being considered.
Thermal	$T_j = (P_d \times \theta_{j-a}) + T_a$	--	(1) $T_j \leq T_{jmax}$ BJT; (2) θ_{j-a} : Junction to ambient thermal Coefficient (It is recommended to have enough evaluation with the final PCB to determine actual θ_{j-a} and T_j of the NPN) (3) T_a =Ambient Temperature (4) $P_d = (VBAT_{max} - 5.0V) \times I_{Cmax}$

Table. 3.1.3 VDD50 BJT selection consideration

Chapter 3 Regulators Components and setting

3.2 REGEXT settings

REGEXT is a supply for external MCU and the internal interface I/O pins (ALARM1, FETOFF1, SPI, GPIO3, GPIO4). It takes the input voltage from VDD50 and generates a regulated 3.3V as shown in Fig. 3.2.1. Besides providing power for the interface I/O pins for internal usage, this REGEXT can support an external max load of 50mA for the MCU. The recommended components are shown in Table 3.2.3.

For MCU that uses 5V supply, VDD50 can be connected to REGEXT directly as shown in Fig. 3.2.2. Turn OFF REGEXT function by setting REGEXT_EN register to be “0”(address 0x02h[8]=“0”) The C_{REGEXT} is not needed in the 5V mode but do ensure VDD50 output cap is near to REGEXT routing in PCB layout to enhance transient response at REGEXT output. The recommended components are shown in Table 3.2.3.

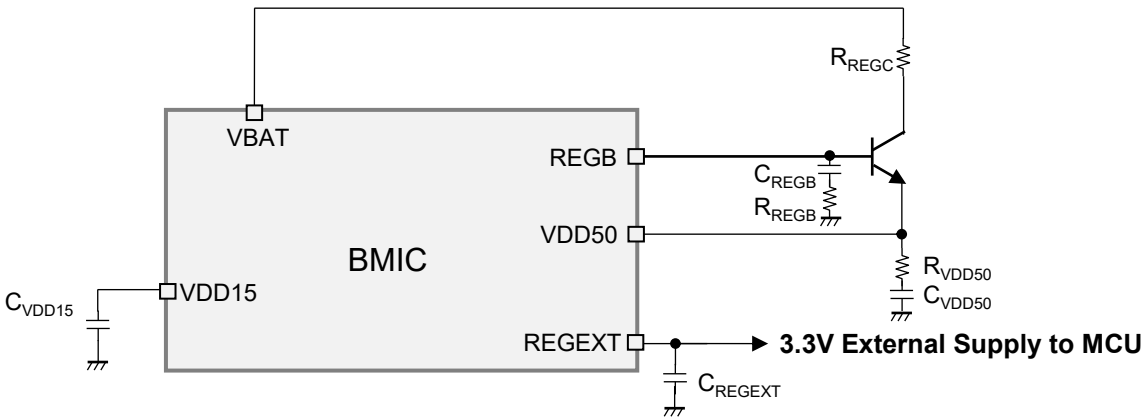


Fig. 3.2.1 REGEXT circuit for 3.3V regulation mode

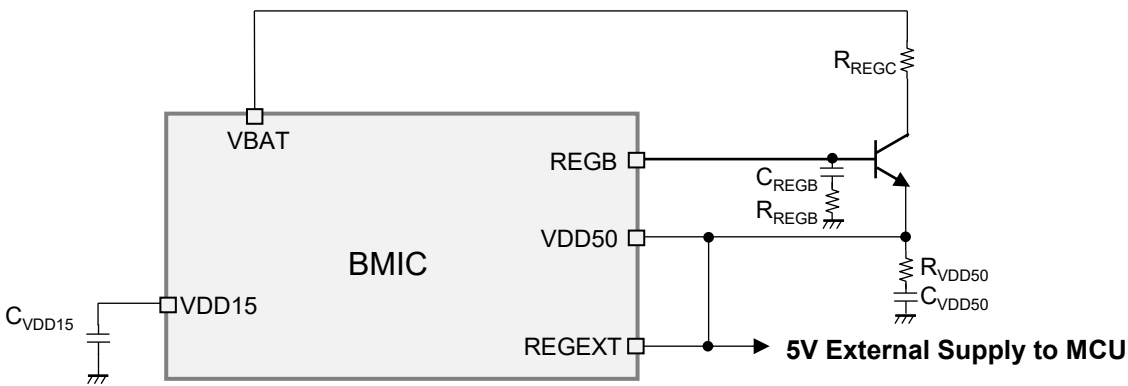


Fig. 3.2.2 REGEXT circuit for 5V mode

Component	Recommended Component Value		Remark
	3.3V REGEXT	5V REGEXT	
C_{REGEXT}	1uF	--	<±20% for stability.
C_{VDD15}	2.2uF	2.2uF	<±20% for stability.

Table. 3.2.3 Recommended BOM for REGEXT regulator

Chapter 3 Regulators Components and setting

3.3 Low current application

For low current application where REGEXT is not used as an external supply VDD50 can be connected to the REGB directly as shown in Fig. 3.3.1.

Fig. 3.3.2 shows the VDD50 low power mode setting for REGEXT=5V setting. The C_{REGEXT} is not needed in the 5V mode but do ensure VDD50 output cap is near to REGEXT routing in PCB layout to enhance transient response at REGEXT output

The recommended values for C_{VDD50} , C_{VDD15} , C_{REGEXT} are listed in Table. 3.3.3 for the proper startup of the system. Note that REGB can only supply 3.3mA current. Thus, VDD50 rise time can be up to 60ms. Please ensure that the VPC startup pulse is at least 100ms.



Fig. 3.3.1 VDD50 low power mode setting for REGEXT= 3.3V



Fig. 3.3.2 VDD50 low power mode setting for REGEXT= 5V

Component	Recommended Component Value		Remark
	3.3V REGEXT	5V REGEXT	
C_{VDD50}	10uF	10uF	<±20% for stability.
C_{REGEXT}	1uF	--	<±20% for stability.
C_{VDD15}	2.2uF	2.2uF	<±20% for stability.

Table. 3.3.3 Recommended components for VDD50 Low Current Application

Chapter 4 Unused pins setting

4.1 Unused Cell Pins:

- 1) All unused Cell pins named 'NC' should be connected via resistor of the same input filter value to the cells. Refer to Fig 4.1.1
- 2) For lower cells count system, the unused battery cells pins (C3~C15) should be connected as shown in Fig 4.1.2 / 4.1.3 / 4.1.4
- 3) Fig.4.1.4 is an example for 4-cell solution, the cells can be added from lower to upper (C3,C4...) for the solution which need more cells.

Fig. 4.1.1
Example of
16 Cell System

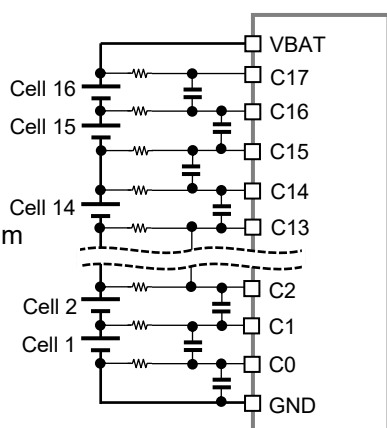


Fig. 4.1.2
Example of
14 Cell System

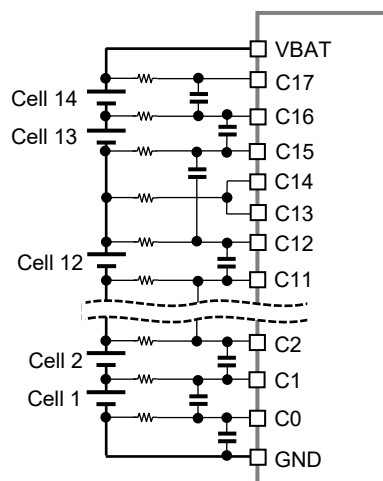


Fig. 4.1.3
Example of
12 Cell System

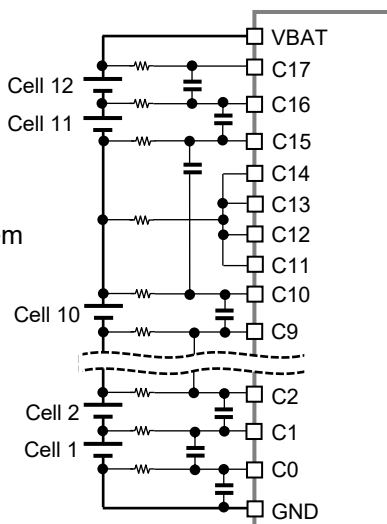
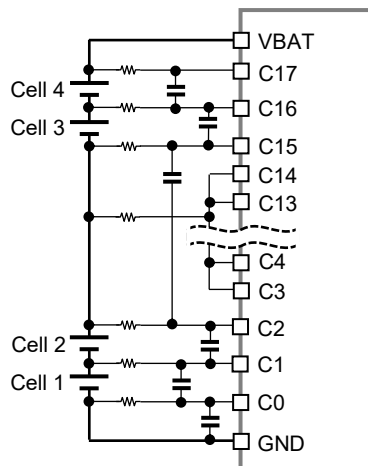


Fig. 4.1.4
Example of
4 Cell System



Chapter 4 Unused pins setting

4.2 Other unused pins:

Table.4.2.1 is a list for unused function pins and its recommended connection method when not used.

Function	Pin	Connection
Temperature	TMONIn (n=1~5)	Open
Nch FET	CHG, DIS	Open
Function pin	ALARM1	Open
	FETOFF	Ground
	SHDN	Ground
MCU communication	SDO	Open
	SDI, SCL, SEN	Open
Current	SRP/SRN	Open or Ground
GPIO	GPIO _n (n=1~4)	Open <i>Note *1</i>

Table. 4.2.1 Connection Example for unused function pins

Note :
*1 : Enabling the pull-down resistor by software is needed

Chapter 5 Battery Cell inputs connection sequence

5.1 Recommendation

Customer should strongly follow the below recommended Battery Cells connection sequence :

Connect the GND pin first, then followed by VBAT pin.

After that, connect lower cells in turn to upper cells.

GND → VBAT → Cell between C0-C1 → Cell between C1-C2 → Cell between...

5.2 Special case

If the recommended sequence can not be followed, but random connection or partial random connection sequence is required. Please use input resistors bigger than 100ohm for a fully random connection sequence.

For input resistors smaller than 100ohm, connect GND and VBAT first and then random connection for others cell voltage pin.

Note: Connection sequence for special case is verified by simulation with limited numbers of IC test, it seems no risks.

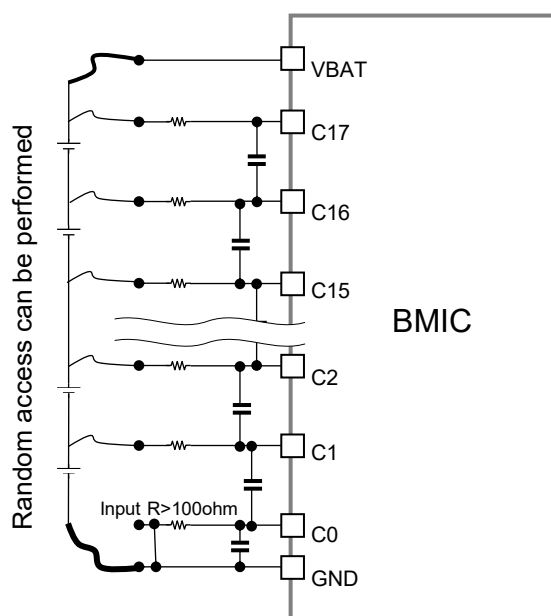


Fig. 5.2.1 Input Resistor bigger than 100ohm

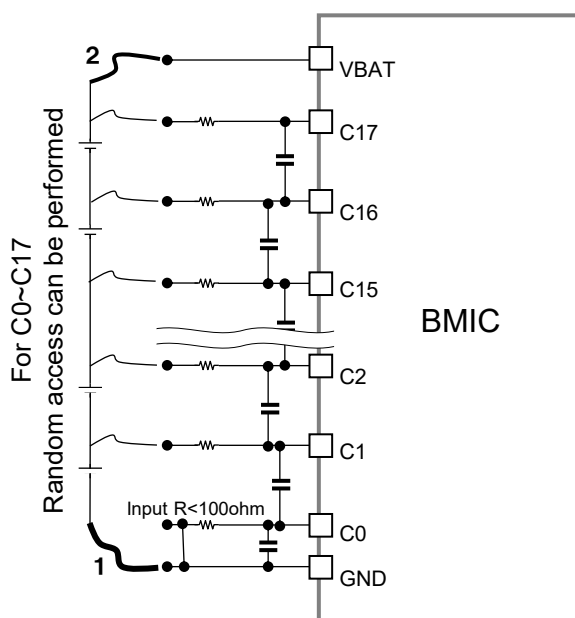


Fig. 5.2.2 Input Resistor smaller than 100ohm

Chapter 6 Low Side FET connection

KA49701A has built-in function to drive external Low-Side NMOS FET switches with some driver parts. The circuit consists of CHG pin with external driver parts, and DIS pin with external driver parts. An external regulator is needed to supply these driver circuit. Occasionally for some higher current application, CHG and DIS pins may control multiple parallel NMOS FETs with proper design verification. The control of DIS and CHG NMOS FETs are by setting register FDRV_CHG_FET (0x04[10]) and FDRV_DIS_FET (0x04[9]) respectively.

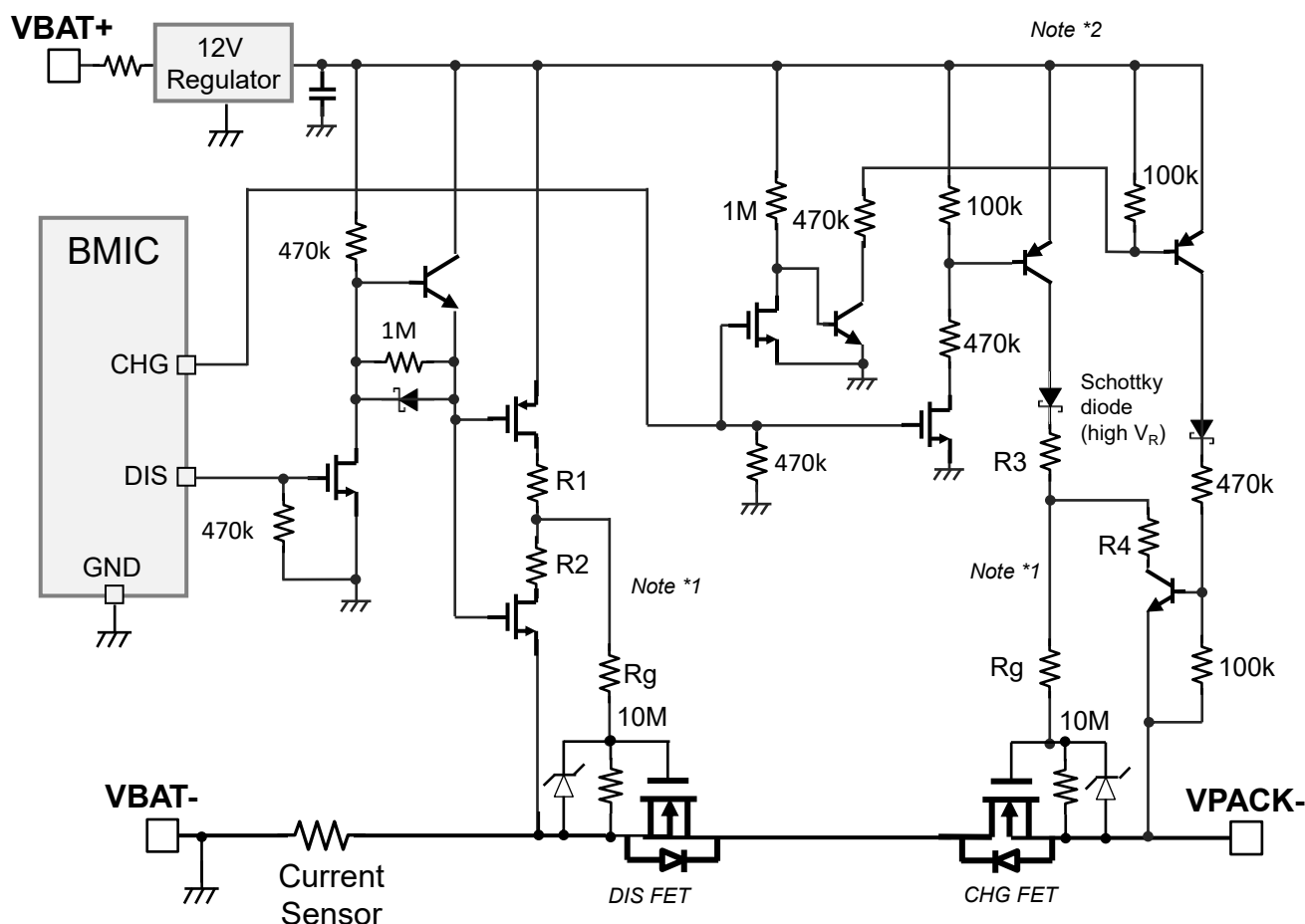


Fig. 6.0 Low-Side FET control circuit

Note :

*1 : The R1, R2, R3, R4 & Rg resistors are to be adjusted based on actual system power FET on/off testing. The common value maybe in tenths or hundreds of ohm.

*2 : More parts are needed for CHG FET driver because of VPACK- negative voltage occurrence during Charging.

Chapter 7 Watchdog Timer (WDT) setting during MCU firmware updating

Generally, REGEXT pin can be used as a power supply for external MCU, which generates a regulated 3.3V supply. As part of the communication safety features, BMIC has a Watchdog Timer (WDT) that will countdown to the set time when there is no communication from the MCU, it is possible to shutdown the MCU through shutting down the REGEXT supply. The WDT default time is 60s.

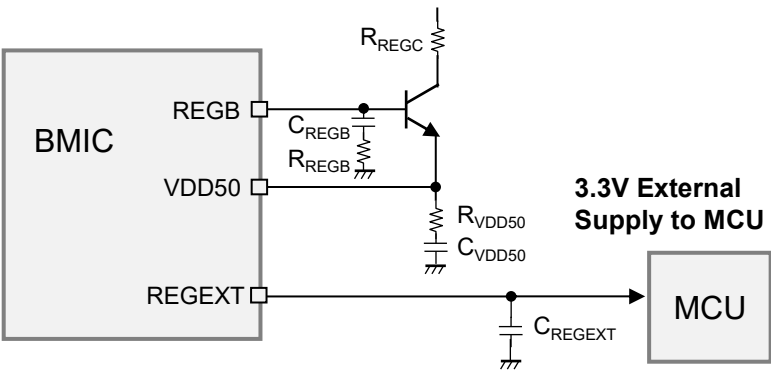


Fig. 7.1 REGEXT supply for MCU

For a particular special usage case, which is during firmware updating on MCU, there is no communication from MCU. This time period may exceed the default WDT. Hence, REGEXT supply will be shutting down and causing failure to the firmware updating process.

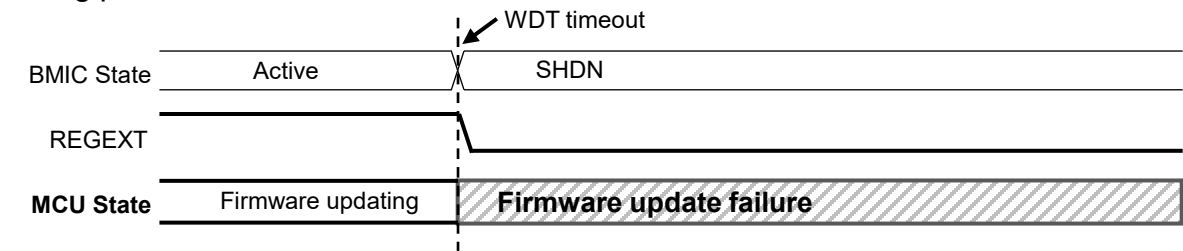


Fig. 7.2 MCU firmware update failure due to WDT timeout

In order to have sufficient time for MCU updating, turn Off WDT or set WDT with longer time before the MCU updating process. (Set register bit COMTIMON (0x03[12]) to “0” or set 1s~4096s for register SPI_WDTCOUNT[11:0] (0x03[11:0])). After MCU update is completed, turn back On WDT or set back WDT original time.

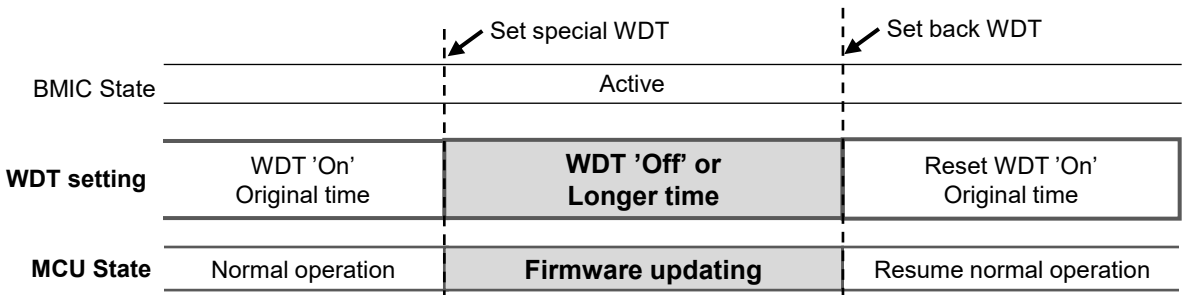
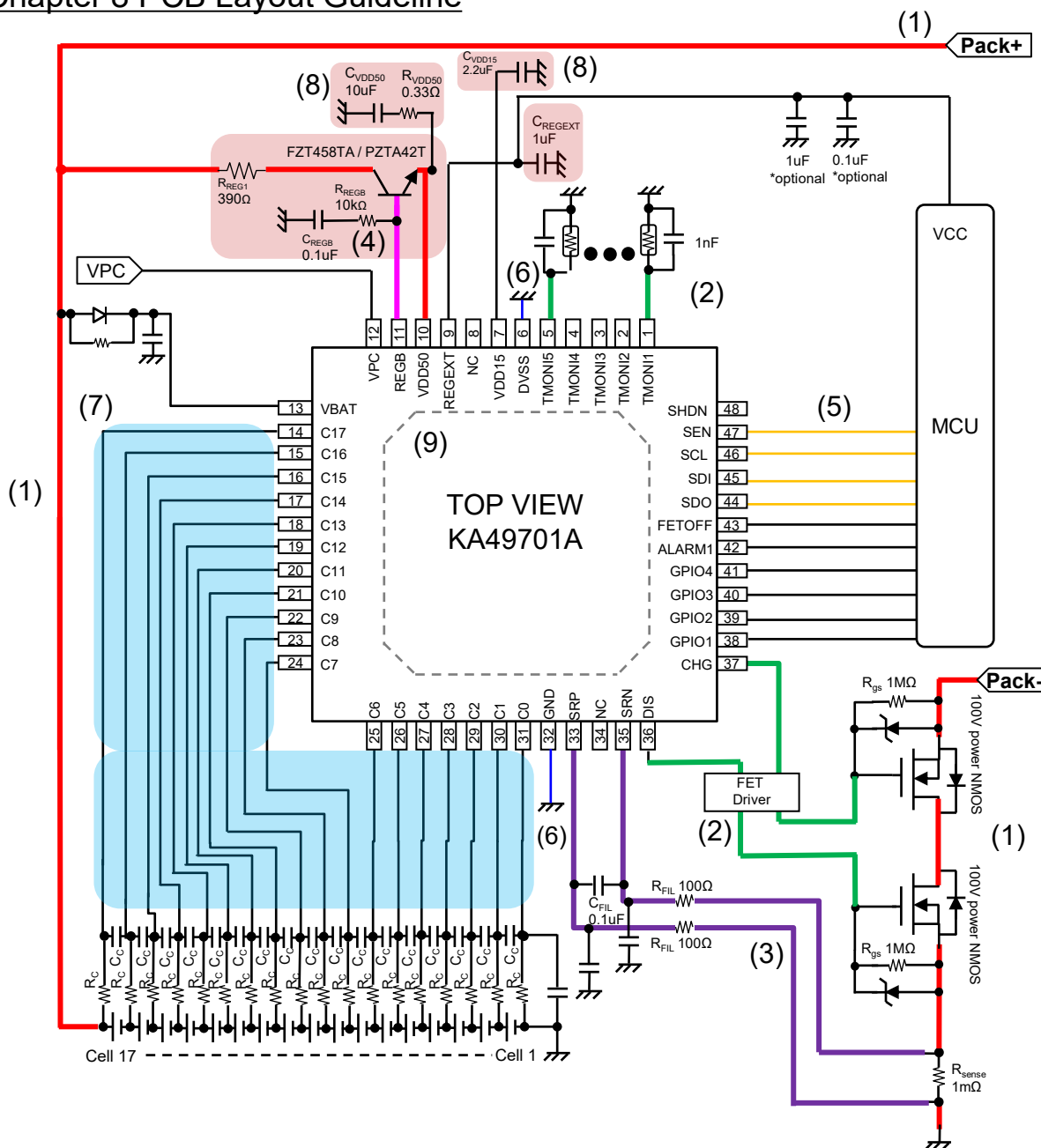


Fig. 7.3 WDT special setting during MCU firmware update

Chapter 8 PCB Layout Guideline



- (1) Wide line width to be drawn based on the desired Current.
- (2) Away from noisy signals lines.
- (3) Differential Pair routing which have to be as short as possible and closely identical.
Route both lines on same layer as RC filter. Avoid to be parallel with high current and noisy lines.
For 1 piece Rsense case: Connect both lines directly to the center inner part of Rsense pads.
For multiple Rsense case: All Rsense must be put near together. Connect both lines to the center of this group of Rsense. Evaluate the actual measured current value, adjust the lines connection location or firmware parameter in order to get accurate current reading.
- (4) Route lines as short as possible
- (5) Insert capacitor if necessary, at communication lines according to your noise test
Draw all the SPI lines as short as possible and with same length to avoid propagation.
Draw all the SPI lines side by side and within the same layer.
Keep noisy lines and high voltage switching lines away from SPI lines.
- (6) Connect all ground pins (DVSS, GND) together and routed use copper plane under the IC
- (7) Route these lines with the similar shape as much as possible since they are differential signals
- (8) Devices to be placed close to IC pin
- (9) User can choose to float the bottom heat pad or connect it to GND plane for best heat dissipation

Important Notice

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
Any applications other than the standard applications intended.
 - (1) Space appliance (such as artificial satellite, and rocket)
 - (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
 - (3) Medical equipment for life support
 - (4) Submarine transponder
 - (5) Control equipment for power plant
 - (6) Disaster prevention and security device
 - (7) Weapon
 - (8) Others : Applications of which reliability equivalent to (1) to (7) is required

Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins.
In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.

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Important Notice

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