LQFP-EP 216-Pin Package in MA35 Family MPUs

Application Note for 32-bit NuMicro® Family

Document Information

Abstract	This document introduces the LQFP-EP 216-pin package and its PCB layout guidelines and stencil design, as well as considerations during assembly and soldering.
Apply to	NuMicro® MA35D1/MA35H0/MA35D0 series

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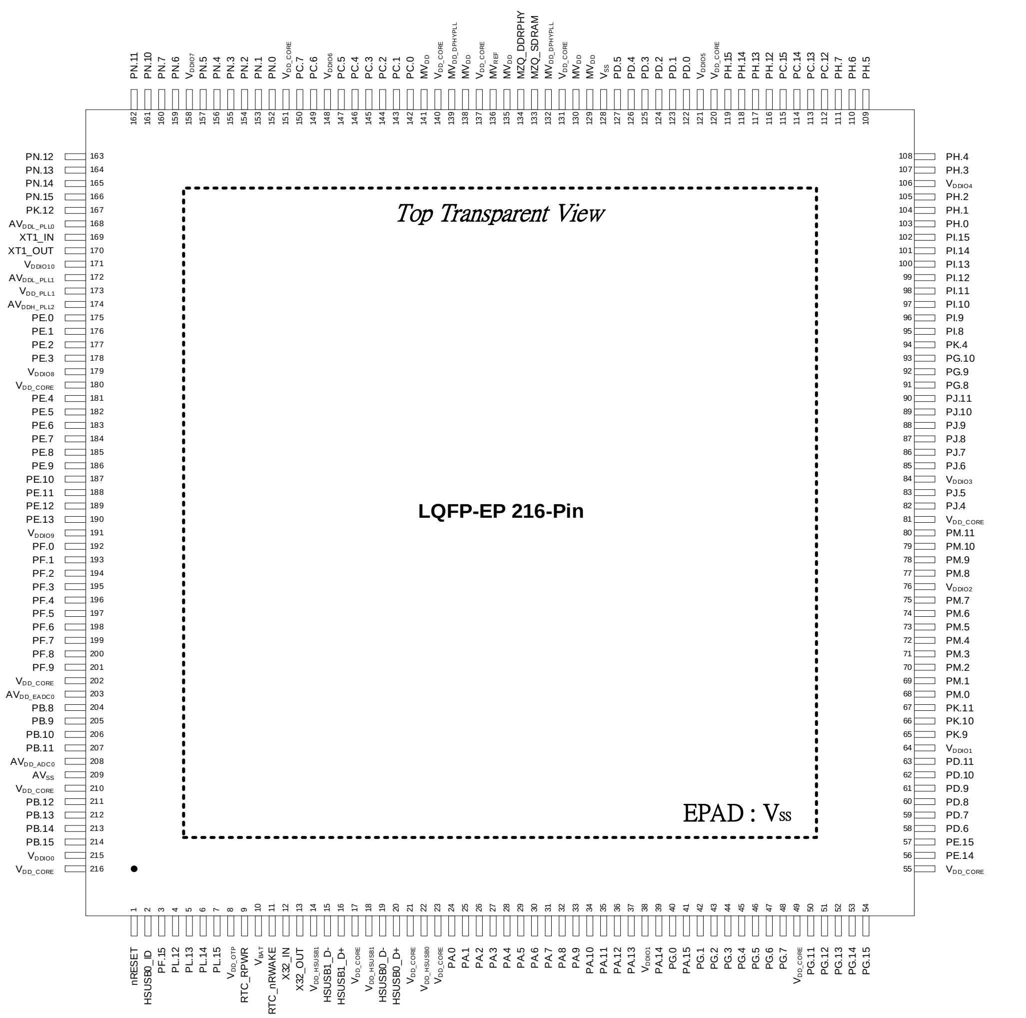
1 Overview

The NuMicro MA35D1/MA35H0/MA35D0 series microprocessors (MPUs) have the same Low Profile Quad Flat Package (LQFP) with an exposed die pad (EPAD) and is denoted with the suffix '-EP', called the LQFP-EP 216-Pin package. This LQFP-EP 216-Pin package is a special package that is slightly different from the ordinary LQFP 216-Pin package due to the EPAD on the bottom side of IC chip. There are two main purposes of the EPAD, one is for the heat radiation from the power dissipation of chip, and the other is for the ground connection between IC chip and Printed Circuit Board (PCB). For the normal operation of IC chip, it is crucial to make sure the EPAD on the bottom of LQFP-EP 216-Pin package is tightly soldered to the ground of the PCB.

1.1 LQFP-EP 216-Pin Package Pinout

Figure 1.1-1 shows the NuMicro MA35D1 series LQFP-EP 216-Pin pinout diagram that is the same shown in the related Datasheet (DS) and Technical Reference Manual (TRM).



Note: When soldering SMD, please make sure the EPAD on the bottom of LQFP-EP 216-Pin package is tightly soldered to the ground of the PCB.

Figure 1.1-1 NuMicro MA35D1 Series LQFP-EP 216-Pin Pinout Diagram

1.2 LQFP-EP 216-Pin Package Structure

Standard LQFP packages have mold compound which encompasses the entire bottom side of the package, while the EPAD design exposes the die pad, which increases thermal radiation performance. Figure 1.2-1 shows the cross-section drawing and the structure of LQFP-EP 216-Pin package. In the MA35D1/MA35H0/MA35D0 series, almost all the ground pads of IC die are wire bonded to the EPAD inside the LQFP-EP 216-Pin package. It is special important for the ground connection through the EPAD of package with the ground planes of PCB.

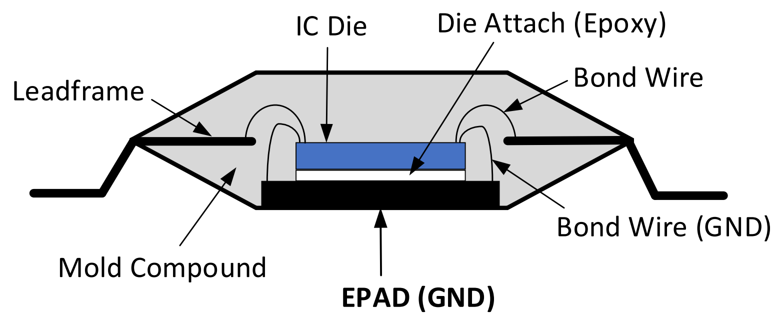
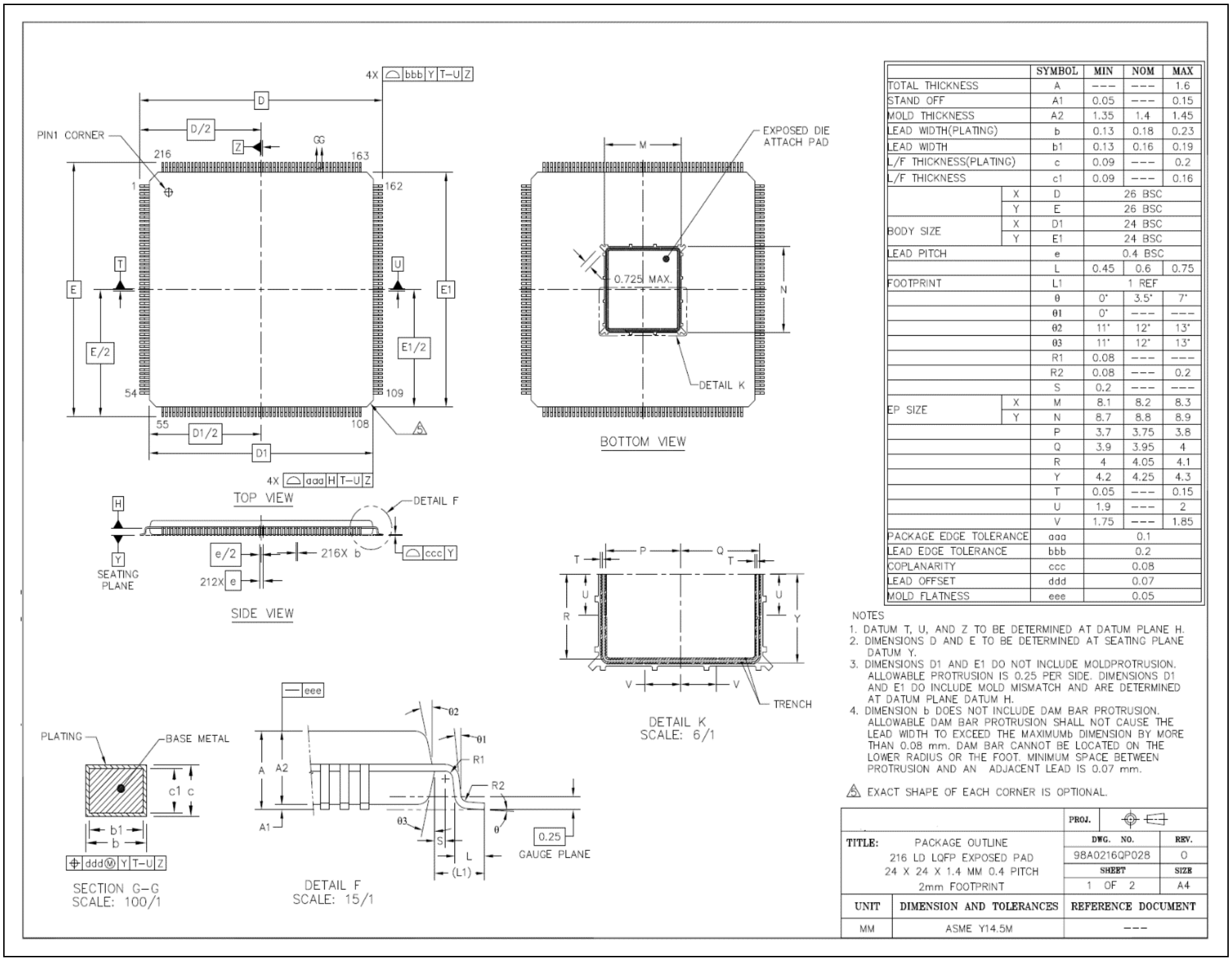


Figure 1.2-1 Cross-section of LQFP-EP 216-Pin with an EPAD

2 LQFP-EP 216-Pin Package

2.1 LQFP-EP 216-Pin Package Dimensions

Figure 2.1-1 shows the LQFP-EP 216-Pin package dimension copied from the related Datasheet.



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	26 BSC		
	Y	E	26 BSC		
BODY SIZE	X	D1	24 BSC		
	Y	E1	24 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	8.1	8.2	8.3
	Y	N	8.7	8.8	8.9
		P	3.7	3.75	3.8
		Q	3.9	3.95	4
		R	4	4.05	4.1
		Y	4.2	4.25	4.3
		T	0.05	---	0.15
		U	1.9	---	2
		V	1.75	---	1.85
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

Figure 2.1-1 LQFP-EP 216-Pin Package Dimension

2.2 LQFP-EP 216-Pin Actual Chip

Figure 2.2-1 shows the top and bottom view of LQFP-EP 216-Pin actual chip. The center of chip bottom side is an EPAD.

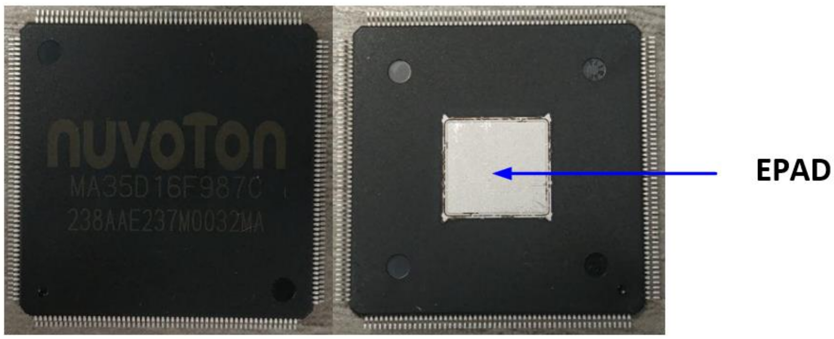


Figure 2.2-1 Top and Bottom View of LQFP-EP 216-Pin Actual Chip

3 PCB Layout Guidelines for LQFP-EP 216-Pin Package

3.1 PCB Pads for LQFP-EP 216-Pin Package

Figure 3.1-1 shows the PCB terminal pads and thermal pad for LQFP-EP 216-Pin package on the PCB layout.

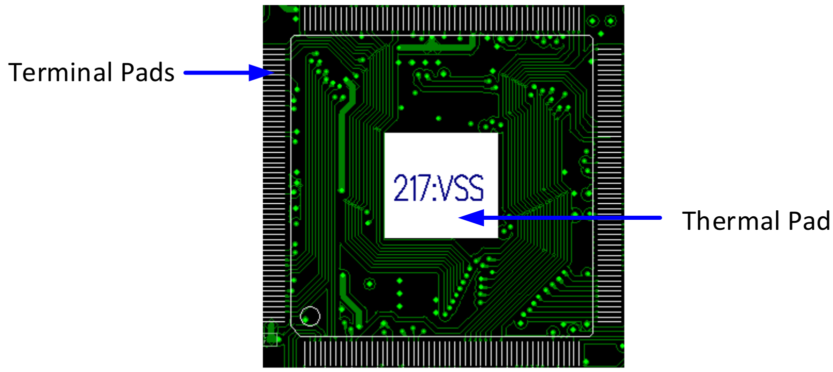


Figure 3.1-1 PCB Terminal Pads and Thermal Pad of LQFP-EP 216-Pin Package

3.2 Terminal Pad

3.2.1 Terminal Pad Type

There are two basic types of land pad for the LQFP package: Non-Solder Mask Defined (NSMD) and Solder Mask Defined (SMD). Both types are acceptable for the LQFP package.

- NSMD pads have a solder mask opening which is larger than the metal pad.
- NSMD is recommended because the copper etch process has tighter control than the solder masking process. The reliability of solder joint was also improved.
- The clearance around the copper pad and solder mask is 1 to 3 mil.

Figure 3.2-1 shows the NSMD terminal pad.

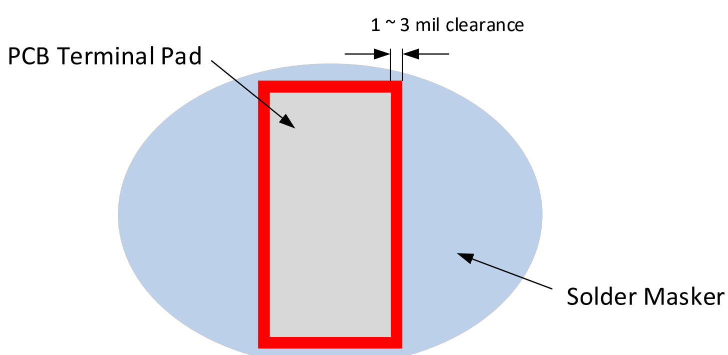


Figure 3.2-1 NSMD Terminal Pad

3.2.2 Terminal Pad Size

- An ideal solder joint is one that has equal cross-sectional areas at the terminal pad and the PCB interfaces.
  - Smaller pad is better for thermal fatigue reliability
  - Larger pad is better for bend or drop performance
- Package lead pad should be approximately centered on the PCB terminal pad with equal pad extension.
- The pad pattern dimension is most likely to be larger than the nominal lead dimension. It is recommended that using the nominal dimensions and extend the pad at least 0.5 mm on the outside and 0.5 mm on the inside, at least 0.01 to 0.02 mm on the left side and at least 0.01 to 0.02 mm on the right side.

Figure 3.2-2 shows the size of terminal pad.

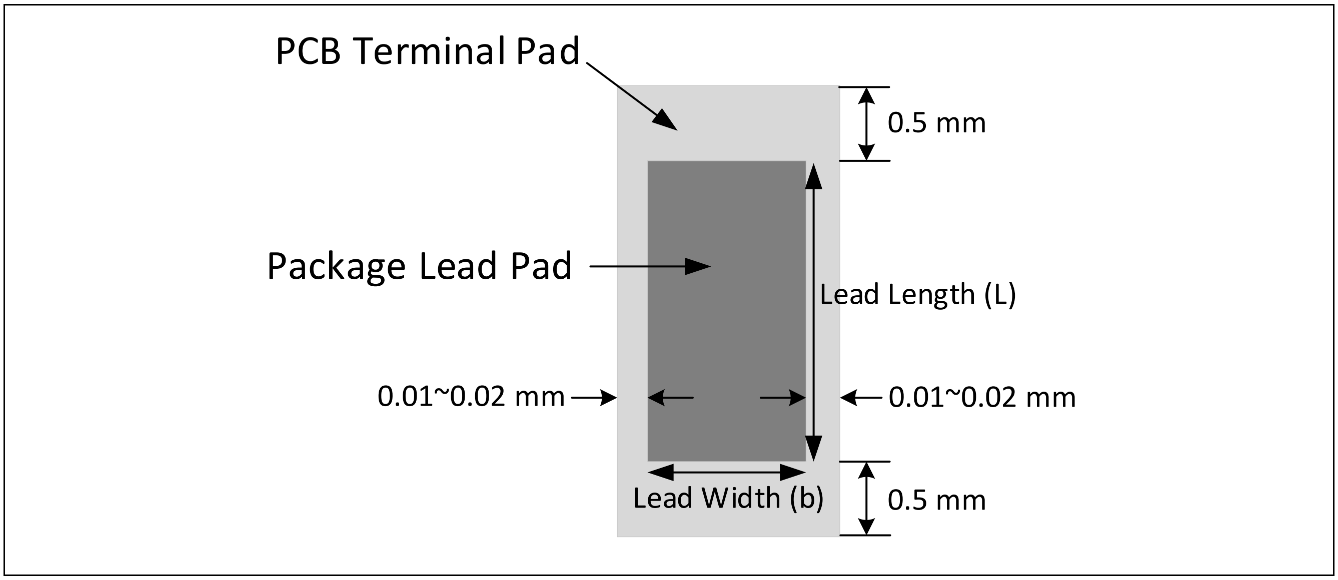


Figure 3.2-2 Size of Terminal Pad

3.3 Thermal Pad

3.3.1 Thermal Pad Land

Figure 3.3-1 shows the thermal pad land on the center of PCB footprint, and this thermal pad land also is a ground copper area for the PCB layout. This thermal pad land is not only for the heat sinking but also for the chip ground connection with the PCB ground planes (V_{SS}). The size of the thermal land should at least match the exposed die flag size (EPAD). But it is necessary to avoid solder bridge between thermal pad and the perimeter pads. It is recommended that the clearance between thermal pad and perimeter pads is 0.25 mm.

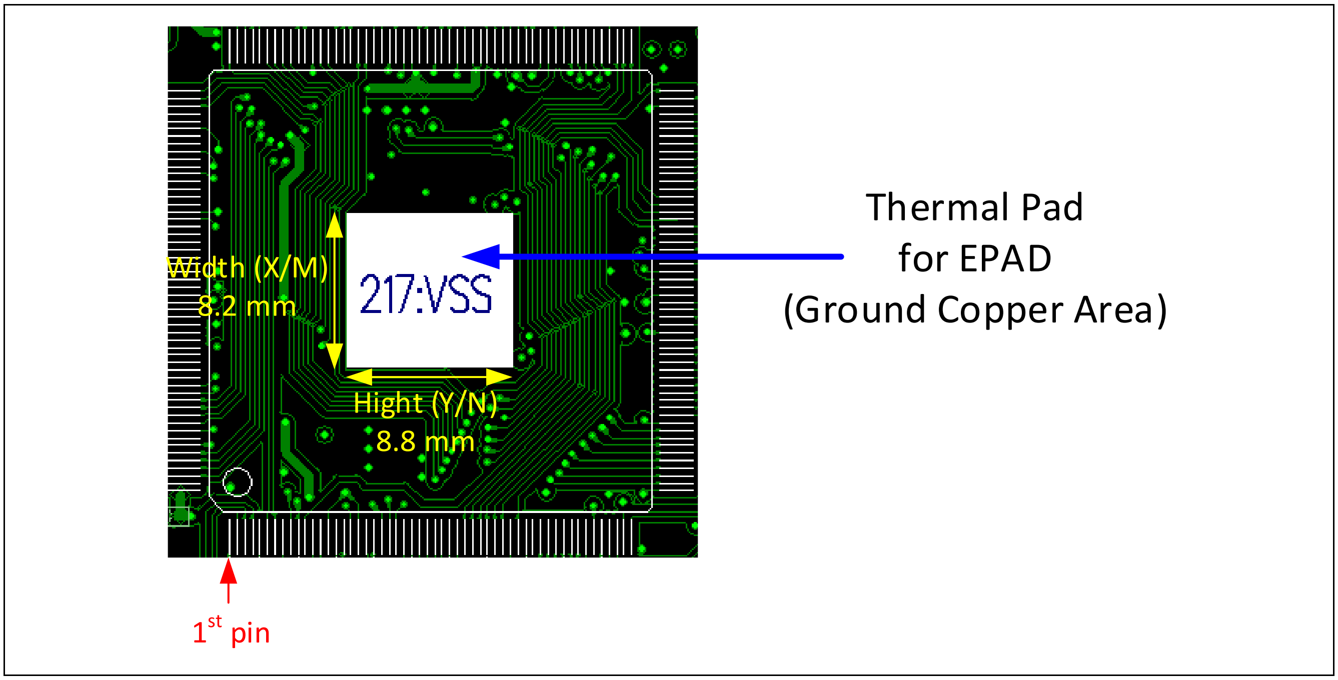


Figure 3.3-1 Thermal Pad Land

3.3.2 Thermal Pad Via

For the thermal pad via, the recommended via diameter is 0.3 to 0.33 mm or less with 1.0 oz. copper via barrel plating, and the recommended via spacing is 1 to 1.2 mm shown in Figure 3.3-2. The number of via depends on the application, but it is recommended as much as possible.

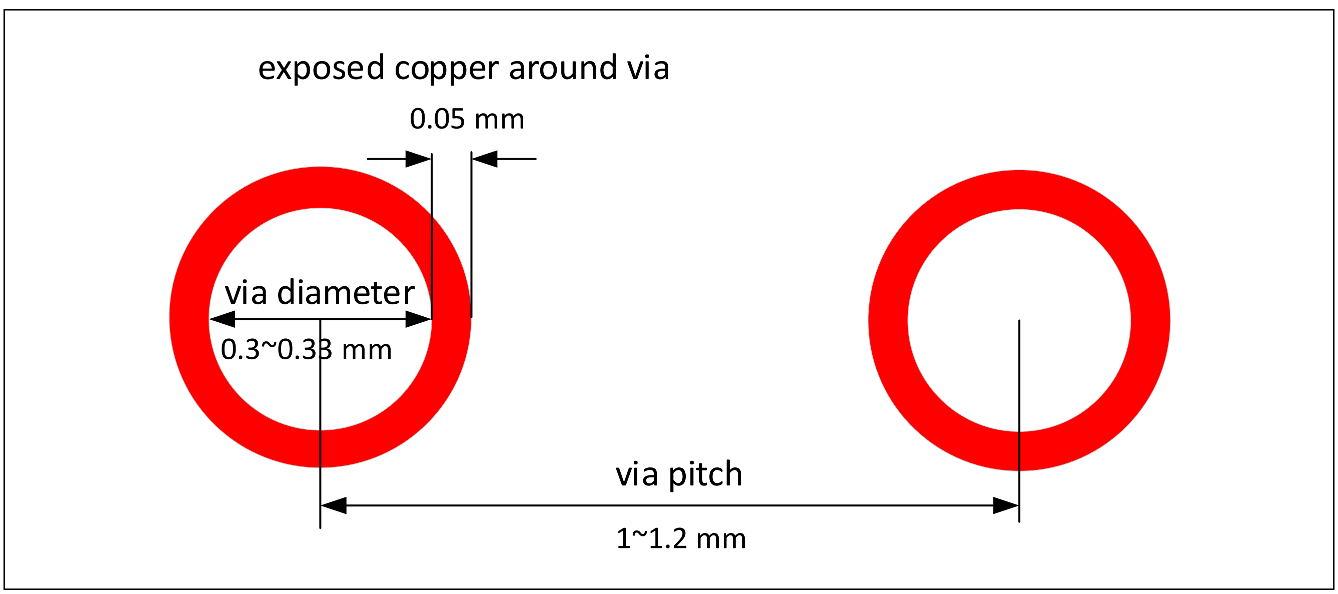


Figure 3.3-2 Recommended Solid Via

The maximum thermal and electrical performance is achieved when an array of vias is incorporated into the pattern of thermal pad land at 1.2 mm grid. Figure 3.3-3 shows the recommended thermal pad vias inside the thermal pad land for the EPAD of LQFP-EP 216-Pin package on PCB layout.

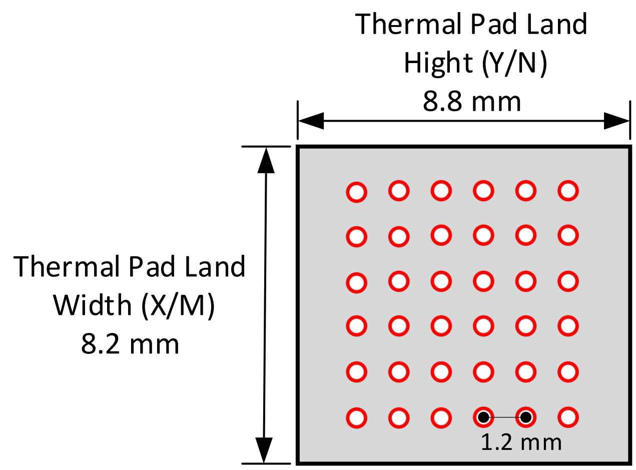


Figure 3.3-3 Recommended Thermal Vias for the EPAD of LQFP-EP 216-Pin Package

Figure 3.3-4 shows the actual thermal pad vias on the top-layer and bottom-layer of PCB layout. These vias are not only used to effectively transfer heat from the top copper layer of the PCB to the inner or bottom copper layers, but also used to connect with the inner and bottom-layer ground copper planes.

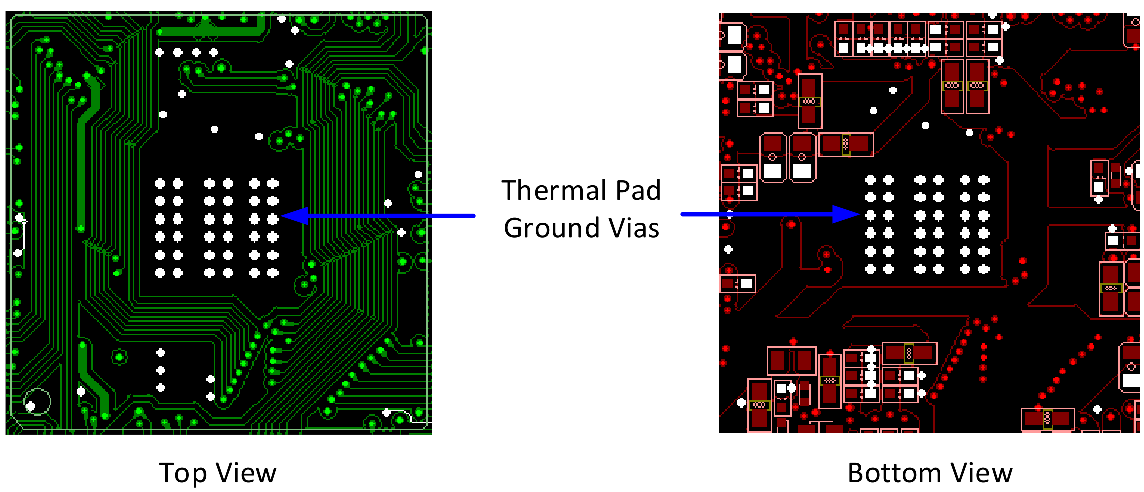


Figure 3.3-4 Actual Thermal Pad Vias on PCB Layout

3.4 Example of NG Layout for Thermal Pad

Figure 3.4-1 shows an example of an NG (not good) layout for the thermal pad. This PCB design has only two layers without any ground vias connected to another ground layer on the thermal pad land. The main problem is that the contact area between the thermal pad's ground and another larger ground plane is too narrow and small.

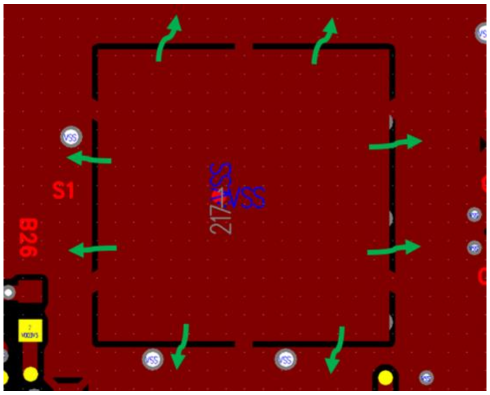


Figure 3.4-1 An Example of NG Layout for EPAD

4 SMT Assembly Considerations

4.1 Stencil Consideration

4.1.1 Stencil Type and Thickness

For stencil, the Laser for cutting and stainless steel is recommended. The lead pitch of LQFP-EP 216-Pin package as 0.4 mm and the thickness of stencil as 0.1 to 0.12 mm is recommended. Figure 4.3-1 shows lead width and lead pitch of LQFP-EP 216-Pin package.

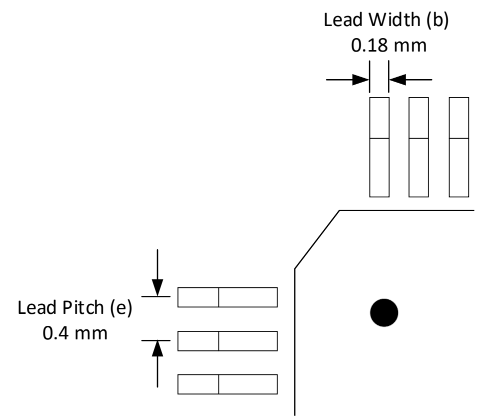


Figure 4.1-1 Lead Width and Lead Pitch of LQFP-EP 216-Pin Package

4.1.2 Aperture Size and Shape for Terminal Pad

- Aspect ratio (width / thickness) > 1.5
- Aperture shape
  - The edge is 0.25 to 0.45 mm inward compared to thermal pad design on the PCB.
  - Oval-shaped opening should be used to get the optimum paste release.
  - Rounded corners to minimize clogging
  - Positive taper walls (5˚ tapering) with bottom opening is larger than the top.

4.1.3 Aperture Design for Thermal Pad

- The small multiple openings should be used in steady of one big opening.
- The apertures should be kept away from thermal vias if possible.
- The minimum value of the distance between matrices must be greater than 0.4 mm.
- 50% to 80% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper with bottom opening is larger than the top.

Figure 4.3-1 shows the examples of aperture design for the thermal pad land.

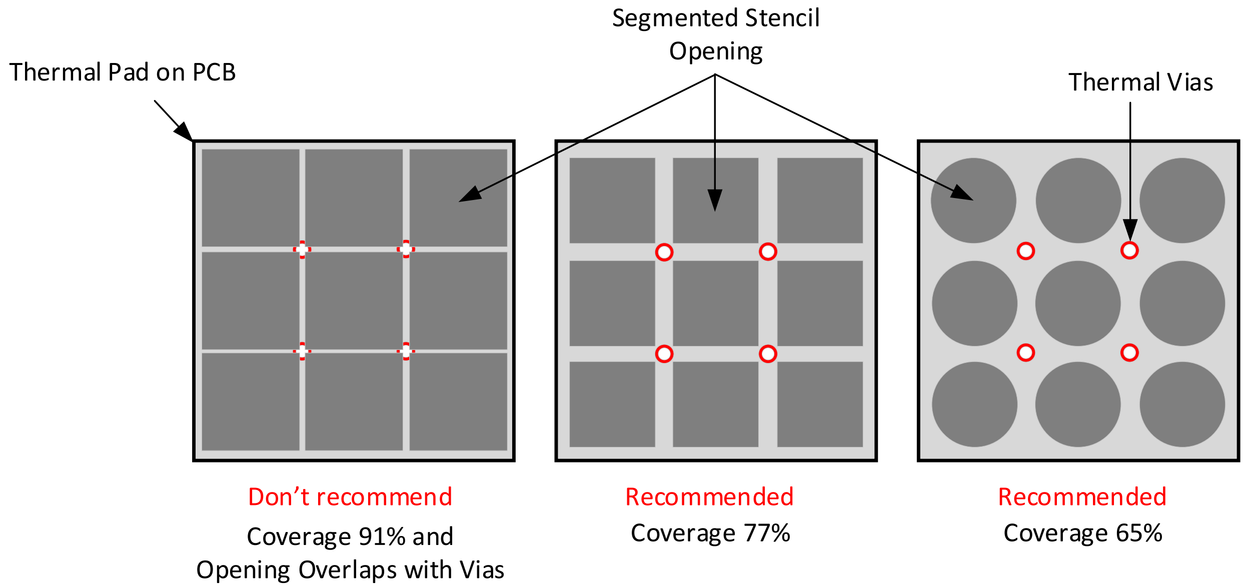


Figure 4.1-2 Examples of Aperture Design for Thermal Pad Land

4.1.4 Actual Stencil Picture

Figure 4.1-3 shows the actual aperture design of stencil for the terminal pads and the thermal pad of the PCB. The thickness of stencil is 0.1 mm, the opening is 1mm x 1mm, the area for solder paste is 43.5% and the whole solder paste coverage is around 56.5% to 58.5%.

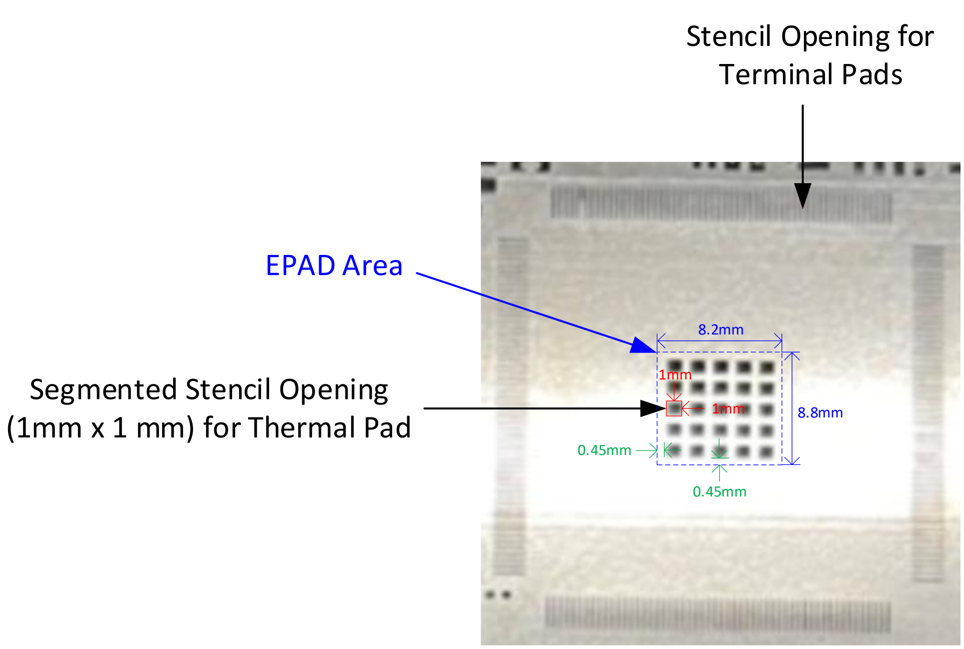


Figure 4.1-3 Actual Aperture Design of Stencil for Terminal Pads and Thermal Pad

4.2 Solder Paste Considerations

Solder paste consists of solder alloy and a flux system. Typically, the volume is split into about 50% alloy and 50% flux and solvents. The following items are recommended.

- Alloys: 63Sn/37Pb or 62Sn/36Pb/2Ag
  - Sn/Ag/Cu family for lead-free application
- No Clean flux
- Particle size: Type IV is preferred to improved printing performance.

4.3 Profile Setting Consideration

4.3.1 Reflow Profile

Figure 4.3-1 shows the PCB reflow profile diagram and Table 4.3-1 lists the PCB reflow profile parameters.

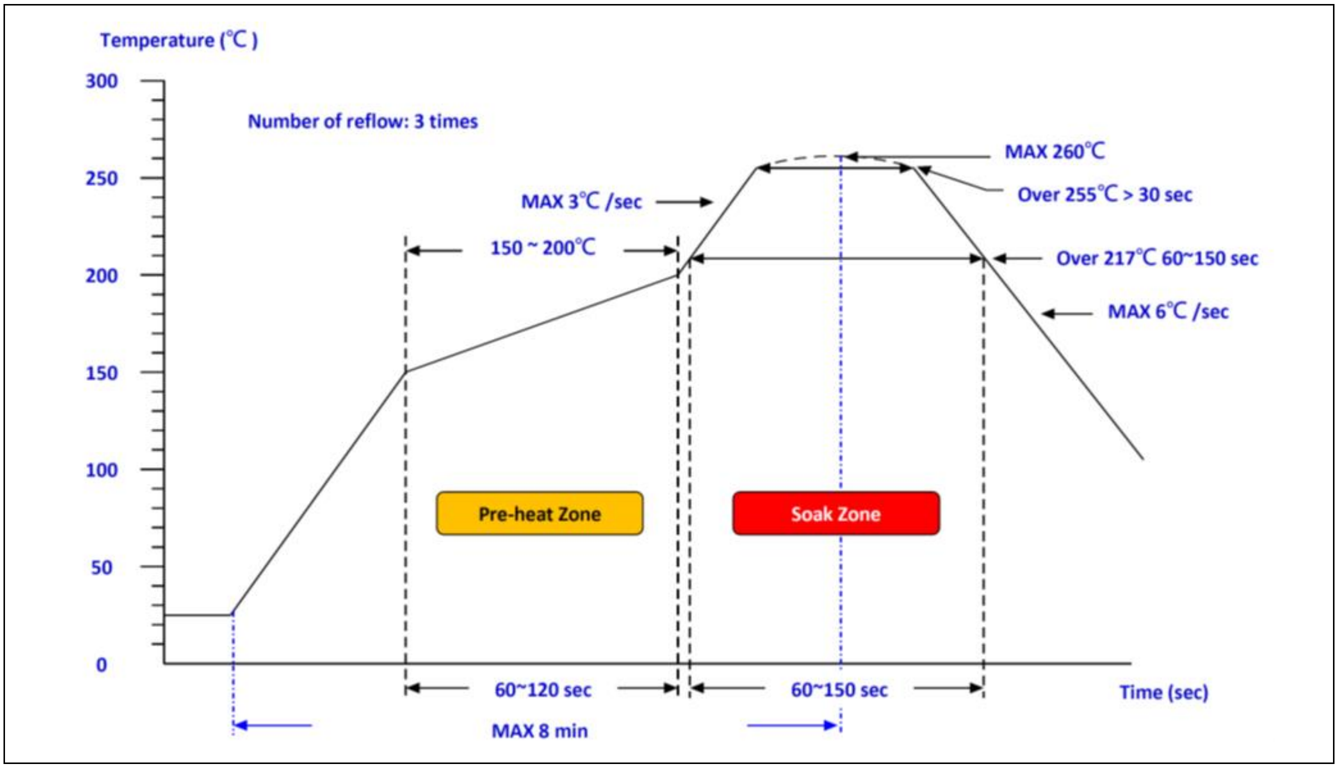


Figure 4.3-1 PCB Reflow Profile Diagram

Profile Feature	Sn-Pb Eutestic Assembly		Pb-Free Eutestic Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	< 3°C/second		< 3°C/second	
Preheat • Temperature Min (Ts_{min}) • Temperature Max (Ts_{max})	100°C 150°C 60-120 seconds		150°C 200°C 60-120 seconds	

• Time (min to max) (ts)		
Time maintained above: • Temperature (T_L) • Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature (T_p)	225+0/-5°C	245+5/-5°C
Time within 5°C of actual Peak Temperature (t_p)	10-20 seconds	10-30 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.
Note: 1. All temperatures refer to topside of the package, measured on the package body surface. 2. Depends on other parts on board density and follower solder paste manufacturer's guideline.		

Table 4.3-1 PCB Reflow Profile Parameters

4.3.2 Actual Reflow Profile Curve

Figure 4.3-2 shows the actual reflow profile curve during PCBA assembly process after KIC intelligent temperature measurement and computer-assisted fine-tuning. Before PCBA assembly mass production and during the first PCBA trial running process, please confirm with the SMT factory engineers about whether the temperature sensor is close to the main MPU chip and that the temperature and time are within the specifications shown in Figure 4.3-1 and Table 4.3-1. If the temperature and time are not met the specifications of reflow, it needs to be fine-tuned and follows the experience of SMT factory engineers.

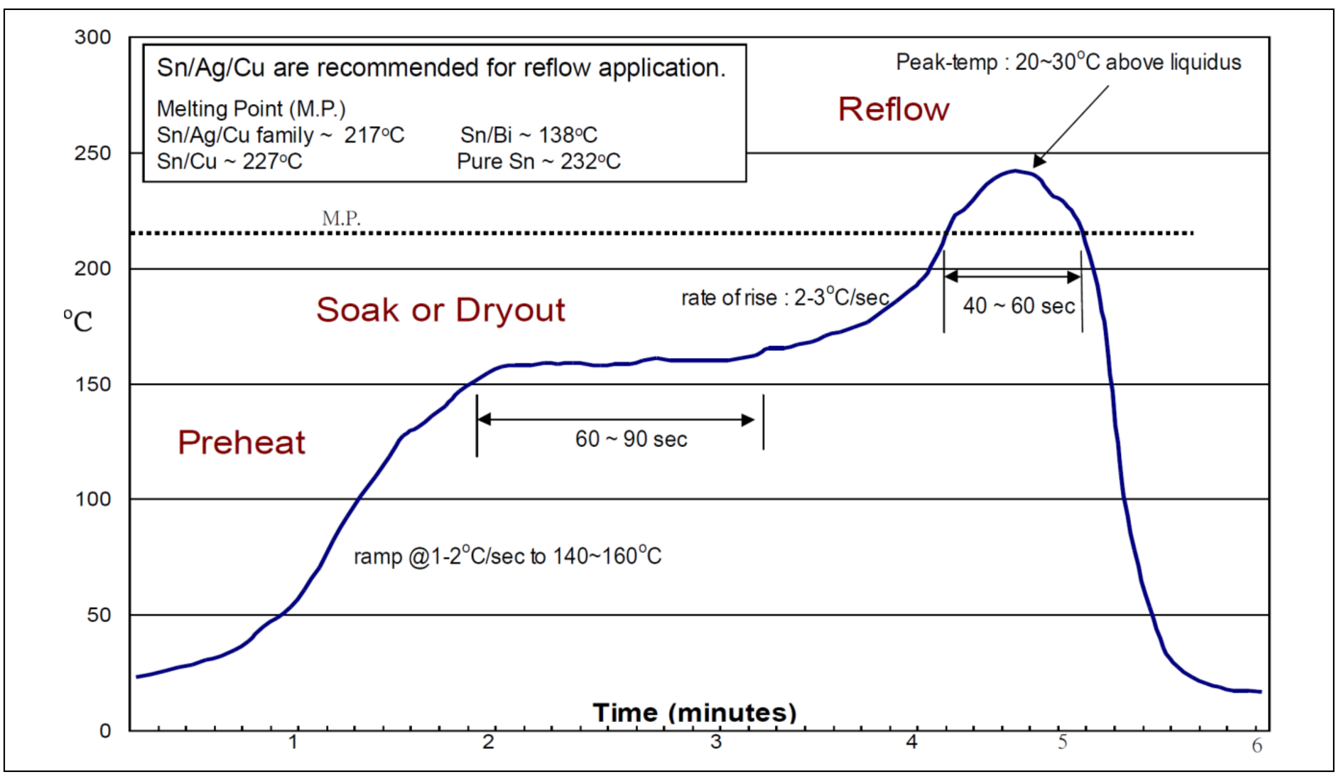


Figure 4.3-2 Actual Reflow Profile Curve

4.3.3 PCB Assembly Considerations

This profile is designed for use with 96.5Sn/3Ag/0.5Cu and can serve as a general guideline in establishing a reflow profile.

Reflow Profile:

- Heat-up@1~3°C/sec to 140°C
- Preheat@140°C -150°C for 120 - 160 sec
- Ramp@2~3°C/sec to peak temperature (220°C - 225°C), temperature over 183°C for 45 to 75 sec
- Cool down to room temperature@4~2°C/sec to avoid undesired intermetallic compound layer.

4.4 Actual Mounted Picture of LQFP-EP 216-Pin Package

Figure 4.4-1 shows the X-ray picture after LQFP-EP 216-Pin package is mounted on the PCB from the assembly factory.

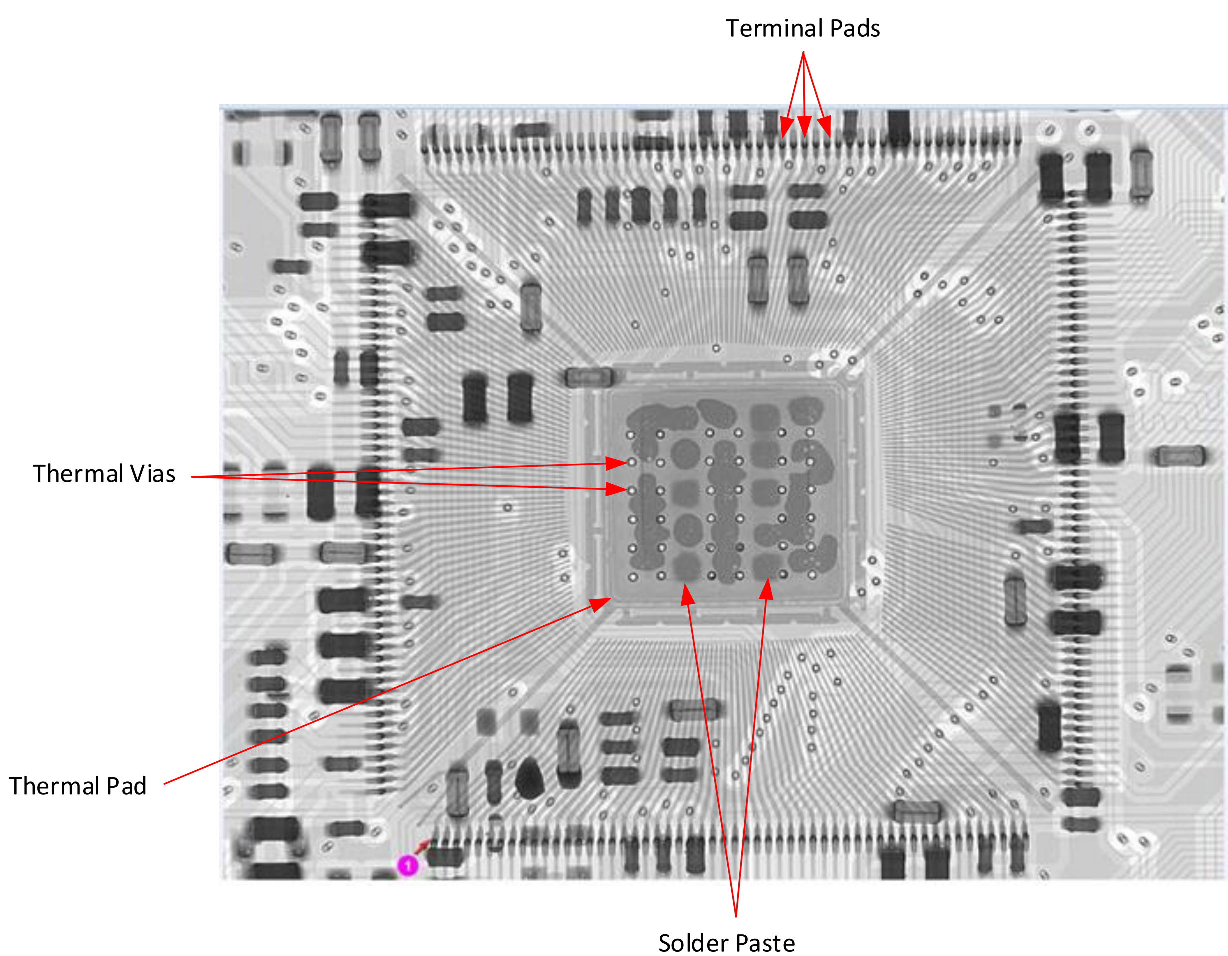


Figure 4.4-1 X-ray Picture of LQFP-EP 216-Pin Mounted on PCB

4.5 Larger PCB

When a PCB is used for a special application and the area is too large (e.g. an area larger than 30cm x 30cm), the following items require special consideration. Please consult the SMT factory about these items to ensure that the LQFP-EP 216-pin packaged EPAD is soldered tightly to a large PCB.

- Thickness of PCB. (stress)
- Thickness of steel plate. (solder paste volume)
- Is the PCB damp? (baking)
- Whether the IC is oxidized by moisture? (cleaning and baking)
- Composition of solder paste. (leaded or lead-free)
- Temperature of the reflow furnace.

5 Conclusion

To achieve the MA35D1/MA35H0/MA35D0 series packaged in LQFP-EP 216-Pin type that can operate normally in the application system, it is very important to make sure all the terminal pads and the thermal pad (EPAD) of the LQFP-EP 216-Pin package are tightly soldered to the ground planes of the PCB.

When testing the PCBA, you may find that the program sometimes operates unstably or out of control, and suspect that the EPAD soldering is incomplete. Is there any way to quickly confirm whether the EPAD is soldered incorrectly or incompletely with the thermal pad of PCB? You can try the following two methods.

- Increase program complexity, such as heavier HMI program load.
- Slightly increase the voltage of the VDD_CORE power supply, but do not exceed the maximum value 1.31V of the VDD_CORE specification as defined in the *MA35D1/MA35H0/MA35D0 series Datasheet*. The higher voltage of VDD_CORE, the higher the probability of the same issue occurs.

Revision History

Date	Revision	Description
2024.12.16	1.00	• Initial version.
2025.03.12	1.01	• Updated the sections 4.1.2, 4.1.3, 4.1.4, 4.3.2 and chapter 5. • Added the sections 3.4 and 4.5.

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