

Single N-channel MOSFET

FK4B01100L Datasheet

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1. GENERAL DESCRIPTION

Single N-channel MOSFET
for load switching circuits.

2. FEATURES

- Low Drain-source ON Resistance: $R_{DS(on)}$ typ = 27 m Ω (V_{GS} = 2.5 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1)

3. MARKING SYMBOL: 1A

4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

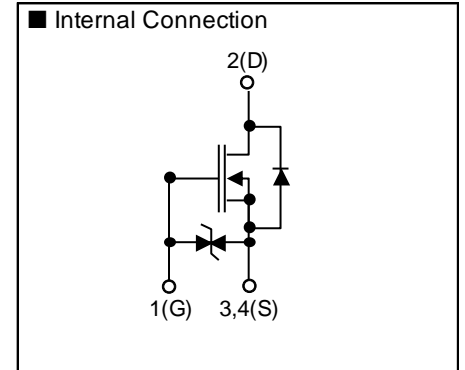
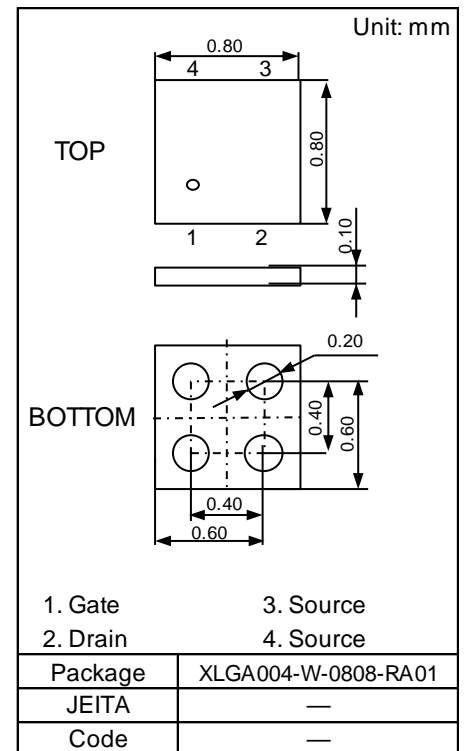
Parameter	Symbol	Rating	Unit
Drain-Source Voltage	VDS	12	V
Gate-Source Voltage	VGS	± 8	V
Drain Current	ID1 ^{*1}	3.4	A
	ID2 ^{*2}	5.2	
	ID3 ^{*3}	6.5	
Peak Drain Current	IDp1 ^{*1*4}	27	A
	IDp2 ^{*2*4}	41	
	IDp3 ^{*3*4}	52	
Power Dissipation	PD1 ^{*1}	0.36	W
	PD2 ^{*2}	0.82	
	PD3 ^{*3}	1.30	
Channel Temperature	Tch	150	$^\circ\text{C}$
Operating Ambient Temperature	Topr	-40 to +85	$^\circ\text{C}$
Storage Temperature	Tstg	-55 to +150	$^\circ\text{C}$

Note *1 FR4 board (25.4mm \times 25.4mm \times t1.0mm)、Min Cu 36mm² Copper.

*2 FR4 board (25.4mm \times 25.4mm \times t1.0mm)、Full Cu.

*3 Ceramic substrate (70mm \times 70mm \times t1.0mm).

*4 $t = 10 \mu\text{s}$, Duty Cycle < 1 %.



6. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Drain Current	IDSS	VDS = 12 V, VGS = 0 V			10	μA
Gate-Source Leakage Current	IGSS	VGS = ± 8 V, VDS = 0 V			± 10	μA
Gate Threshold Voltage	Vth	ID = 236 μA , VDS = 10 V	0.3		1.0	V
Drain-Source ON Resistance	RDS(on)	ID = 1.5 A, VGS = 4.5 V		22	30	m Ω
		ID = 1.0 A, VGS = 2.5 V		27	40	
		ID = 0.5 A, VGS = 1.8 V		33	56	
		ID = 0.25 A, VGS = 1.5 V		43	99	
Input Capacitance *1	Ciss	VDS = 10 V VGS = 0 V f = 1MHz		275		pF
Output Capacitance *1	Coss			100		
Reverse Transfer Capacitance *1	Crss			70		
Turn-on Delay Time *1,*2	td(on)	VDD = 6 V VGS = 0 to 4.5 V ID = 1.0 A		7		ns
Rise Time *1,*2	tr			14		
Turn-off Delay Time *1,*2	td(off)			165		
Fall Time *1,*2	tf			76		
Total Gate Charge *1	Qg	VDD = 6 V VGS = 4.5 V IS = 1.0 A		5.8		nC
Gate to Source Charge *1	Qgs			0.75		
Gate to Drain Miller Charge *1	Qgd			0.95		
Body Diode Forward Voltage	VF(D-S)	IF = 0.2A, VGS = 0V		0.6	1.2	V

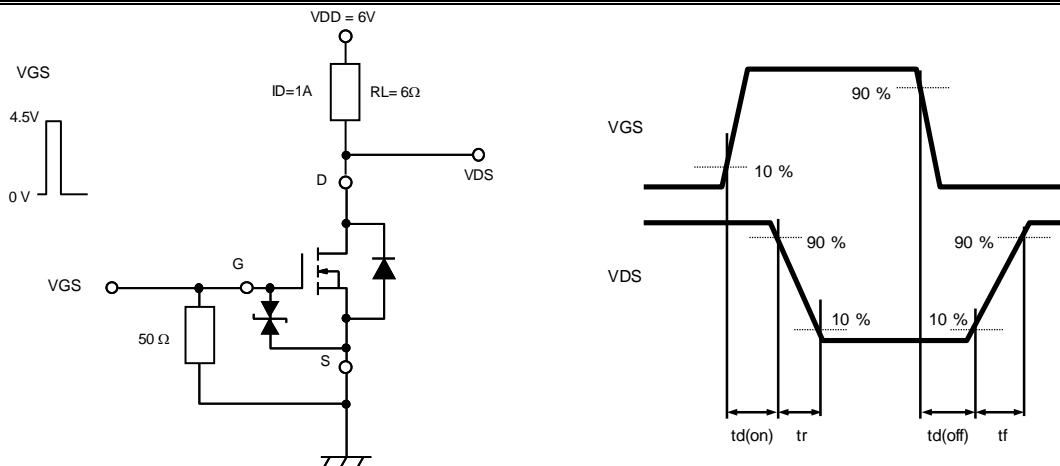
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

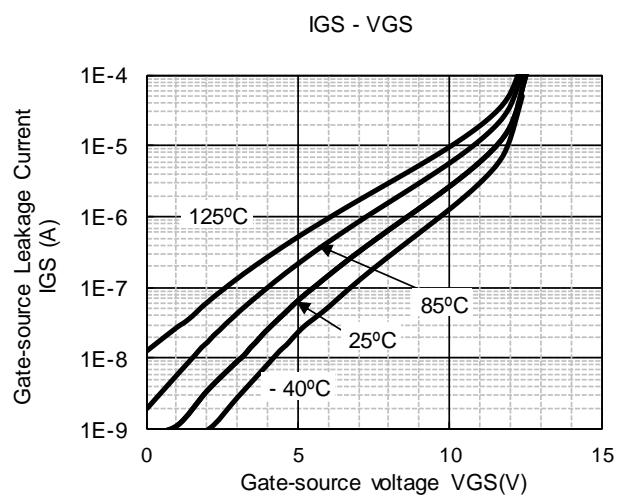
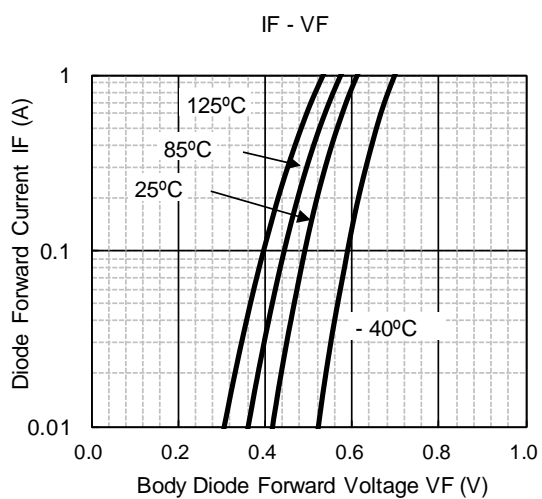
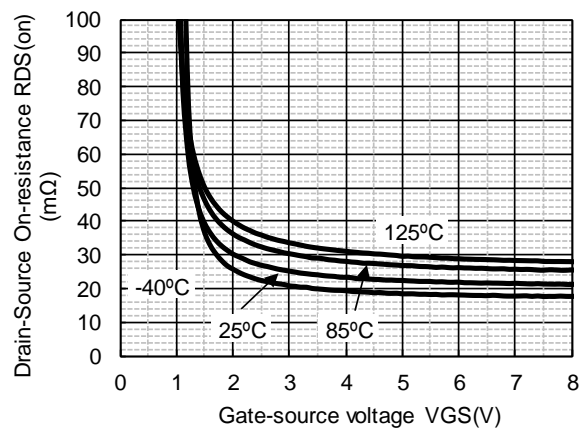
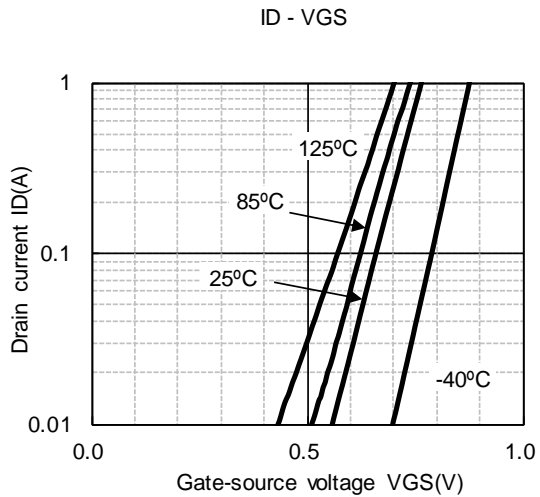
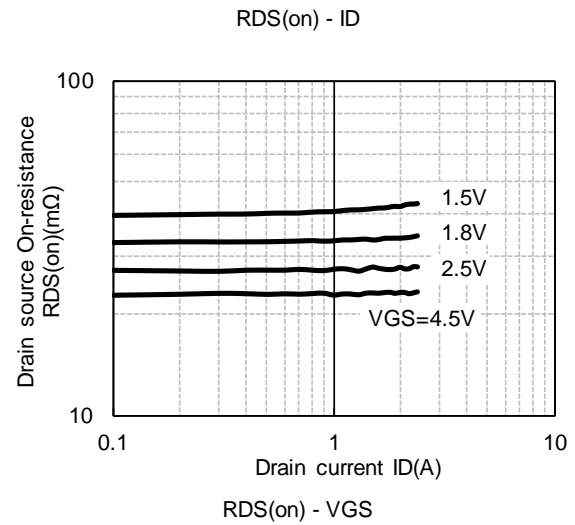
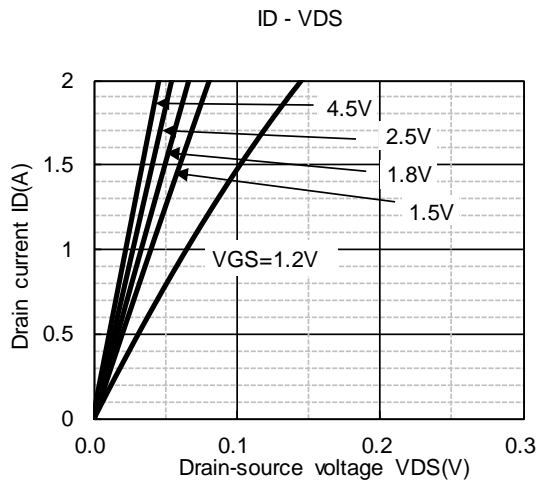
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

7. ELECTRICAL STATE DISCHARGE CHARACTERISTICS

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human body model	HBM	C = 100 pF, R = 1.5 k Ω	H1C	> 1k to \leq 2k	V
	Machine model	MM	C = 200 pF, R = 0 Ω	M2	> 100 to \leq 200	V

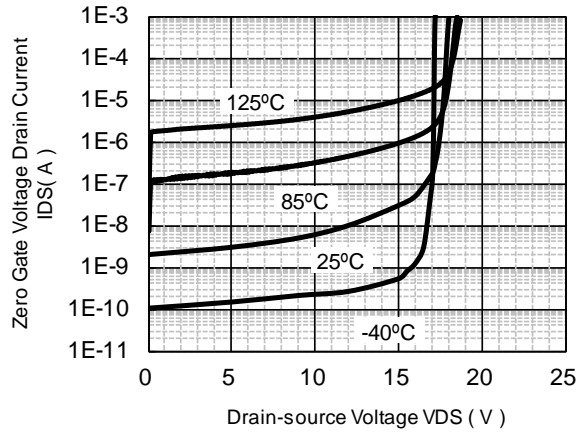


8. TECHNICAL DATA (Reference)

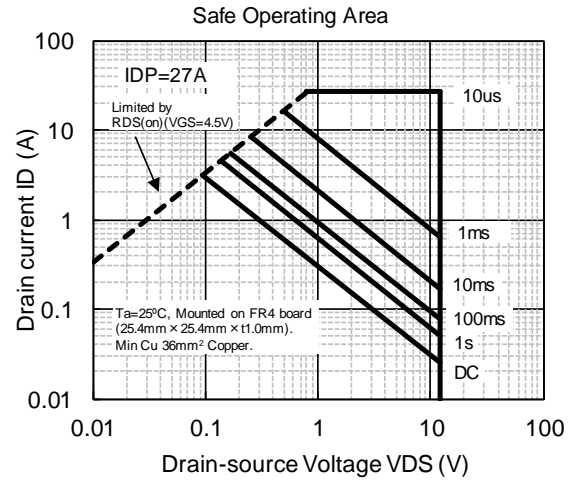
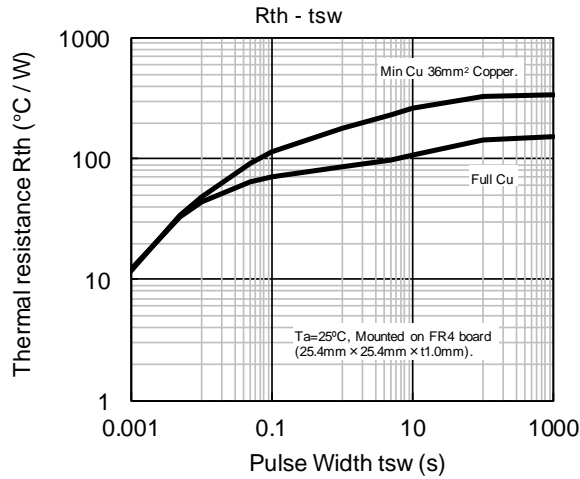
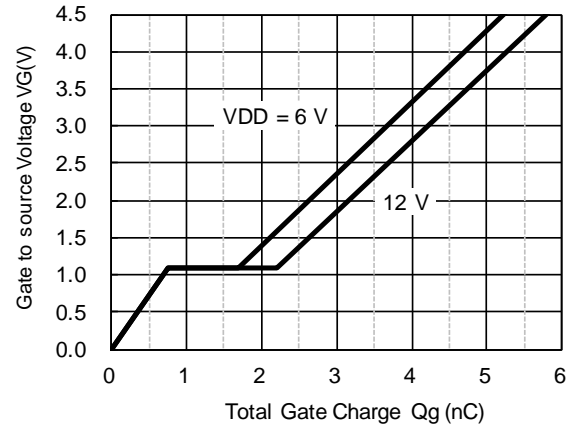


TECHNICAL DATA (Reference)

IDS - VDS

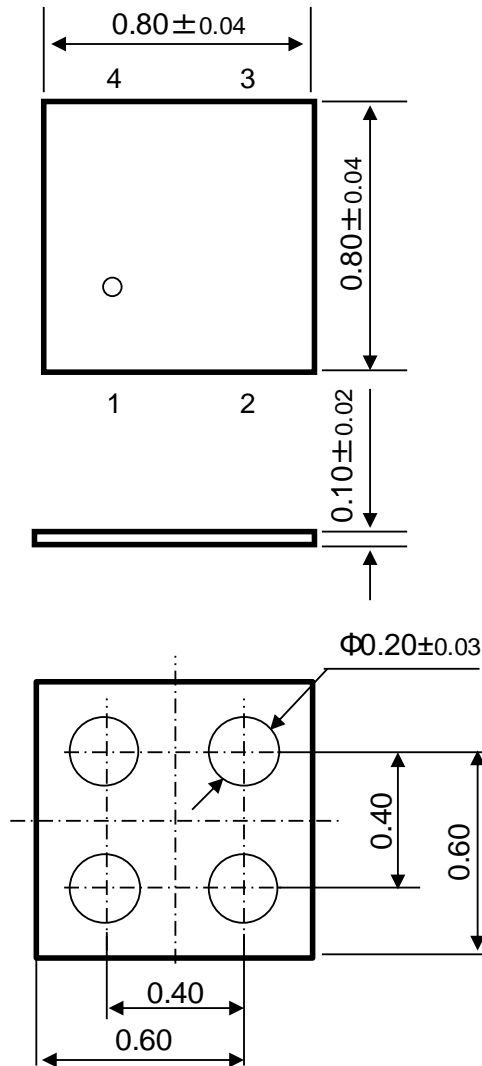


Dynamic Input/Output Characteristics



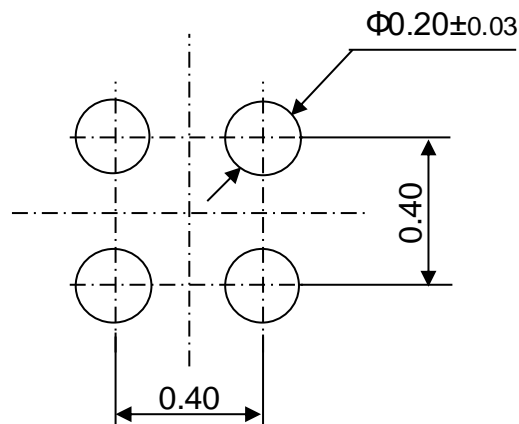
9. OUTLINE

Unit: mm



10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.02.05	1.00	1. Initially issued.
2021.08.31	1.01	1. Added important notice in Land Pattern. 2. Added special attention and precautions notes.
2021.11.11	1.02	1. Changed document name from Product Standards to Datasheet.

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