Single N-channel

MOSFET

FK4B01110L
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.

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1. GENERAL DESCRIPTION

Single N-channel MOSFET
for load swiching circuits.

2. FEATURES

- Low Drain-source ON Resistance: RDS(on) typ = 57 mΩ (VGS = 2.5 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1)

3. MARKING SYMBOL: 1B

4. PACKAGING

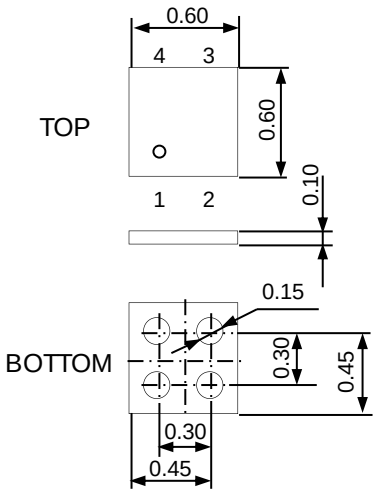
Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	VDS	12	V
Gate-Source Voltage	VGS	±8	V
Drain Current	ID1*1	2.3	A
	ID2*2	3.4	
	ID3*3	4.1	
Peak Drain Current	IDp1*1*4	18	A
	IDp2*2*4	27	
	IDp3*3*4	32	
Power Dissipation	PD1*1	0.34	W
	PD2*2	0.76	
	PD3*3	1.10	
Channel Temperature	Tch	150	°C
Operating Ambient Temperature	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Note *1 FR4 board (25.4 mm x 25.4 mm x t1.0 mm), Min Cu 36mm^2 Copper.
*2 FR4 board (25.4 mm x 25.4 mm x t1.0 mm), Full Cu.
*3 Ceramic substrate (70 mm x 70 mm x t1.0 mm).
*4 t = 10 μs, Duty Cycle ≤ 1 %.

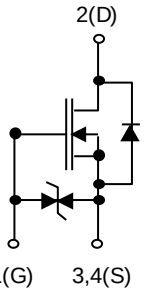
Unit: mm



1. Gate 3. Source
2. Drain 4. Source

Package	ALGA004-W-0606-RA01
JEITA	—
Code	—

■ Internal Connection

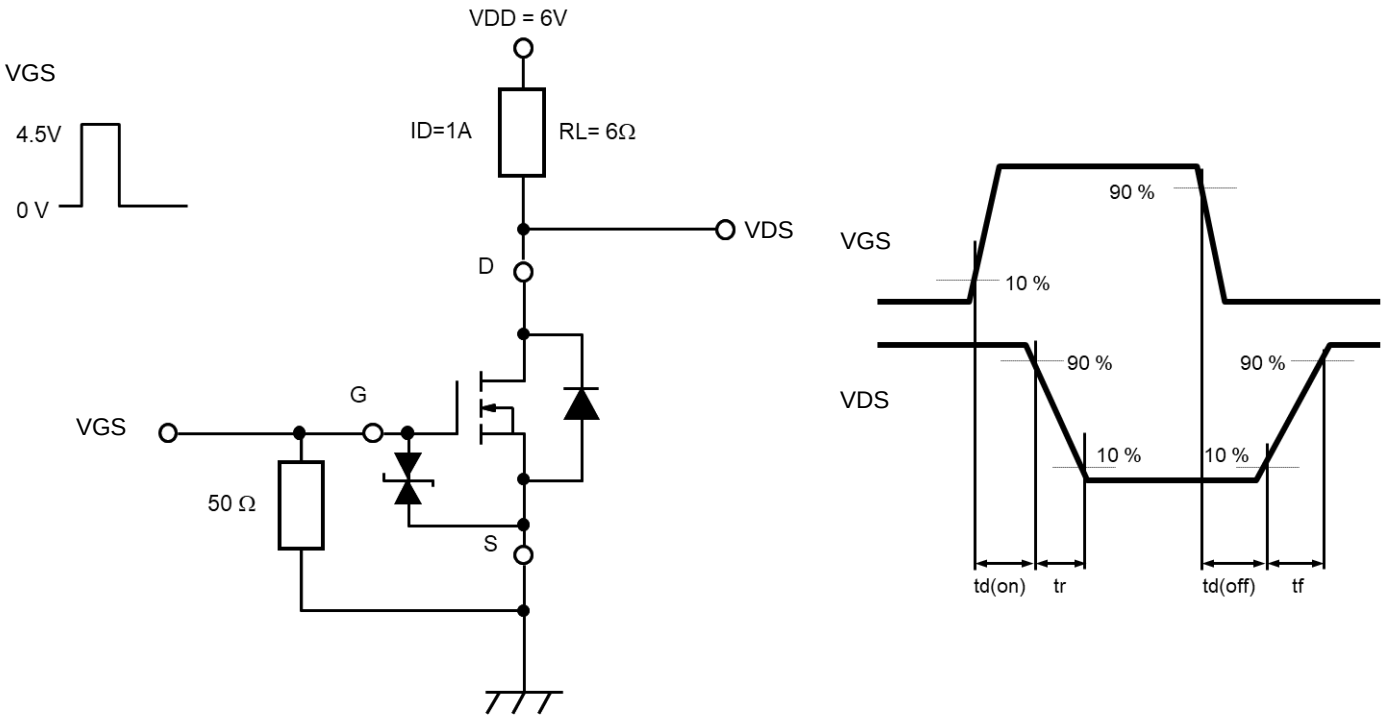


6. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0	12			V
Zero Gate Voltage Drain Current	IDSS	VDS = 12 V, VGS = 0			10	μA
Gate-Source Leakage Current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate Threshold Voltage	Vth	ID = 118 μA, VDS =10 V	0.3		1.0	V
Drain-Source ON Resistance	RDS(on)1	ID = 1.5 A, VGS = 4.5 V		47	64	mΩ
	RDS(on)2	ID = 1.0 A, VGS = 2.5 V		57	84	
	RDS(on)3	ID = 0.5 A, VGS = 1.8 V		70	119	
	RDS(on)4	ID = 0.25 A, VGS = 1.5 V		91	210	
Input Capacitance *1	Ciss	VDS = -10 V VGS = 0 V f = 1MHz		274		pF
Output Capacitance *1	Coss			63		
Reverse Transfer Capacitance *1	Crss			42		
Turn-on Delay Time *1,*2	td(on)	VDD = 6 V VGS = 0 to 4.5 V ID = 1.0 A		3.6		ns
Rise Time *1,*2	tr			3		
Turn-off Delay Time *1,*2	td(off)			34		
Fall Time *1,*2	tf			38		
Total Gate Charge *1	Qg	VDD = 6 V VGS = 4.5 V ID = 1.0 A		2.55		nC
Gate to Source Charge *1	Qgs			0.55		
Gate to Drain Miller Charge *1	Qgd			0.55		
Body Diode Forward Voltage	VF(D-S)	IF = 0.2 A, VGS = 0 V		0.6	1.2	V

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Guaranteed by design, not subject to production testing.
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

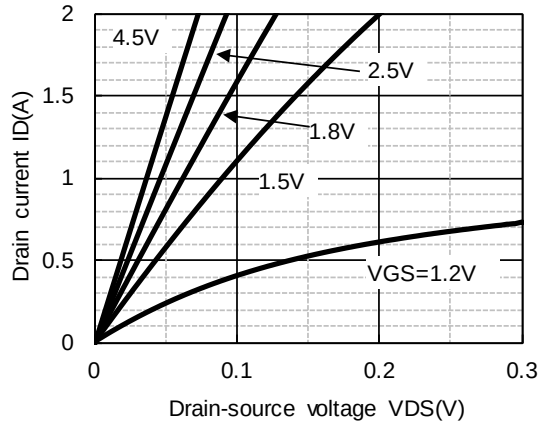


7. ELECTRICAL STATE DISCHARGE CHARACTERISTICS

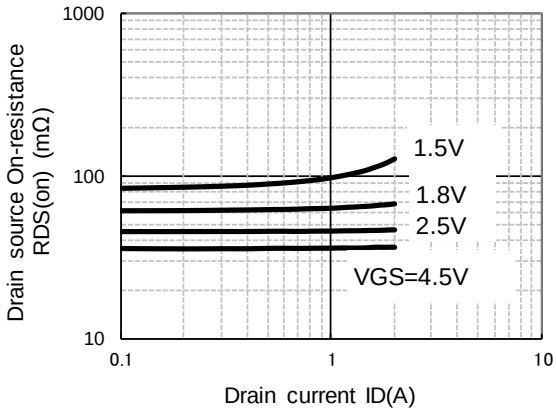
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H1B	> 500 to ≤ 1k	V
	Machine model	MM	C = 200 pF, R = 0 Ω	M1B	> 50 to ≤ 100	V

8. TECHNICAL DATA (Reference)

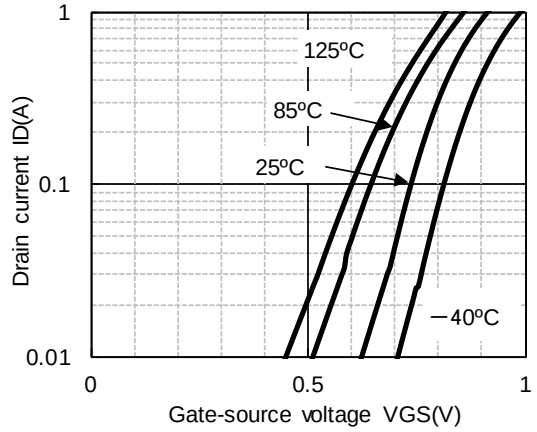
ID - VDS



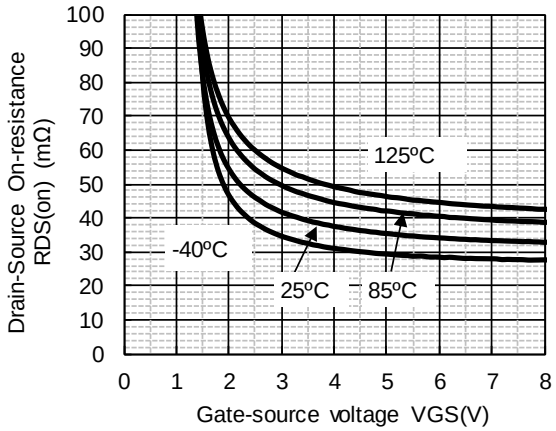
RDS(on) - ID



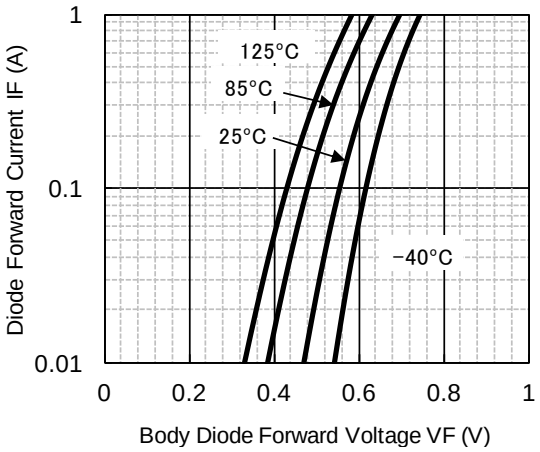
ID - VGS



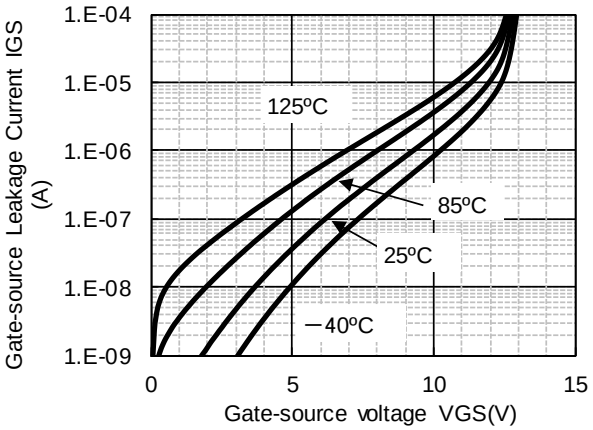
RDS(on) - VGS



IF - VF

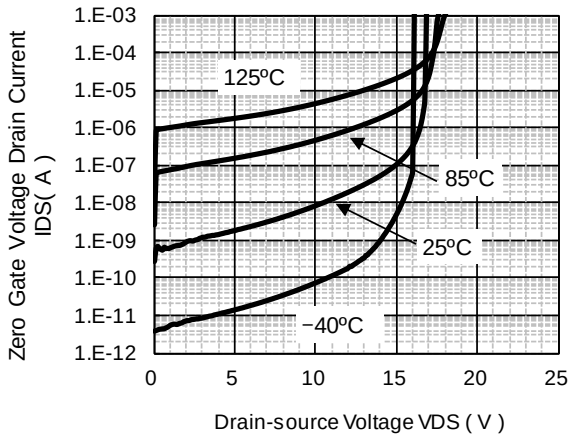


IGS - VGS

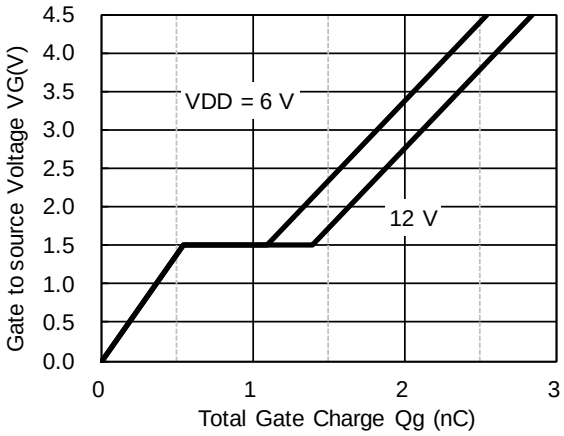


TECHNICAL DATA (Reference)

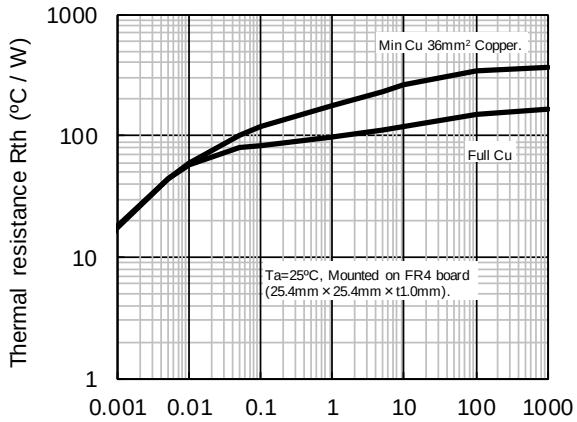
IDS - VDS



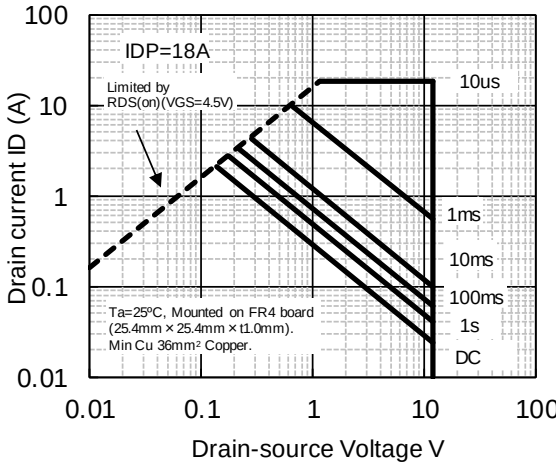
Dynamic Input/Output Characteristics



Rth - tsw

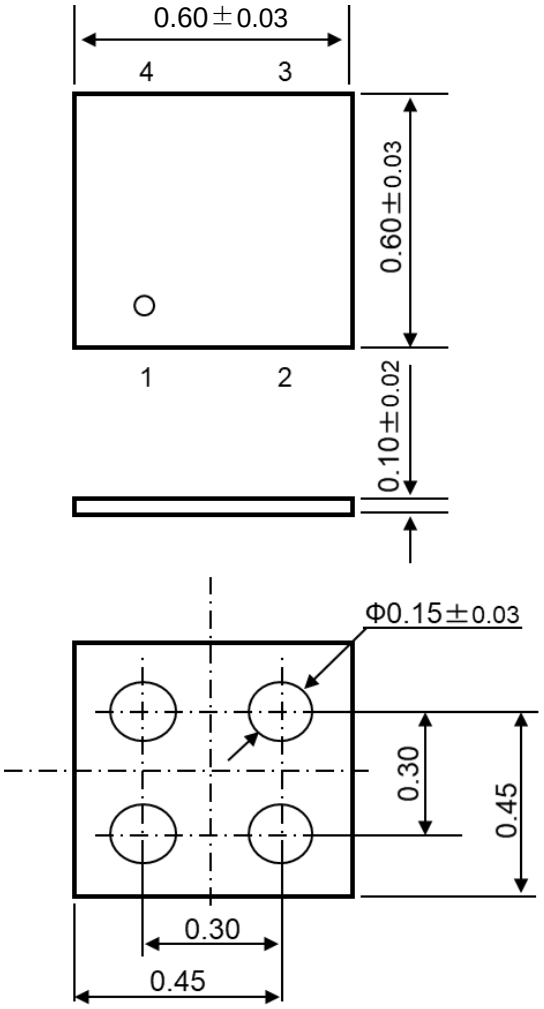


Safe Operating Area



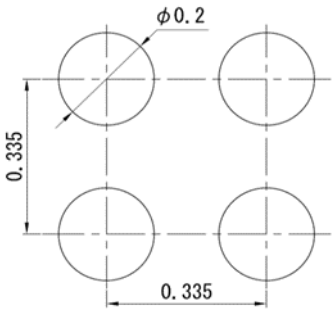
9. OUTLINE

Unit: mm



10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.02.05	1.00	1. Initially issued.
2021.08.31	1.01	1. Added important notice in Land Pattern. 2. Added special attention and precautions notes.
2021.11.11	1.02	1. Changed document name from Product Standards to Datasheet.

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