Single P-channel MOSFET

KFJ9B0466ZL
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Single P-channel MOSFET for automotive.

2. FEATURES

- Drain-source On-state Resistance: RDS(on) typ = 27 mΩ (VGS = - 10 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)
- AEC-Q101 Qualified

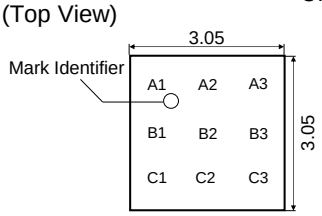
3. MARKING SYMBOL: UK

4. PACKAGING

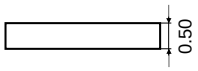
Embossed type (Thermo-compression sealing): 5,000 pcs / reel (standard)

Unit: mm

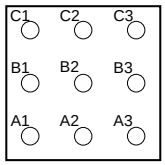
(Top View)



(Front View)



(Bottom View)



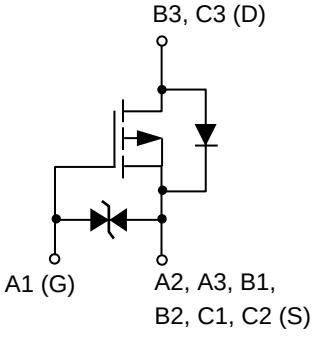
A1. Gate

B3, C3. Drain

A2, A3, B1, B2, C1, C2. Source

Package	MLGA009-W-3030-FA

Equivalent Circuit



5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	- 40	V
Gate-source Voltage		VGS	- 20 / + 10	V
Drain Current	DC *1	ID1	- 4.9	A
	DC *2	ID2	- 7.0	
	DC *3	ID3	- 8.4	
	Pulsed *4	IDp	- 56.0	
Total Power Dissipation	DC *1	PD1	0.86	W
	DC *2	PD2	1.75	
	DC *3	PD3	2.50	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	145	°C / W
	Rth2 *2	72	
	Rth3 *3	50	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (79.9 mm^2 area, 36 µm thickness).

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (616 mm^2 area, 36 µm thickness).

*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

*4 t = 10 µs, Duty Cycle ≤ 1 %.

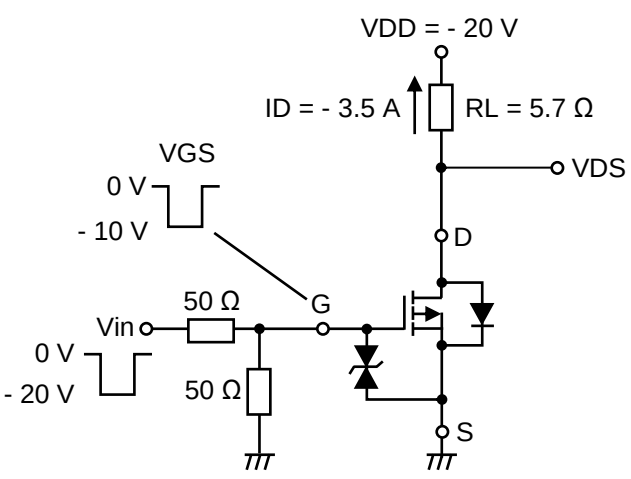
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

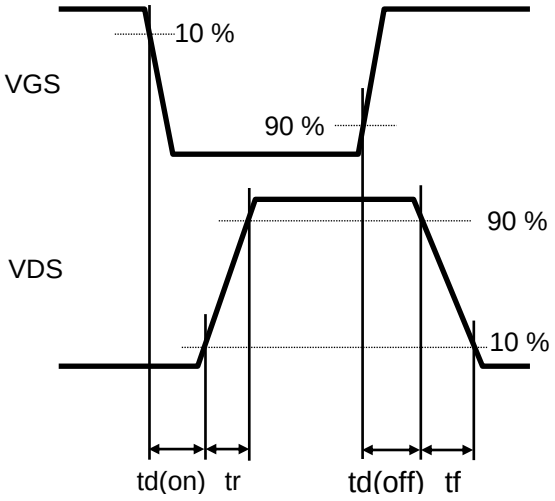
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = - 1 mA, VGS = 0 V	- 40			V
Zero Gate Voltage Drain Current	IDSS	VDS = - 40 V, VGS = 0 V			- 1	µA
Gate-source Leakage Current	IGSS	VGS = - 16 V, VDS = 0 V			- 10	µA
		VGS = + 8 V, VDS = 0 V			10	
Gate-source Threshold Voltage	Vth	ID = - 16.8 mA, VDS = - 10 V	- 1	- 2	- 3	V
Drain-source On-state Resistance	RDS(on)1	ID = - 2 A, VGS = - 10 V	19	27	35	mΩ
	RDS(on)2	ID = - 2 A, VGS = - 4.5 V	21	30	49	
Body Diode Forward Voltage	VF(s-d)	IF = - 2 A, VGS = 0 V		- 0.8	- 1.0	V
Input Capacitance *1	Ciss	VDS = - 20 V, VGS = 0 V f = 1 MHz		7500		pF
Output Capacitance *1	Coss			500		
Reverse Transfer Capacitance *1	Crss			450		
Turn-on Delay Time *1, *2	td(on)	VDD = - 20 V, VGS = 0 to - 10 V ID = - 3.5 A		40		ns
Rise Time *1, *2	tr			70		
Turn-off Delay Time *1, *2	td(off)	VDD = - 20 V, VGS = - 10 to 0 V ID = - 3.5 A		580		
Fall Time *1, *2	tf			200		
Total Gate Charge *1	Qg1	VDD = - 20 V, VGS = - 4.5 V ID = - 7 A		70		nC
	Qg2	VDD = - 20 V, VGS = - 10 V ID = - 7 A		140		
Gate-source Charge *1	Qgs			20		
Gate-drain Charge *1	Qgd			26		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



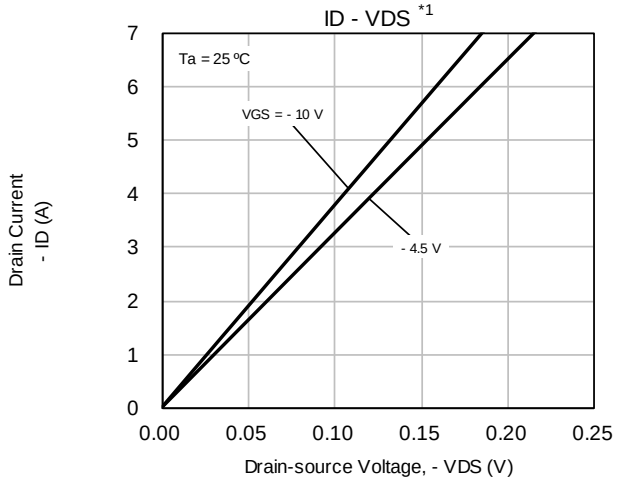


8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

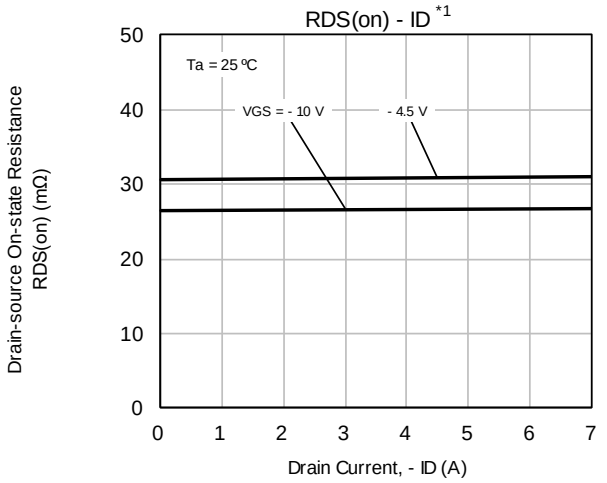
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H3A	> 4 to ≤ 8	kV

9. TECHNICAL DATA (Reference)

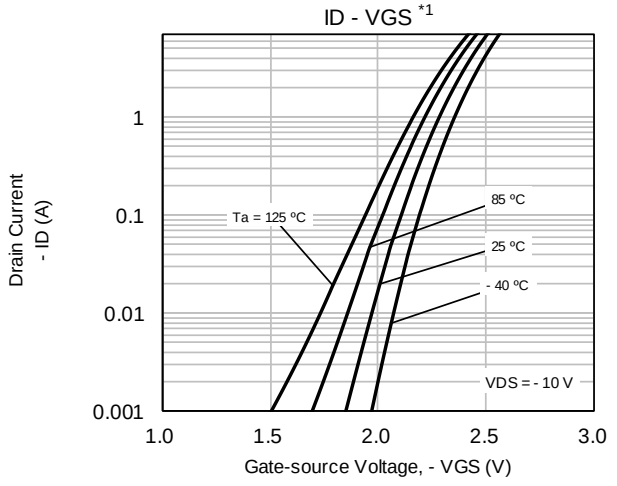
ID - VDS *1



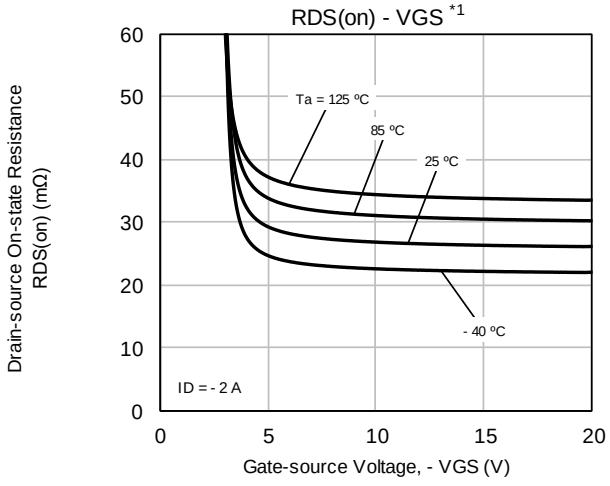
RDS(on) - ID *1



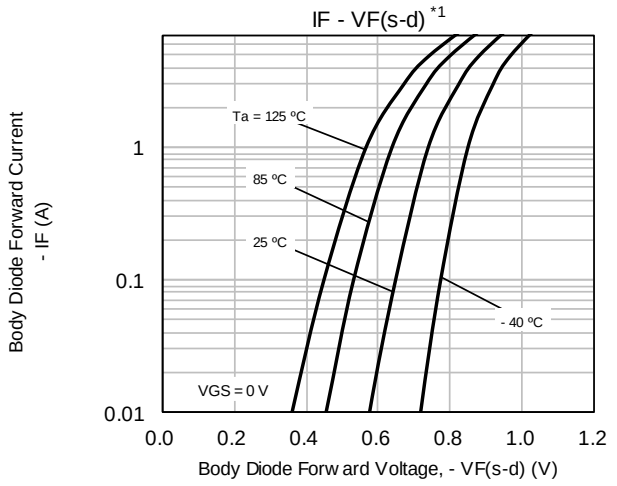
ID - VGS *1



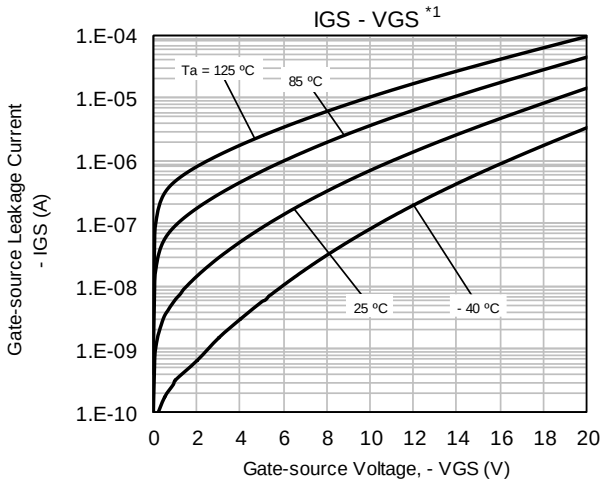
RDS(on) - VGS *1



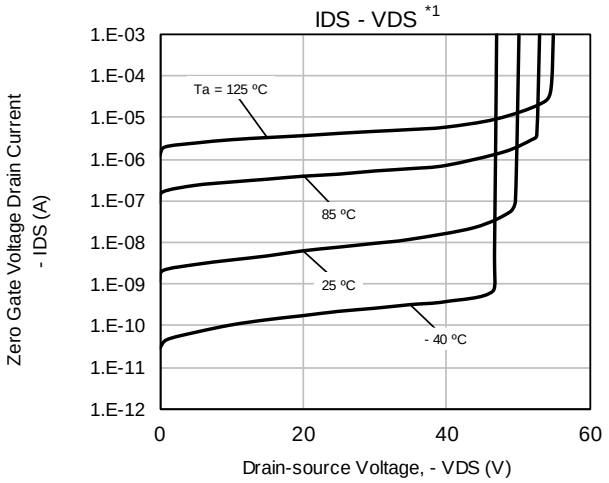
IF - VF(s-d) *1

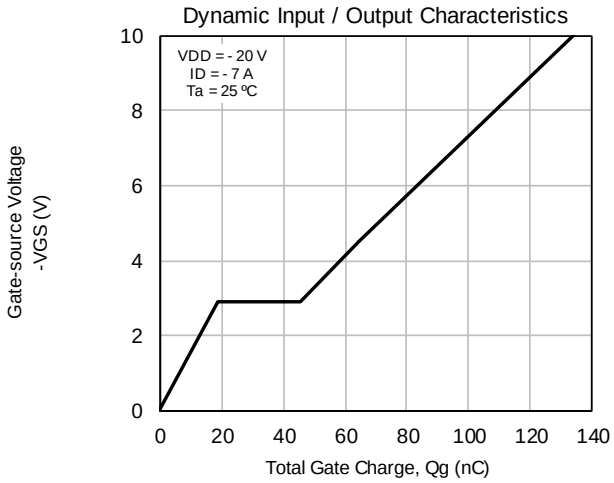


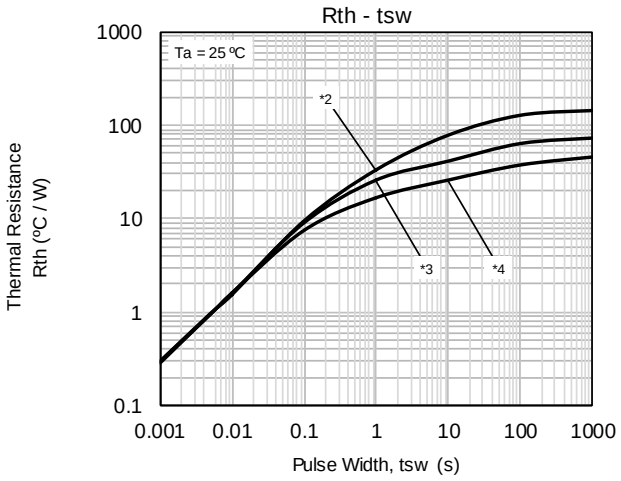
IGS - VGS *1

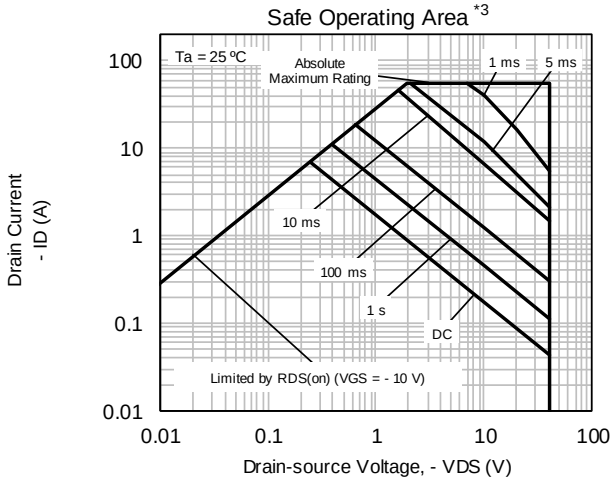


TECHNICAL DATA (Reference)









Note

*1 Pulse measurement.

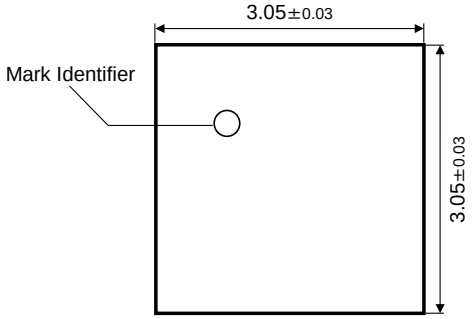
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (79.9 mm^2 area, 36 µm thickness).

*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (616 mm^2 area, 36 µm thickness).

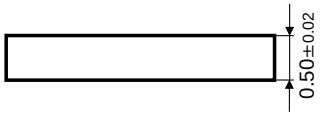
*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

10. OUTLINE

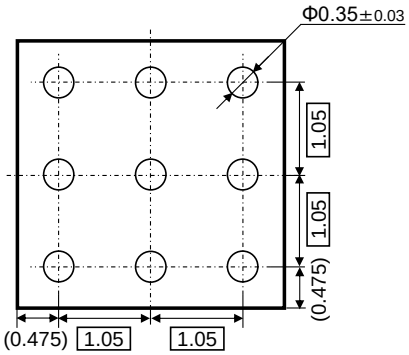
(Top View) Unit: mm



(Front View)

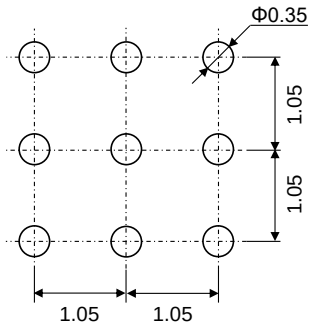


(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.4.16	1.00	1. Initially issued.
2021.11.15	1.01	1. Changed document name from Product Standards to Datasheet.
		2. Added electrostatic discharge
		3. Added important notice in Land Pattern.
		4. Added special attention and precautions notes.

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