Single N-channel MOSFET

KFK9B0652ZL Datasheet

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1. GENERAL DESCRIPTION

Single N-channel MOSFET for automotive.

2. FEATURES

- Drain-source On-state Resistance: RDS(on) typ = $18 \text{ m}\Omega$ (VGS = 10 V)
- · CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)
- AEC-Q101 Qualified

3. MARKING SYMBOL: WW

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

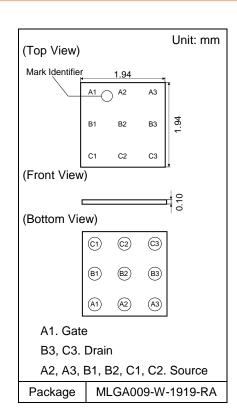
Parameter		Symbol	Rating	Unit	
Drain-source Voltage		VDS	60	V	
Gate-source Voltage		VGS	+ 20 / - 10	V	
	DC *1	ID1	5.5	А	
Drain Current	DC *2	ID2	8.3		
Drain Current	DC *3	ID3	10.0		
	Pulsed*4	IDp	66.4		
	DC *1	PD1	0.71		
Total Power Dissipation	DC *2	PD2	1.60	W	
	DC *3	PD3	2.31		
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C	

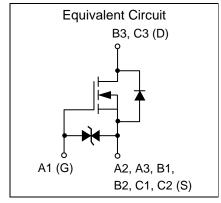
6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
	Rth1 *1	175	
Thermal Resistance (ch-a)	Rth2 *2	79	°C / W
	Rth3 *3	54	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (79.2 mm² area, 36 µm thickness).

- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (616 mm² area, 36 µm thickness).
- *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
- *4 $t = 10 \mu s$, Duty Cycle $\leq 1 \%$.





Rev 1.00

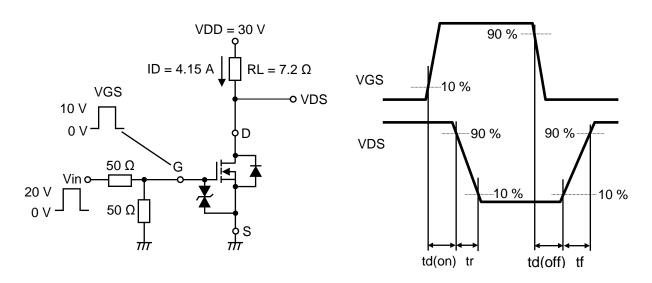


7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit	
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	60			V	
Zero Gate Voltage Drain Current	IDSS	VDS = 60 V, VGS = 0 V			1	μΑ	
Cata aguiras Laglagas Current	IGSS	VGS = + 16 V, VDS = 0 V			10		
Gate-source Leakage Current		VGS = - 8 V, VDS = 0 V			- 10	μA	
Gate-source Threshold Voltage	Vth	ID = -1.85 mA, VDS = 10 V	1	2	3	V	
Duein course On state Desistance	RDS(on)1	ID = 2 A, VGS = 10 V	10	18	23	mΩ	
Drain-source On-state Resistance	RDS(on)2	ID = 2 A, VGS = 4.5 V	12	20	33		
Body Diode Forward Voltage	VF(s-d)	IF = 2 A, VGS = 0 V		0.77	1.2	V	
Input Capacitance *1	Ciss	VPC 20 V VCC 0 V		1400			
Output Capacitance *1	Coss	VDS = 30 V, VGS = 0 V f = 1 MHz		110		pF	
Reverse Transfer Capacitance *1	Crss			60			
Turn-on Delay Time *1, *2	td(on)	VDD = 30 V, VGS = 0 to 10 V		13			
Rise Time *1, *2	tr	ID = 4.15 A		25			
Turn-off Delay Time *1, *2	td(off)	VDD = 30 V, VGS = 10 to 0 V		80		ns	
Fall Time *1, *2	tf	ID = 4.15 A		60			
	0.4	VDD = 30 V, VGS = 4.5 V		40			
Total Gate Charge *1	Qg1	ID = 8.3 A	13				
	Qg2	VPD 00 V VOQ 40 V		26		nC	
Gate-source Charge *1	Qgs	VDD = 30 V, VGS = 10 V		4.5]	
Gate-drain Charge *1	Qgd	ID = 8.3 A		5			

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

- *1 Guaranteed by design, not subject to production testing.
- *2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

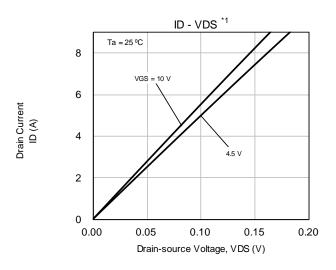


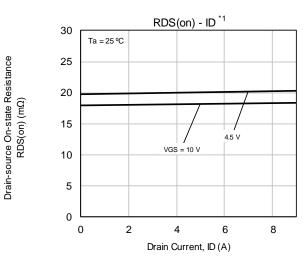
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

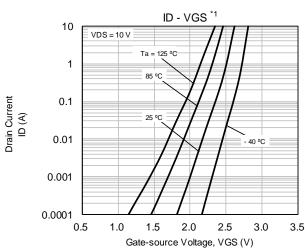
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	$C = 100 \text{ pF}, R = 1.5 \text{ k}\Omega$	H2	> 2 to ≤ 4	kV

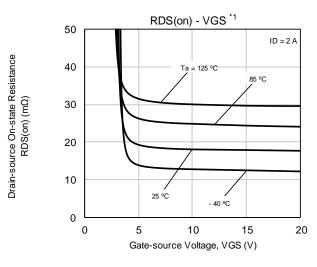


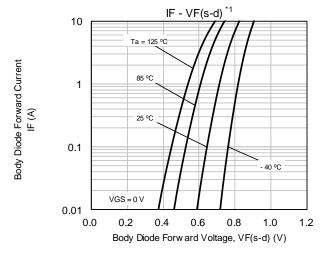
9. TECHNICAL DATA (Reference)

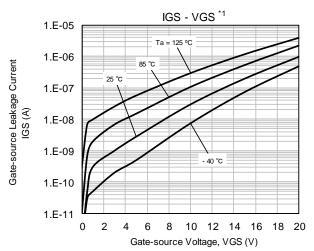








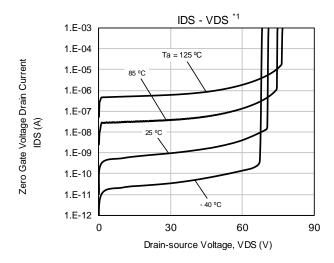


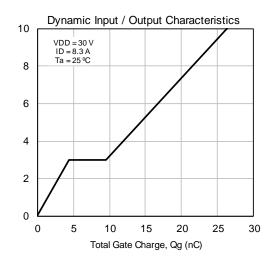


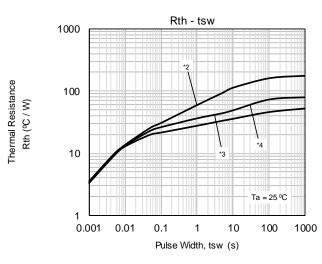
Gate-source Voltage VGS (V)

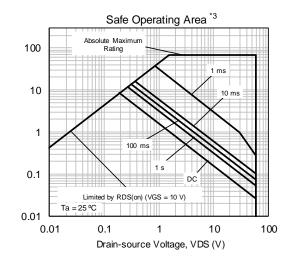
Drain Current ID (A)

TECHNICAL DATA (Reference)









Note

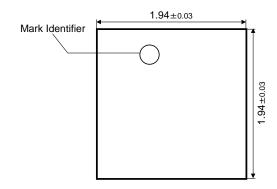
- Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (79.2 mm² area, 36 µm thickness).
- Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). *3 FR4 board fully covered with copper pad (616 mm² area, 36 µm thickness).
- Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).



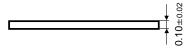
10. OUTLINE

(Top View)

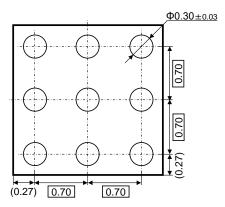
Unit: mm



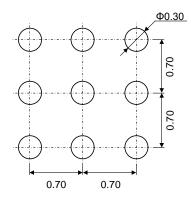
(Front View)



(Bottom View)



11. LAND & STENCIL PATTERN (Reference)



Unit: mm

Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

ADVANCE INFORMATION



KFK9B0652ZL

12. REVISION HISTORY

Date	Revision	Description
2021.11.19	1.00	1. Initially issued.



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