

Gate resistor installed Dual N-channel MOSFET

KFCAB22620L Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: $R_{SS(on)}$ typ = 2.4 m Ω (V_{GS} = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: W7

4. PACKAGING

Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

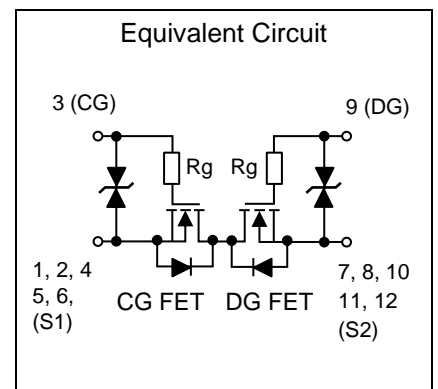
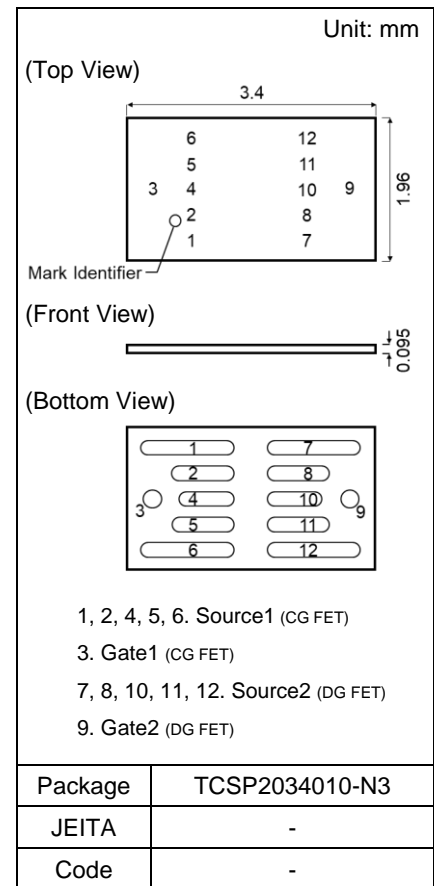
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	23	V
Gate-source Voltage	VGS	± 12	V
Source Current	DC ^{*1}	IS1	A
	DC ^{*2}	IS2	
	DC ^{*3}	IS3	
	Pulsed ^{*4}	ISp	
Total Power Dissipation	DC ^{*1}	PD1	W
	DC ^{*2}	PD2	
	DC ^{*3}	PD3	
Operating Junction and Storage Temperature Range	Tj, Tstg	- 55 to + 150	$^\circ\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 ^{*1}	212	$^\circ\text{C} / \text{W}$
	Rth2 ^{*2}	66	
	Rth3 ^{*3}	36	

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (41 mm² area, 36 μm thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (604 mm² area, 36 μm thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$.



7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	23			V
Zero Gate Voltage Source Current	ISSS	VSS = 23 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS1	VGS = ± 8 V, VSS = 0 V			± 10	μA
	IGSS2	VGS = ± 5 V, VSS = 0 V			± 1	
Gate-source Threshold Voltage	Vth	IS = 1.15 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 6.9 A, VGS = 4.5 V	1.6	2.2	2.9	m Ω
	RSS(on)2	IS = 6.9 A, VGS = 3.8 V	1.7	2.4	3.1	
	RSS(on)3	IS = 6.9 A, VGS = 3.1 V	1.8	2.8	4.6	
	RSS(on)4	IS = 6.9 A, VGS = 2.5 V	3.0	5.0	9.8	
Body Diode Forward Voltage	VF(s-s)	IF = 6.9 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		3500		pF
Output Capacitance *1	Coss			430		
Reverse Transfer Capacitance *1	Crss			340		
Total Gate Charge *1	Qg	VDD = 10 V		29		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		8		
Gate-drain Charge *1	Qgd	IS = 13.8 A		9		

(MOSFET: CG FET)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on Delay Time *1, *2	td(on)	VDD = 10 V, VCGS1 = 0 to 4 V		0.04		μs
Rise Time *1, *2	tr	IS = 6.9 A		0.18		
Turn-off Delay Time *1, *2	td(off)	VDD = 10 V, VCGS1 = 4 to 0 V		0.20		μs
Fall Time *1, *2	tf	IS = 6.9 A		0.20		
Gate Resistance *1	Rg	f = 1 MHz	2	7	13	Ω

(MOSFET: DG FET)

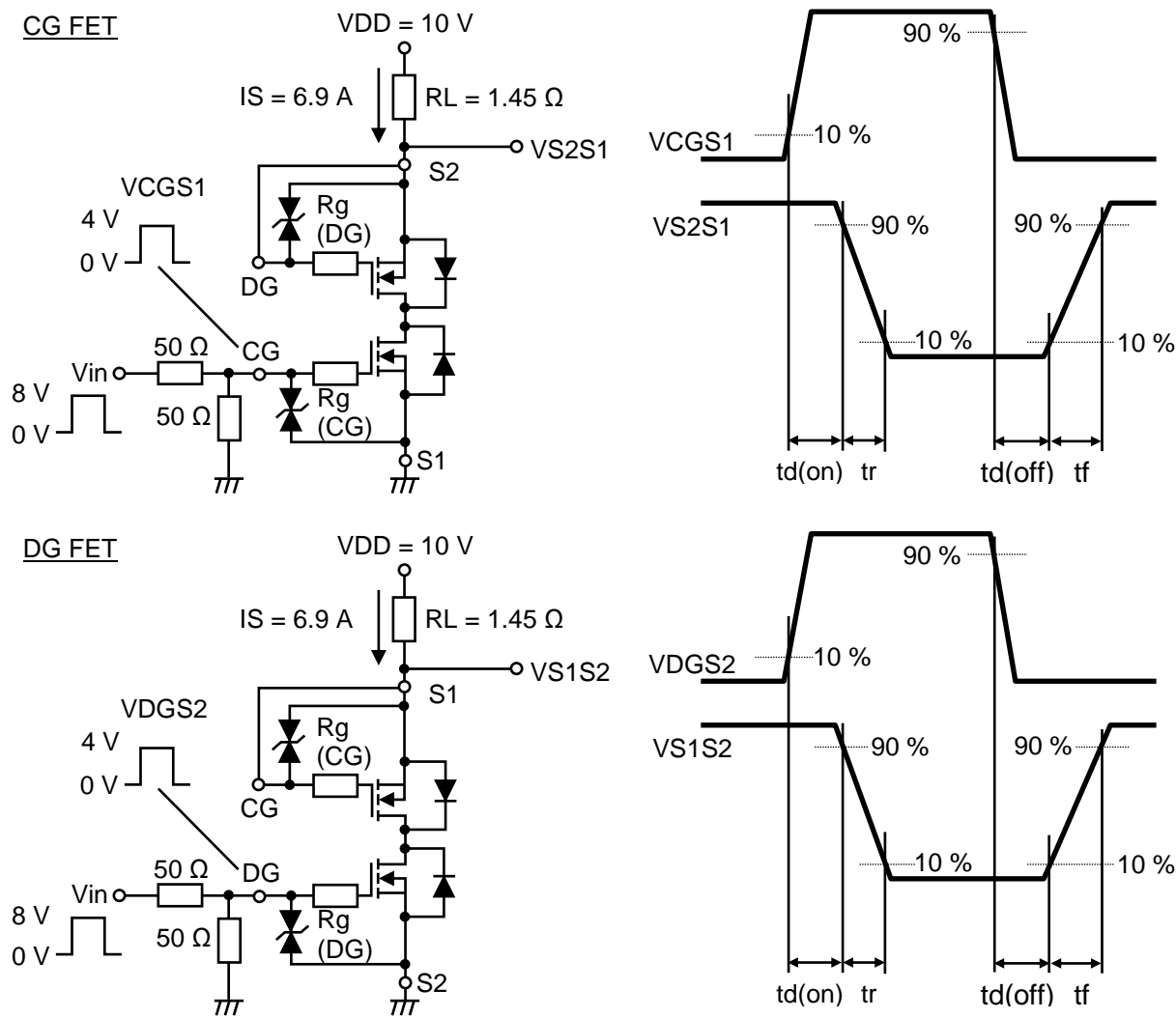
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on Delay Time *1, *2	td(on)	VDD = 10 V, VDGS2 = 0 to 4 V		1.2		μs
Rise Time *1, *2	tr	IS = 6.9 A		2.6		
Turn-off Delay Time *1, *2	td(off)	VDD = 10 V, VDGS2 = 4 to 0 V		5.2		μs
Fall Time *1, *2	tf	IS = 6.9 A		4.1		
Gate Resistance *1	Rg	f = 1 MHz	400	700	1000	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

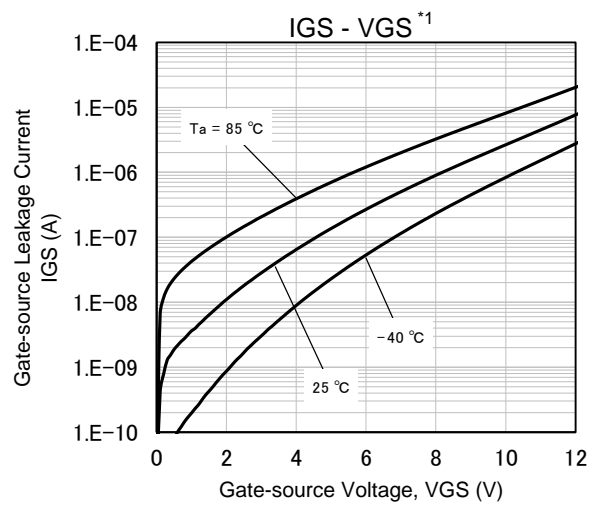
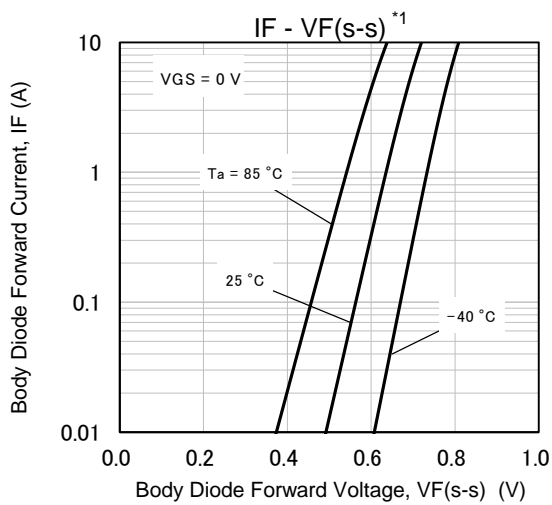
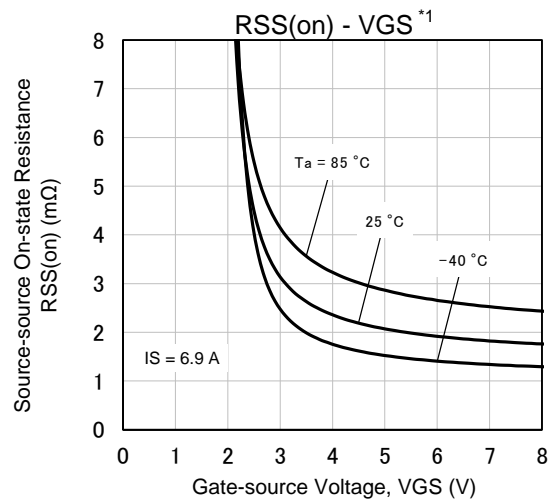
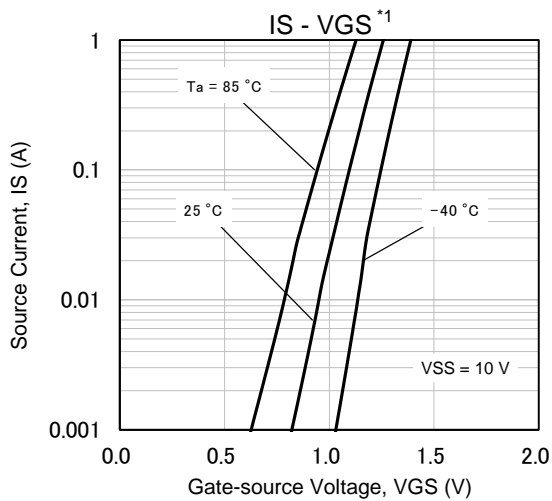
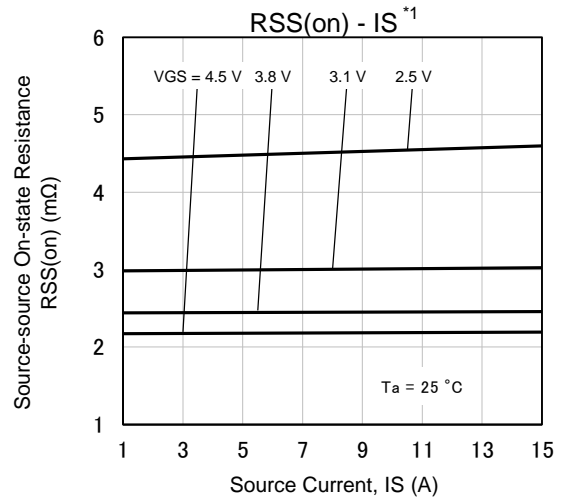
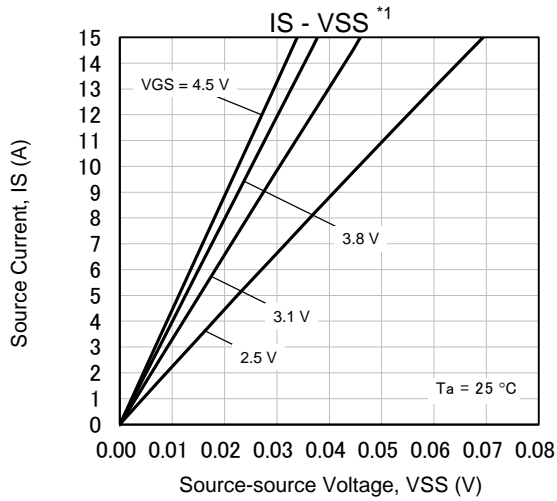
Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



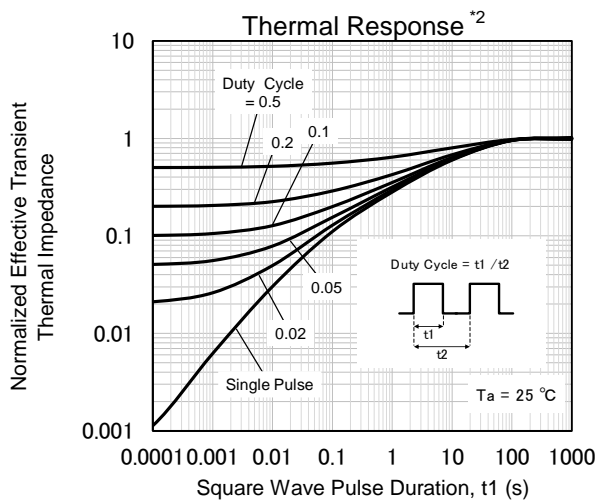
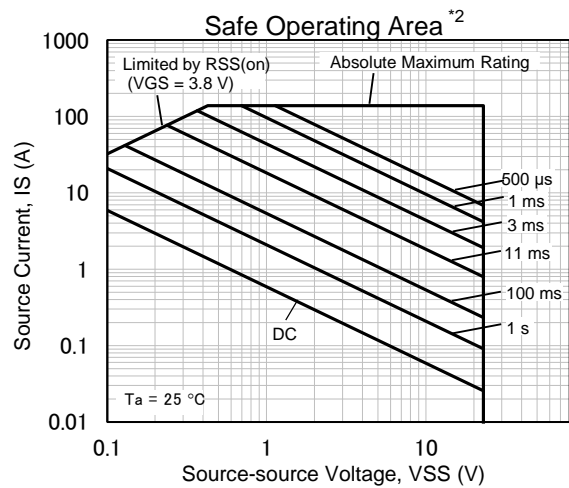
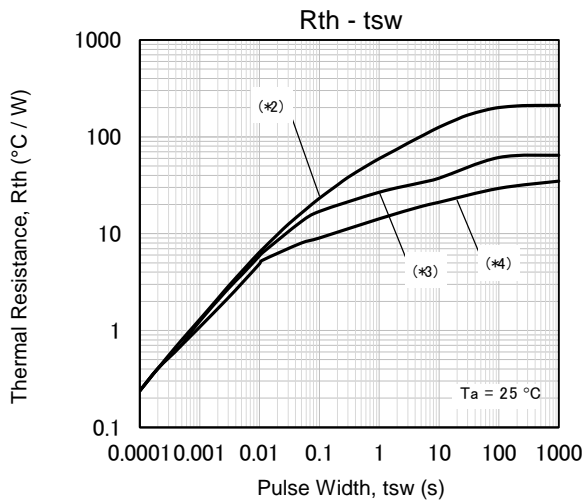
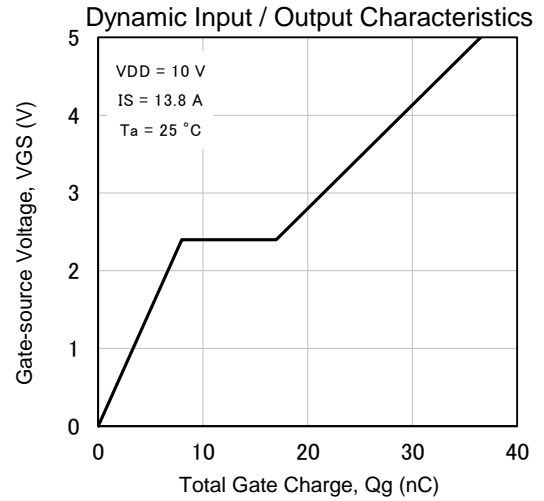
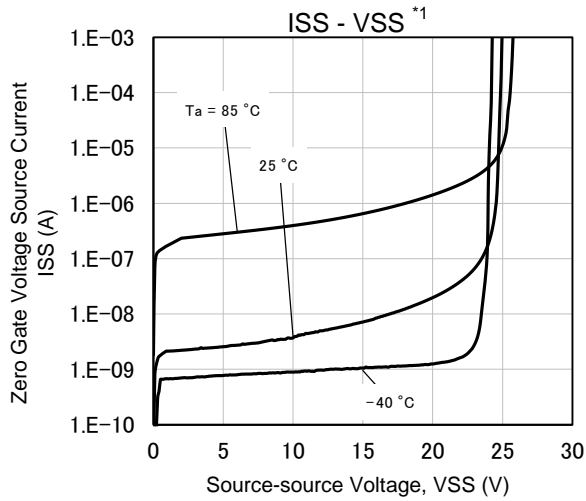
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H2	> 2 to ≤ 4	kV

9. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



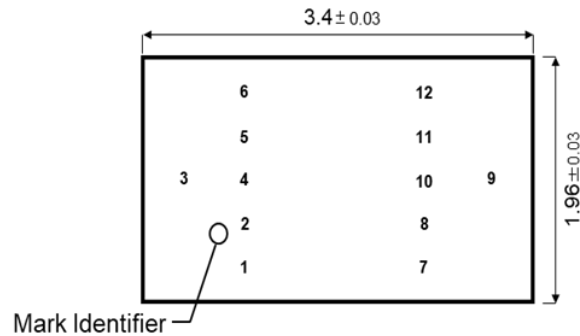
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad
(41 mm² area, 36 μm thickness).
- *3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad
(604 mm² area, 36 μm thickness).
- *4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

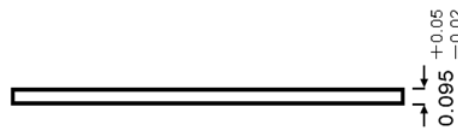
10. OUTLINE

(Top View)

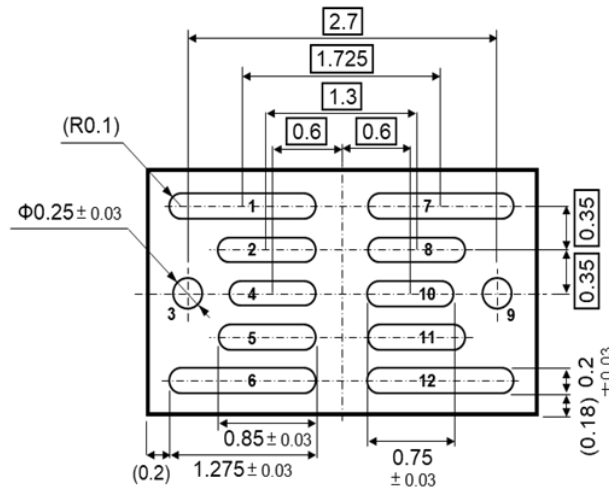
Unit: mm



(Front View)



(Bottom View)

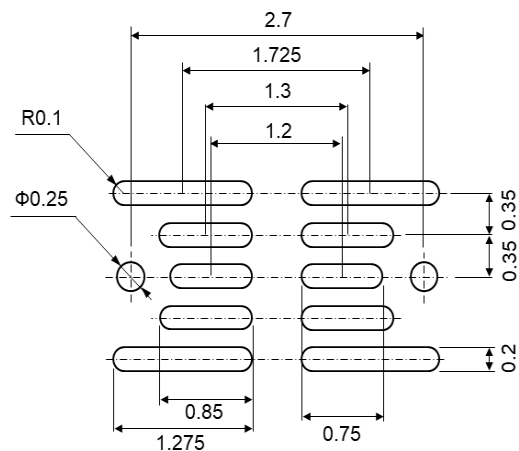
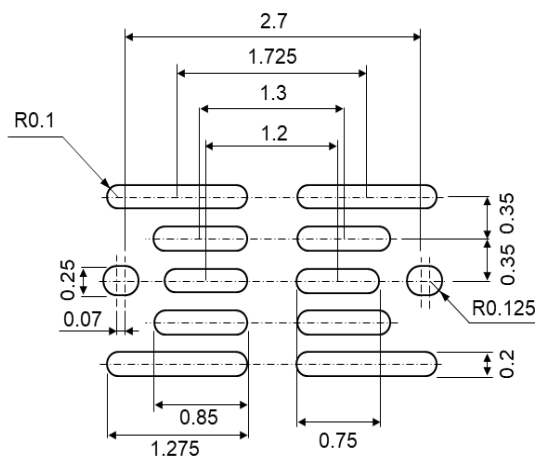


11. LAND & STENCIL PATTERN (Reference)

LAND

STENCIL

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.06.03	1.00	1. Initially issued.
2021.08.31	1.01	1. Changed document name from Product Standards to Datasheet. 2. Added important notice in Land Pattern. 3. Added special attention and precautions notes.

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