Dual N-channel MOSFET

FCAB22710L
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Dual N-channel MOSFET.

2. FEATURES

- Source-source On-state Resistance: RSS(on) typ = 7.5 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

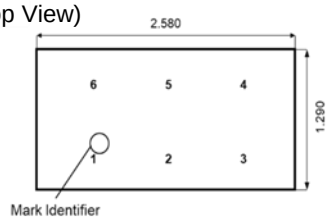
3. MARKING SYMBOL: WJ

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

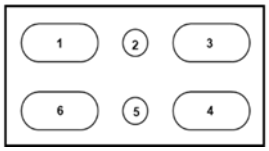
Unit: mm

(Top View)



(Front View)

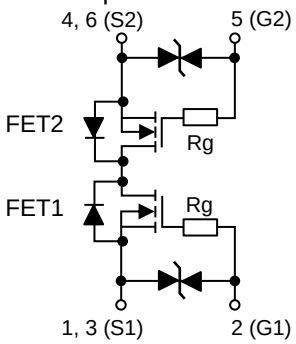
(Bottom View)



1, 3. Source1 (FET1) 2. Gate1 (FET1)
4, 6. Source2 (FET2) 5. Gate2 (FET2)

Package	TCSP1326008-N4
JEITA	-
Code	-

Equivalent Circuit



5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	20	V
Gate-source Voltage		VGS	± 12	V
Source Current	DC *1	IS1	6.1	A
	DC *2	IS2	10.9	
	DC *3	IS3	15.0	
	Pulsed *4	ISp	61.0	
Total Power Dissipation	DC *1	PD1	0.51	W
	DC *2	PD2	1.60	
	DC *3	PD3	3.00	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	245	°C / W
	Rth2 *2	78	
	Rth3 *3	41	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (22 mm^2 area, 36 µm thickness).
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (602 mm^2 area, 36 µm thickness).
*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
*4 t = 10 µs, Duty Cycle ≤ 1 %.

7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 20 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS1	VGS = ± 8 V, VSS = 0 V			± 10	μA
	IGSS2	VGS = ± 5 V, VSS = 0 V			± 1	
Gate-source Threshold Voltage	Vth	IS = 0.54 mA, VSS = 10 V	1.30	1.85	2.35	V
Source-source On-state Resistance	RSS(on)1	IS = 3.05 A, VGS = 4.5 V	3.9	5.5	7.5	mΩ
	RSS(on)2	IS = 3.05 A, VGS = 3.8 V	5.3	7.5	12.5	
	RSS(on)3	IS = 0.20 A, VGS = 3.1 V	5.4	16.5	70.0	
Body Diode Forward Voltage	VF(s-s)	IF = 3.05 A, VGS = 0 V		0.8	1.2	V
Turn-on Delay Time *1, *2	td(on)	VDD = 10 V, VGS = 0 to 4 V		62		ns
Rise Time *1, *2	tr	IS = 3.05 A		240		
Turn-off Delay Time *1, *2	td(off)	VDD = 10 V, VGS = 4 to 0 V		155		ns
Fall Time *1, *2	tf	IS = 3.05 A		140		
Total Gate Charge *1	Qg	VDD = 10 V		17.5		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		6.5		
Gate-drain Charge *1	Qgd	IS = 6.1 A		6.5		
Gate Resistance *1	Rg	f = 1 MHz		24.5		Ω

(MOSFET: FET1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance *1	Ciss	VSS = 10 V, f = 1 kHz VGS1 = 0 V, VGS2 = 6 V		2320		pF
Output Capacitance *1	Coss			265		
Reverse Transfer Capacitance *1	Crss			205		

(MOSFET: FET2)

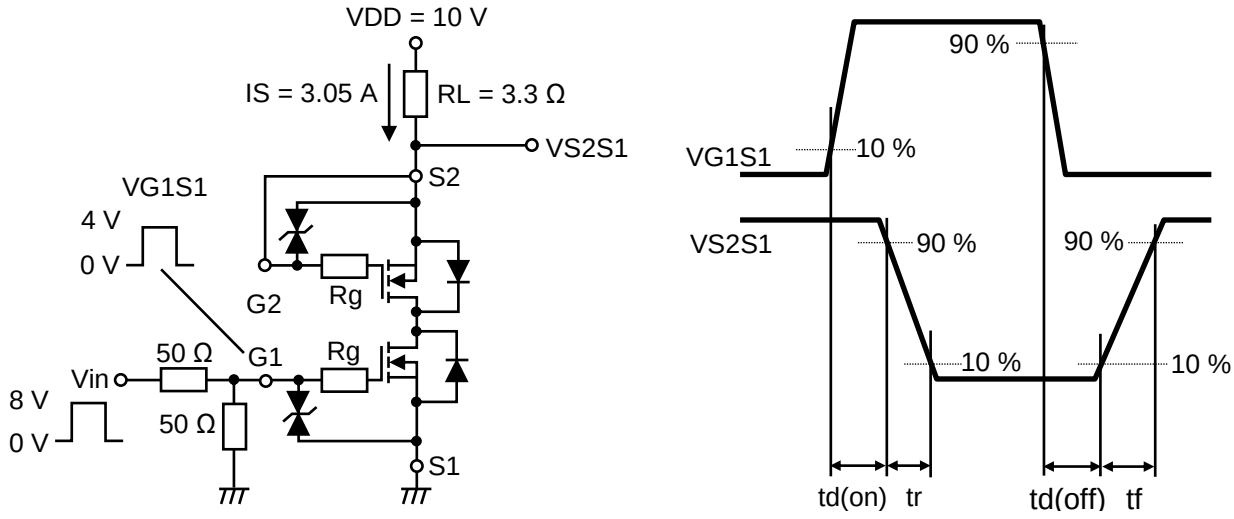
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance *1	Ciss	VSS = 10 V, f = 1 kHz VGS2 = 0 V, VGS1 = 6 V		2320		pF
Output Capacitance *1	Coss			265		
Reverse Transfer Capacitance *1	Crss			205		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

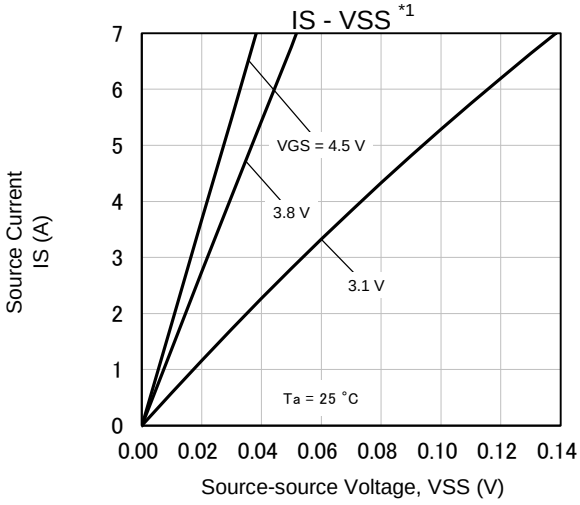


8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

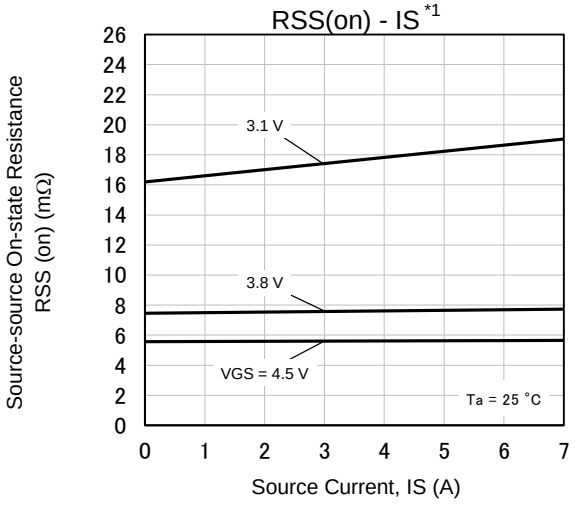
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H1B	> 0.5 to ≤ 1	kV

9. TECHNICAL DATA (Reference)

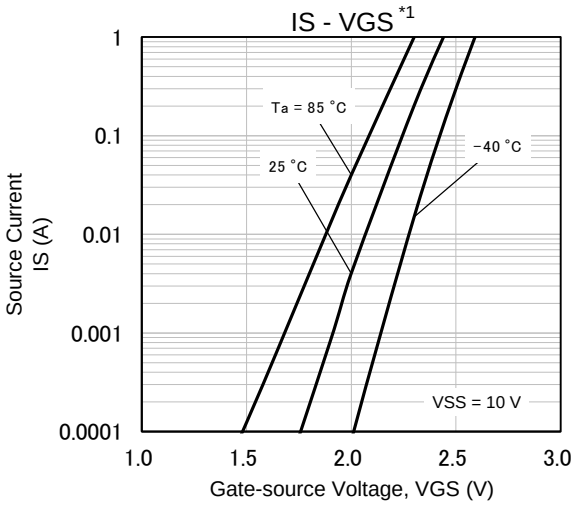
IS - VSS *1



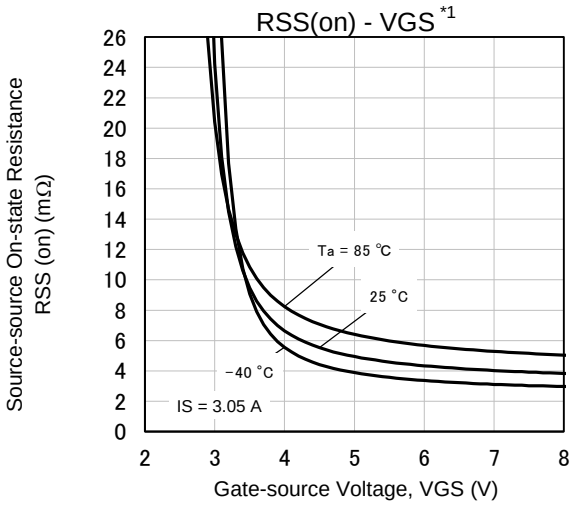
RSS(on) - IS *1



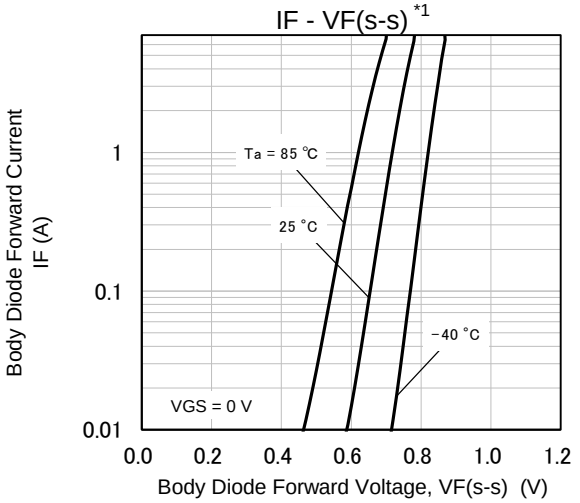
IS - VGS *1



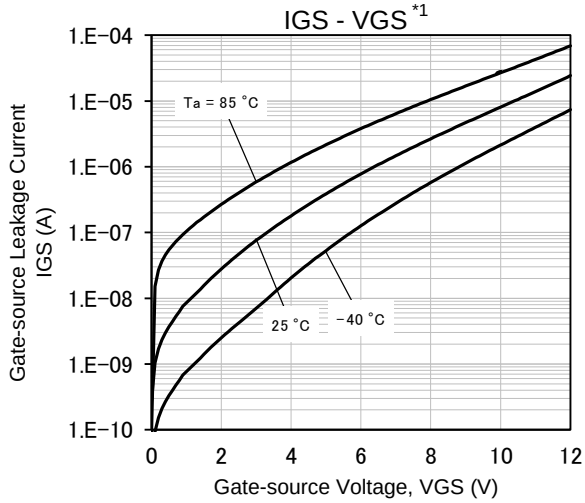
RSS(on) - VGS *1



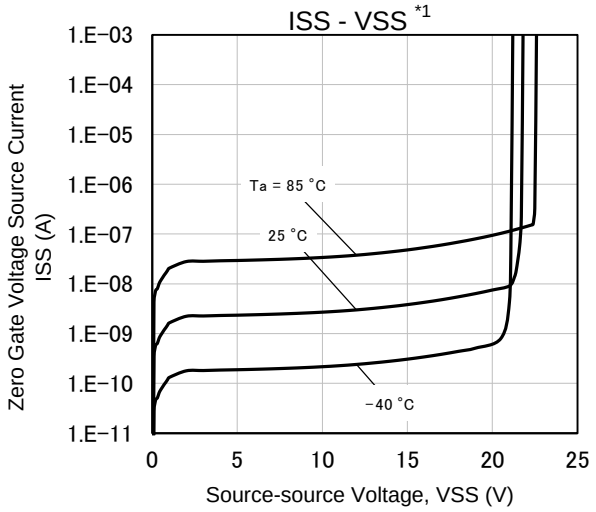
IF - VF(s-s) *1

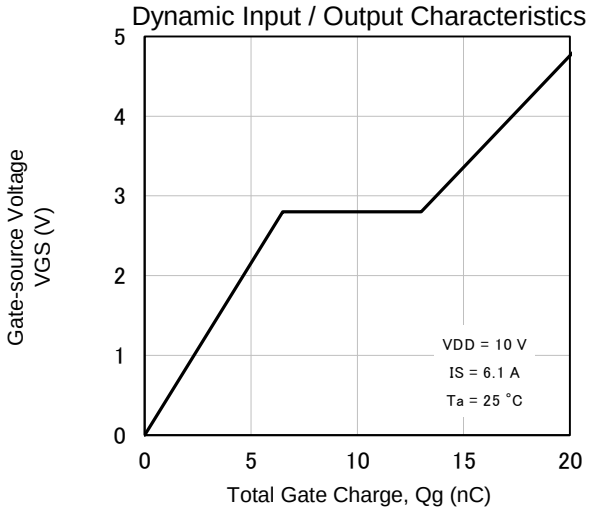


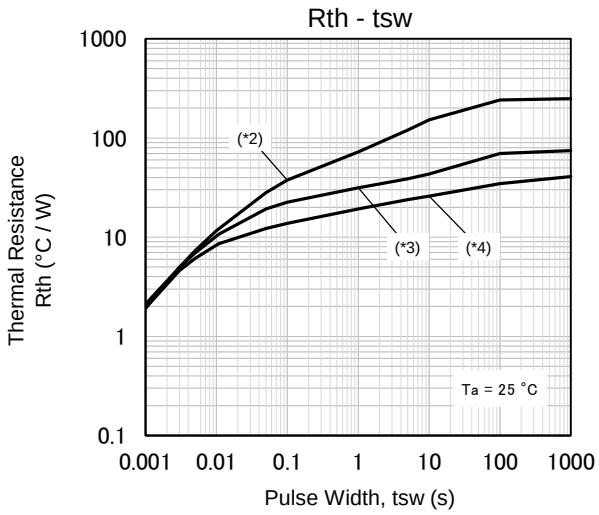
IGS - VGS *1

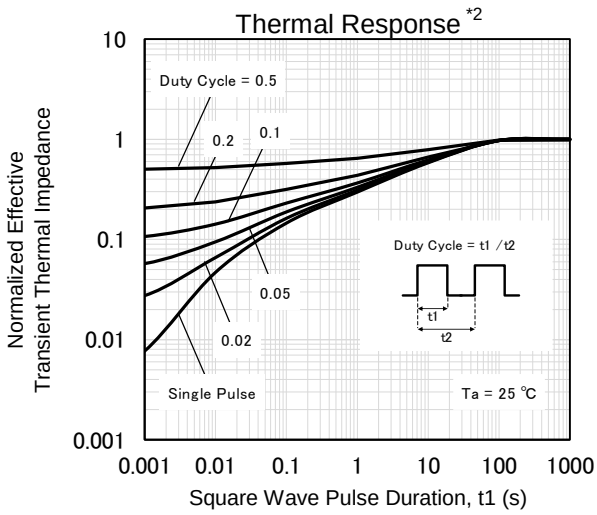


TECHNICAL DATA (Reference)









Note

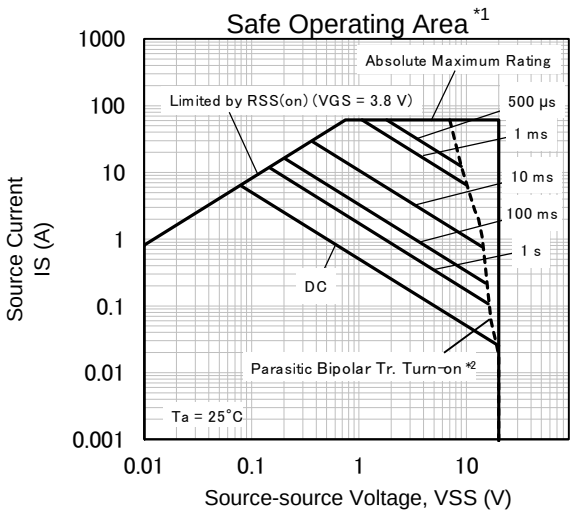
*1 Pulse measurement.

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad
(22 mm^2 area, 36 µm thickness).

*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad
(602 mm^2 area, 36 µm thickness).

*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

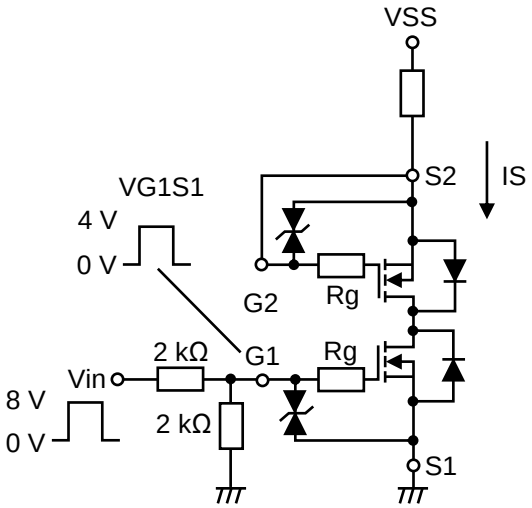
TECHNICAL DATA (Reference)



Note

*1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad
(22 mm^2 area, 36 µm thickness).

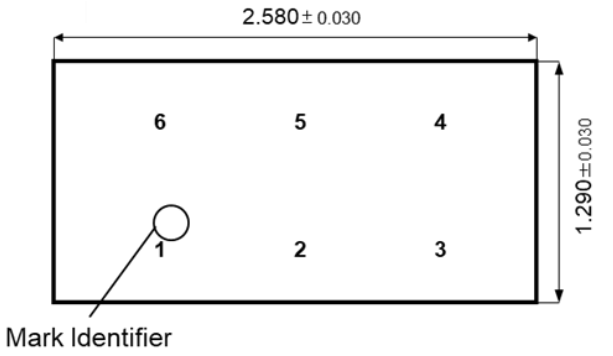
*2 Measurement circuit for Parasitic Bipolar Tr. Turn-on.



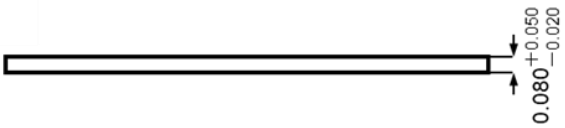
10. OUTLINE

(Top View)

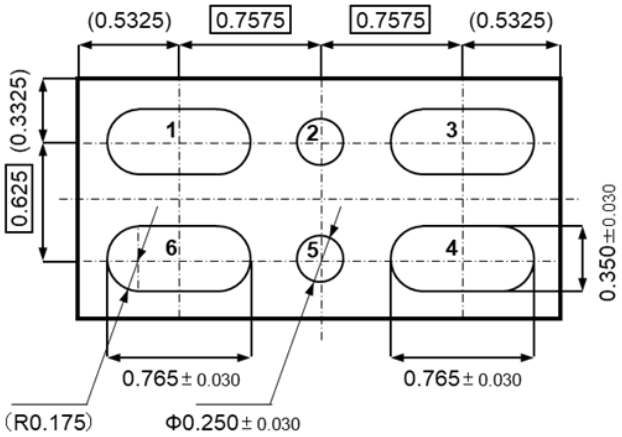
Unit: mm



(Front View)

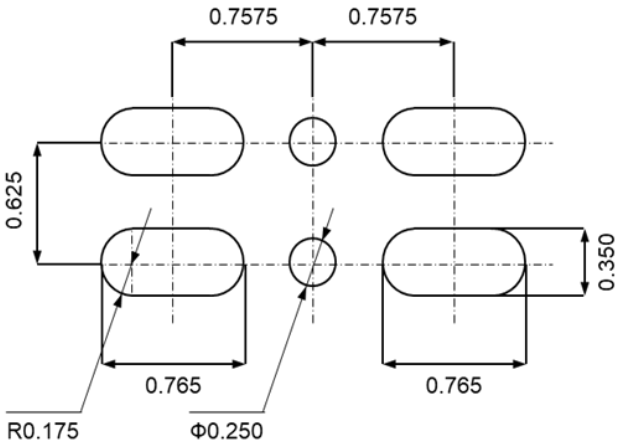


(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.06.09	1.00	1. Initially issued.
2021.08.31	1.01	1. Added important notice in Land Pattern. 2. Added special attention and precautions notes.
2021.11.11	1.02	1. Changed document name from Product Standards to Datasheet.

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