

Dual N-channel MOSFET

KFCAB21B30L Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: $R_{SS(on)}$ typ = 2.2 m Ω (V_{GS} = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: UP

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

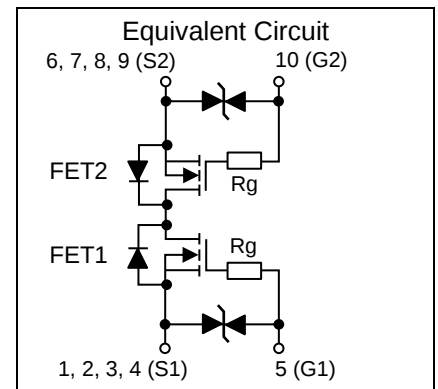
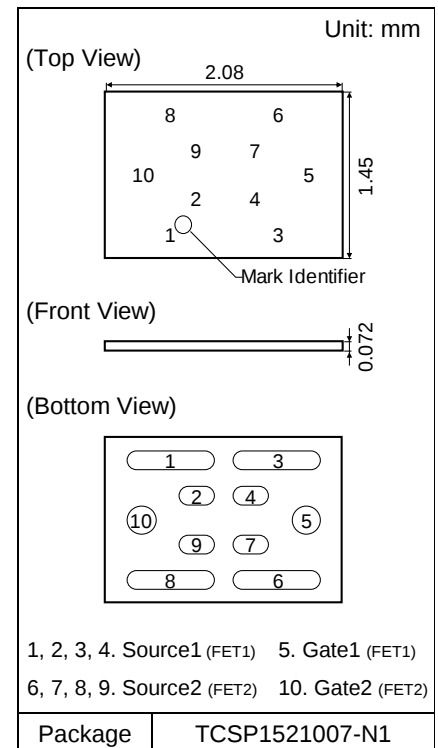
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	± 8	V
Source Current	DC *1	IS1	A
	DC *2	IS2	
	DC *3	IS3	
	Pulsed *4	ISp	
Total Power Dissipation	DC *1	PD1	W
	DC *2	PD2	
	DC *3	PD3	
Operating Junction and Storage Temperature Range	Tj, Tstg	- 55 to + 150	$^\circ\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	205	$^\circ\text{C} / \text{W}$
	Rth2 *2	79	
	Rth3 *3	45	

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (60 mm² area, 36 μm thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (611 mm² area, 36 μm thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$.



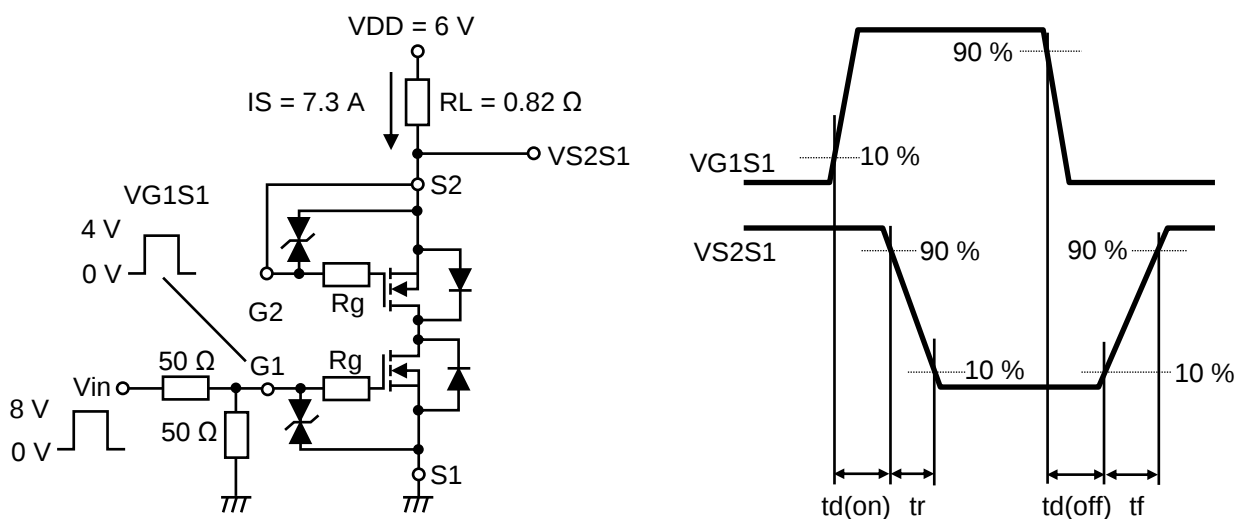
7. ELECTRICAL CHARACTERISTICS $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	$I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	12			V
Zero Gate Voltage Source Current	ISSS	$V_{SS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
Gate-source Leakage Current	IGSS1	$V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$			± 10	μA
	IGSS2	$V_{GS} = \pm 5\text{ V}$, $V_{SS} = 0\text{ V}$			± 1	
Gate-source Threshold Voltage	V_{th}	$I_S = 0.46\text{ mA}$, $V_{SS} = 6\text{ V}$	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	$I_S = 7.3\text{ A}$, $V_{GS} = 4.5\text{ V}$	1.50	2.05	2.70	m Ω
	RSS(on)2	$I_S = 7.3\text{ A}$, $V_{GS} = 3.8\text{ V}$	1.60	2.20	2.85	
	RSS(on)3	$I_S = 7.3\text{ A}$, $V_{GS} = 3.1\text{ V}$	1.75	2.55	3.90	
	RSS(on)4	$I_S = 7.3\text{ A}$, $V_{GS} = 2.5\text{ V}$	2.00	3.30	6.60	
Body Diode Forward Voltage	$V_{F(s-s)}$	$I_F = 7.3\text{ A}$, $V_{GS} = 0\text{ V}$		0.71	1.00	V
Input Capacitance ^{*1}	Ciss	$V_{SS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ kHz}$		3490		pF
Output Capacitance ^{*1}	Coss			425		
Reverse Transfer Capacitance ^{*1}	Crss			360		
Turn-on Delay Time ^{*1, *2}	td(on)	$V_{DD} = 6\text{ V}$, $V_{GS} = 0\text{ to }4\text{ V}$		1.0		μs
Rise Time ^{*1, *2}	tr	$I_S = 7.3\text{ A}$		1.6		
Turn-off Delay Time ^{*1, *2}	td(off)	$V_{DD} = 6\text{ V}$, $V_{GS} = 4\text{ to }0\text{ V}$		6.1		μs
Fall Time ^{*1, *2}	tf	$I_S = 7.3\text{ A}$		2.8		
Total Gate Charge ^{*1}	Qg	$V_{DD} = 6\text{ V}$		32		nC
Gate-source Charge ^{*1}	Qgs	$V_{GS} = 0\text{ to }4\text{ V}$		7		
Gate-drain Charge ^{*1}	Qgd	$I_S = 14.6\text{ A}$		6		
Gate Resistance ^{*1}	Rg	$f = 1\text{ MHz}$	400	700	1000	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

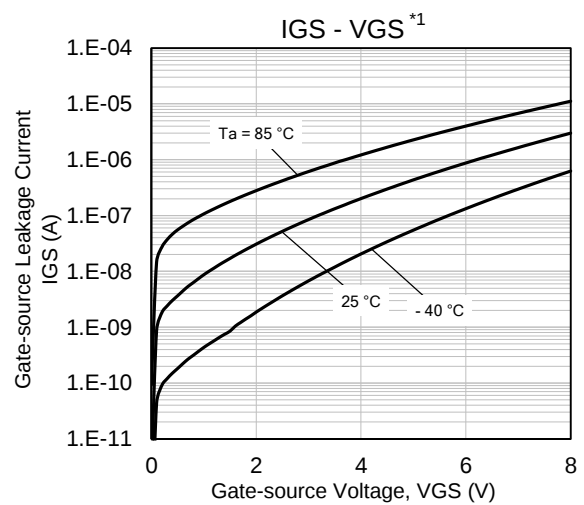
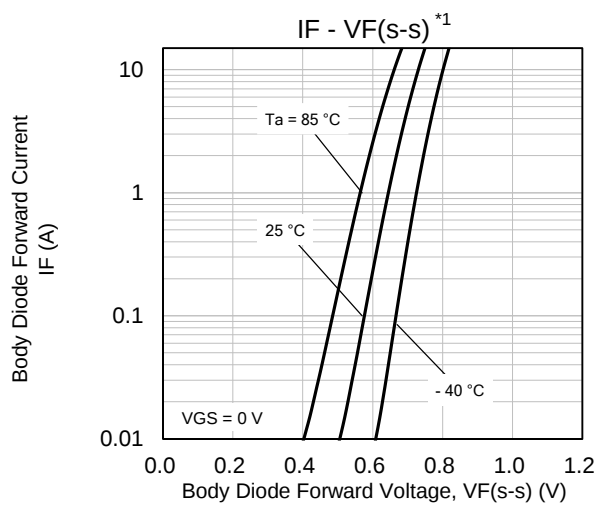
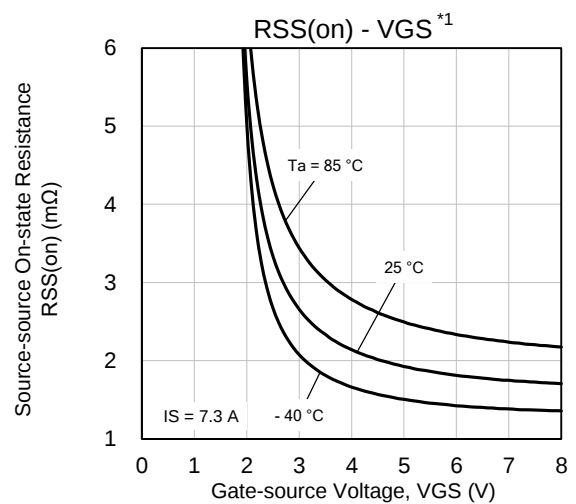
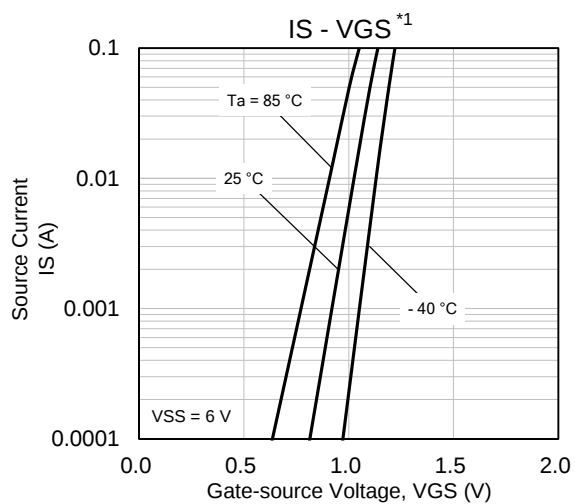
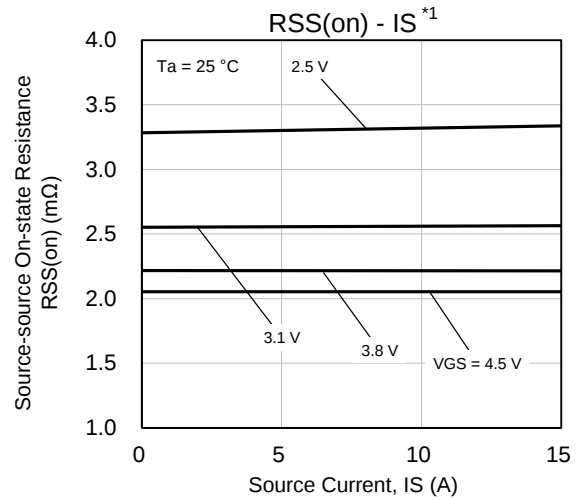
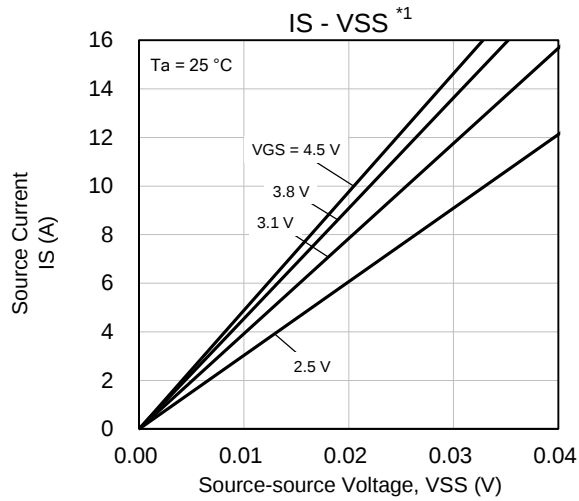
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



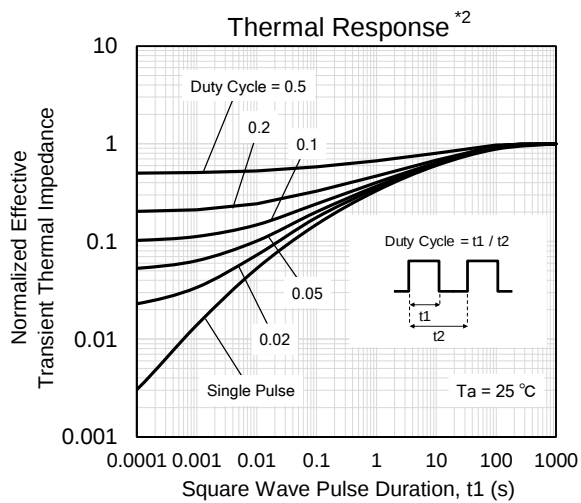
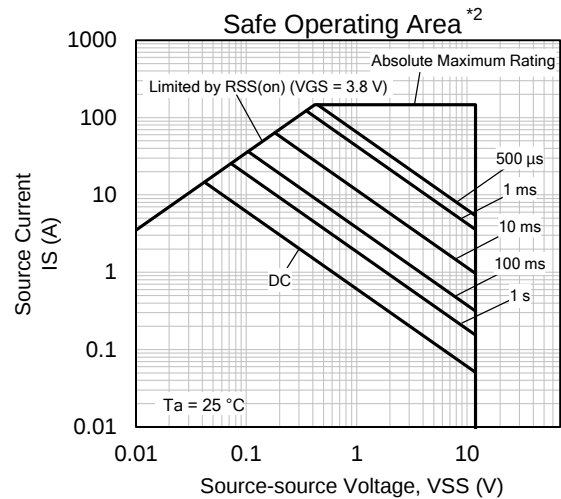
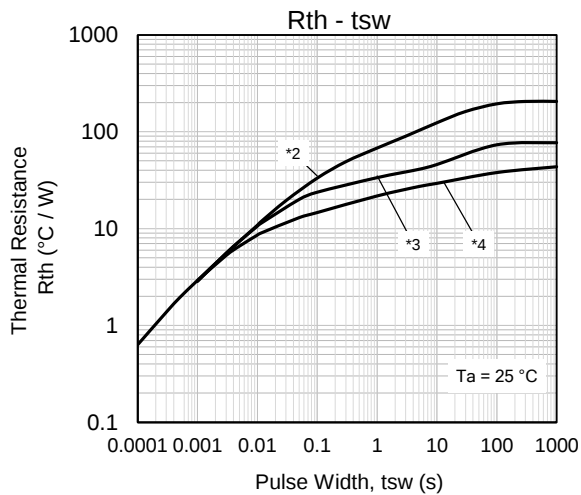
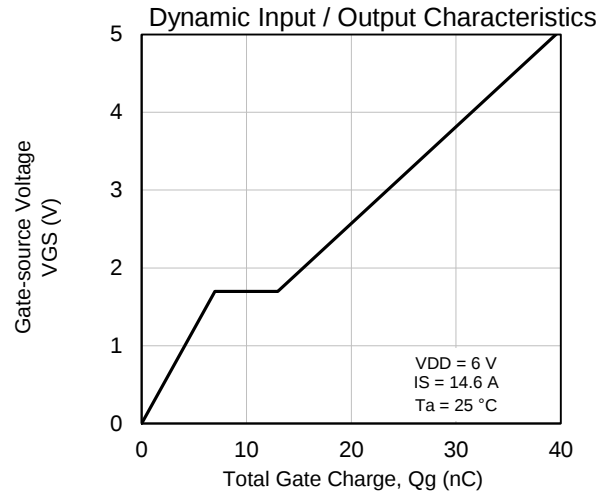
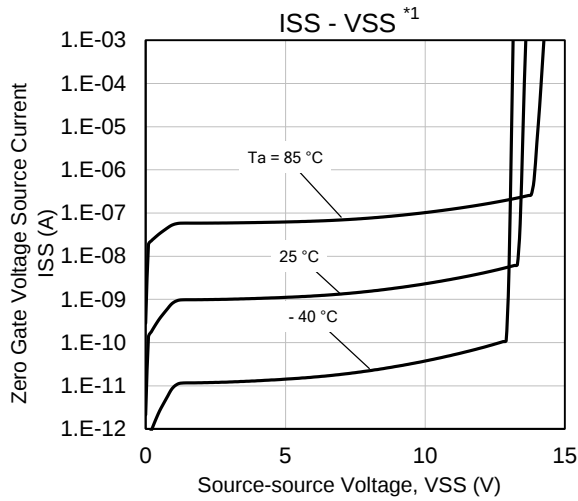
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	$C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$	H2	$> 2\text{ to } \leq 4$	kV

9. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



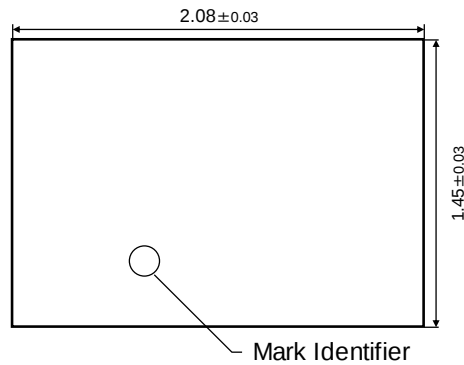
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm). FR4 board partially covered with copper pad (60 mm² area, 36 µm thickness).
- *3 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm). FR4 board fully covered with copper pad (611 mm² area, 36 µm thickness).
- *4 Mounted on ceramic board (70 mm × 70 mm × t1.0 mm).

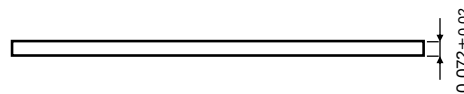
10. OUTLINE

(Top View)

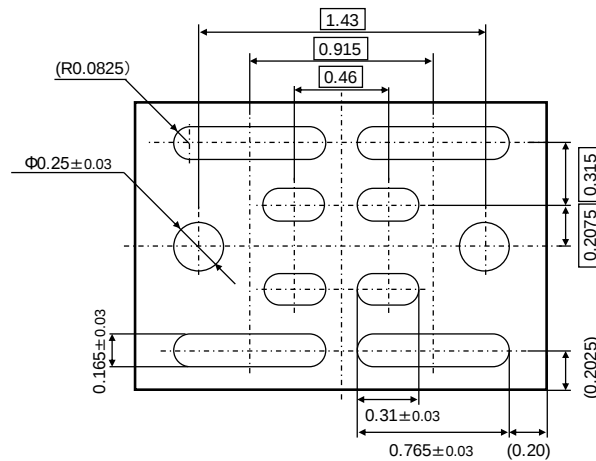
Unit: mm



(Front View)



(Bottom View)

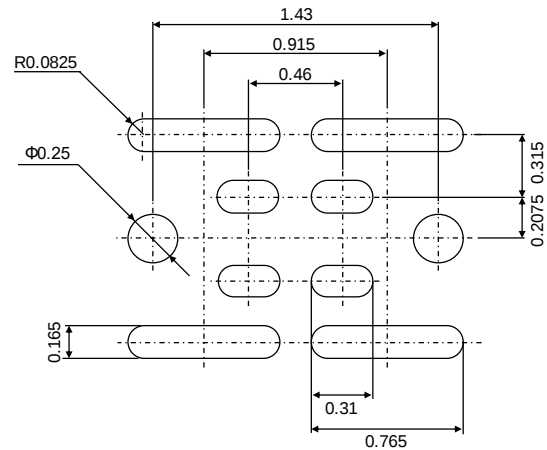
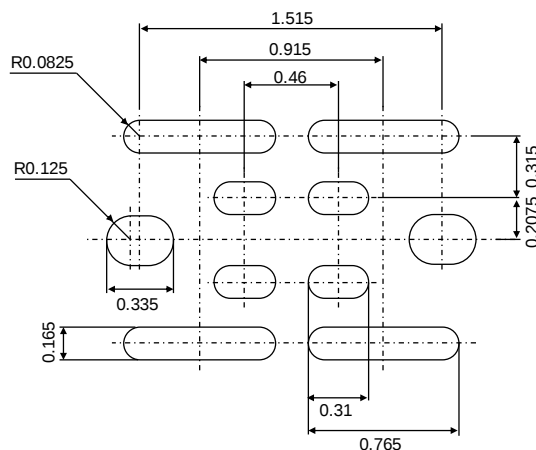


11. LAND & STENCIL PATTERN (Reference)

LAND

STENCIL

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.9.16	1.00	1. Initially issued.

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