

## Dual N-channel MOSFET

# KFCAB22075NL Datasheet

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## 1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

## 2. FEATURES

- Source-source On-state Resistance:  $R_{SS(on)}$  typ = 1.65 m $\Omega$  ( $V_{GS}$  = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

## 3. MARKING SYMBOL: KL

## 4. PACKAGING

Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

## 5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

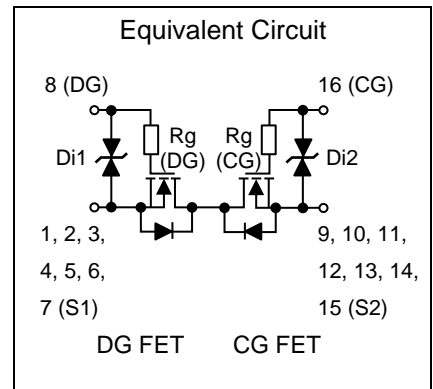
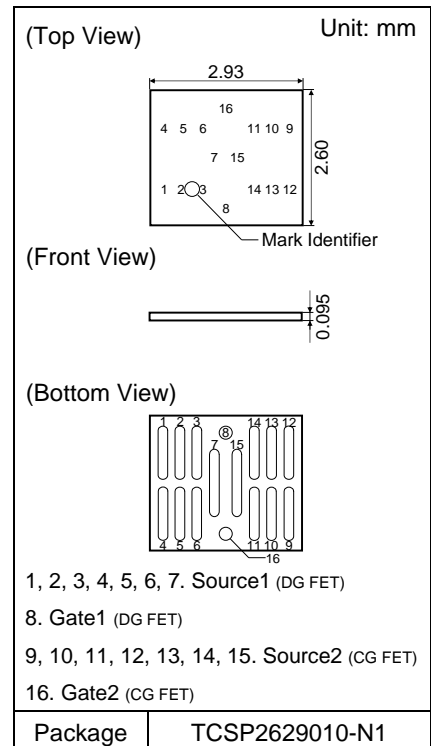
(MOSFET: CG FET, DG FET)

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	22	V
Gate-source Voltage		VGS	$\pm 12$	V
Source Current	DC *1	IS1	17.6	A
	DC *2	IS2	31.6	
	DC *3	IS3	42.9	
	Pulsed *4	ISp	176	
Body Diode Forward Current	DC *1	IF1	1.2	A
	DC *2	IF2	3.5	
	DC *3	IF3	6.2	
Total Power Dissipation	DC *1	PD1	0.59	W
	DC *2	PD2	1.90	
	DC *3	PD3	3.50	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	$^\circ\text{C}$

## 6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1, 2	211	$^\circ\text{C} / \text{W}$
	Rth2 *1, 3	66	
	Rth3 *1, 4	35	

- Note \*1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board partially covered with copper pad (41 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
- \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board fully covered with copper pad (612 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
- \*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
- \*4 t = 10  $\mu\text{s}$ , Duty Cycle  $\leq 1\%$ .



## 7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

(MOSFET: CG FET, DG FET)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	22			V
Zero Gate Voltage Source Current	ISSS	VSS = 22 V, VGS = 0 V			1	$\mu\text{A}$
Gate-source Leakage Current	IGSS1	VGS = $\pm 8\text{ V}$ , VSS = 0 V			$\pm 0.5$	$\mu\text{A}$
	IGSS2	VGS = $\pm 5\text{ V}$ , VSS = 0 V			$\pm 0.1$	
Gate-source Threshold Voltage	Vth	IS = 1.43 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 8.8 A, VGS = 4.5 V	1.30	1.60	1.85	m $\Omega$
	RSS(on)2	IS = 8.8 A, VGS = 3.8 V	1.35	1.65	1.90	
	RSS(on)3	IS = 8.8 A, VGS = 3.1 V	1.40	1.80	2.55	
	RSS(on)4	IS = 8.8 A, VGS = 2.5 V	1.45	2.10	4.20	
Body Diode Forward Voltage	VF(s-s)	IF = 8.8 A, VGS = 0 V		0.70	0.82	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz	5800	8250	10750	pF
Output Capacitance *1	Coss			660		
Reverse Transfer Capacitance *1	Crss			610		
Total Gate Charge *1	Qg	VDD = 10 V		74		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		14		
Gate-drain Charge *1	Qgd	IS = 17.6 A		17		

(MOSFET: CG FET)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on Delay Time *1, *2	td(on)1	VDD = 10 V, VGS = 0 to 4 V		0.08		$\mu\text{s}$
Rise Time *1, *2	tr1	IS = 8.8 A		0.20		
Turn-off Delay Time *1, *2	td(off)1	VDD = 10 V, VGS = 4 to 0 V		0.80		$\mu\text{s}$
Fall Time *1, *2	tf1	IS = 8.8 A		0.37		
Gate Resistance *1	Rg(CG)	f = 1 MHz	1	5	9	$\Omega$

(MOSFET: DG FET)

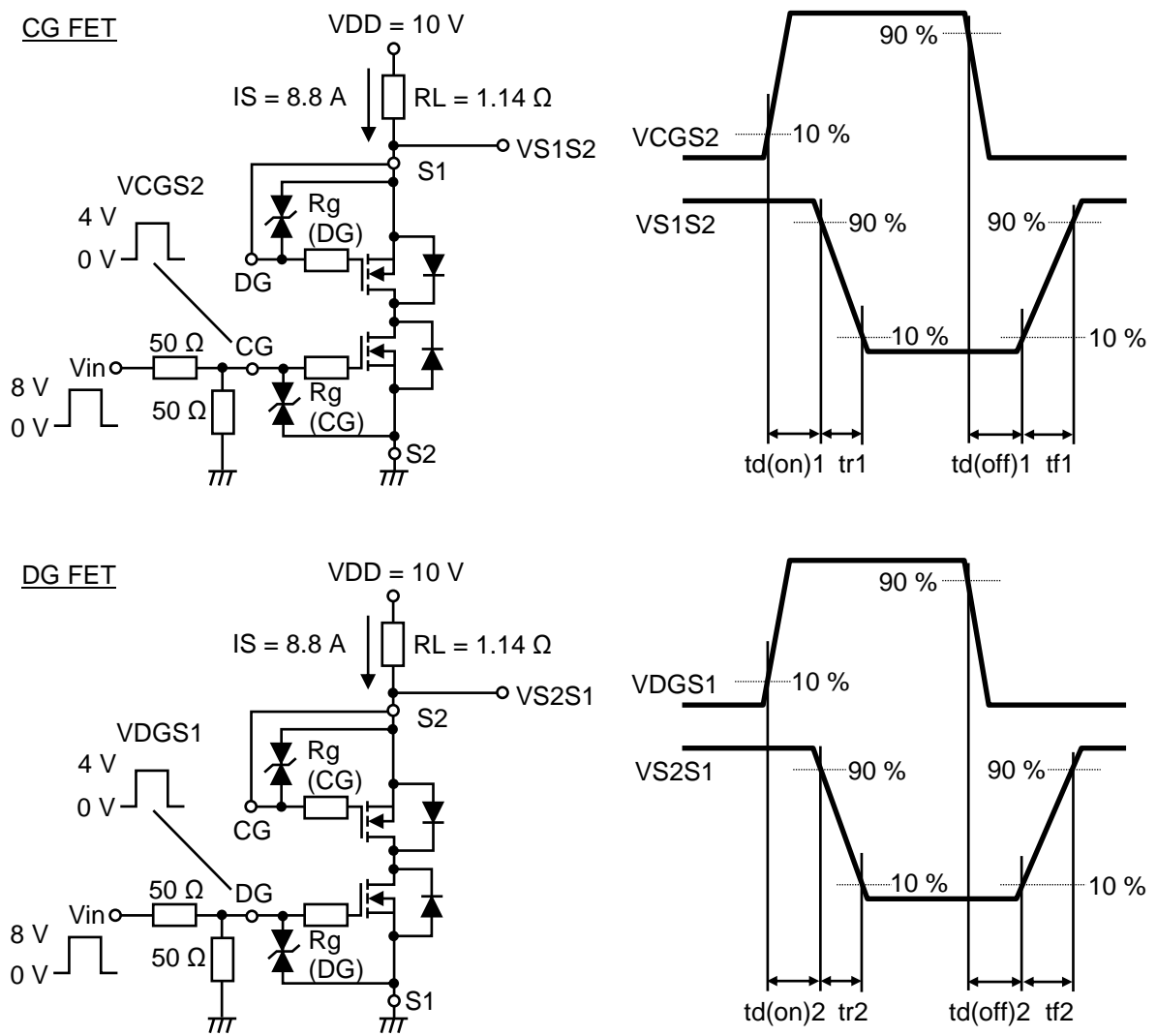
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on Delay Time *1, *2	td(on)2	VDD = 10 V, VGS = 0 to 4 V		2.0		$\mu\text{s}$
Rise Time *1, *2	tr2	IS = 8.8 A		2.9		
Turn-off Delay Time *1, *2	td(off)2	VDD = 10 V, VGS = 4 to 0 V		14		$\mu\text{s}$
Fall Time *1, *2	tf2	IS = 8.8 A		6.6		
Gate Resistance *1	Rg(DG)	f = 1 MHz	400	700	1000	$\Omega$

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\*1 Guaranteed by design, not subject to production testing.

\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

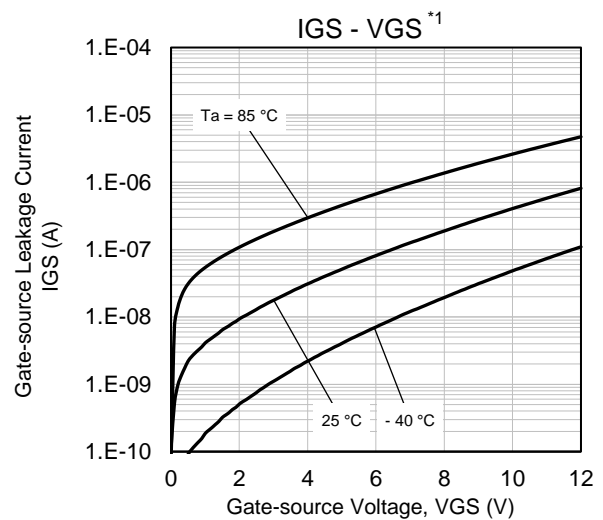
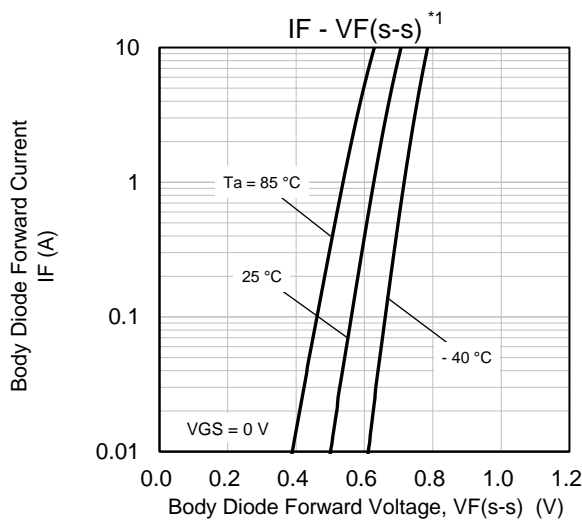
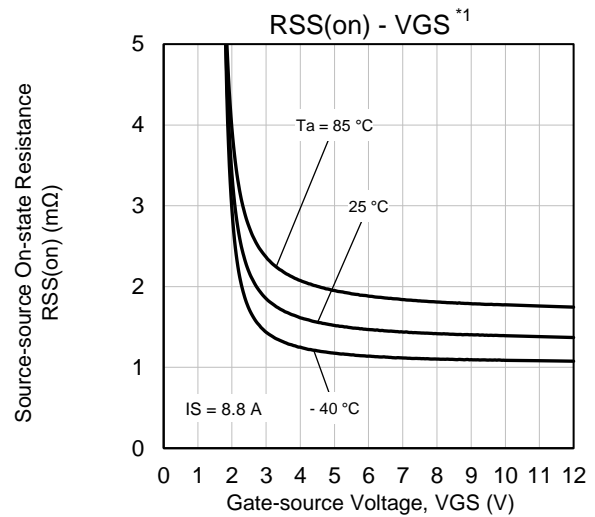
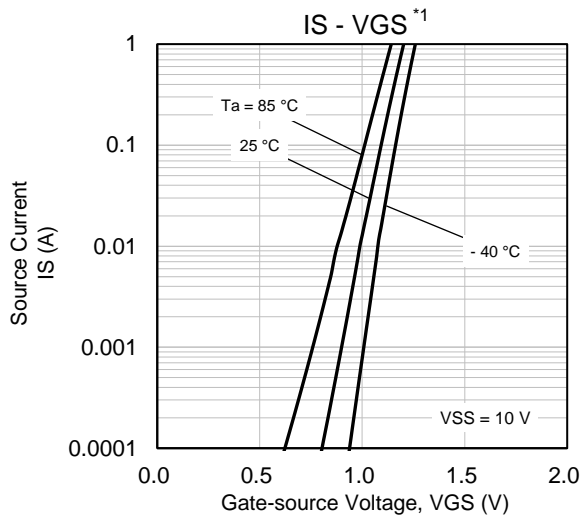
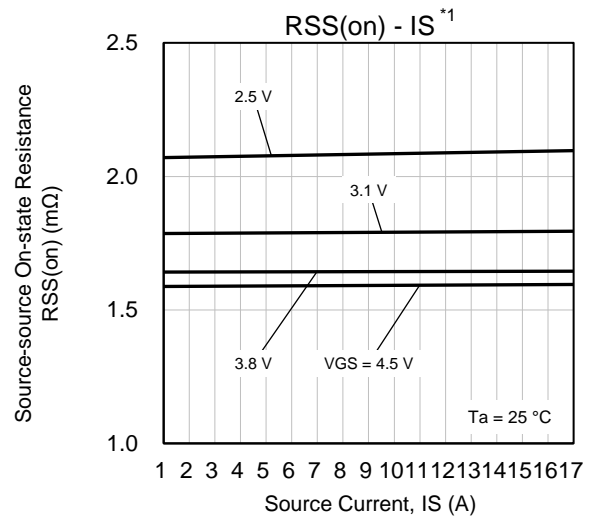
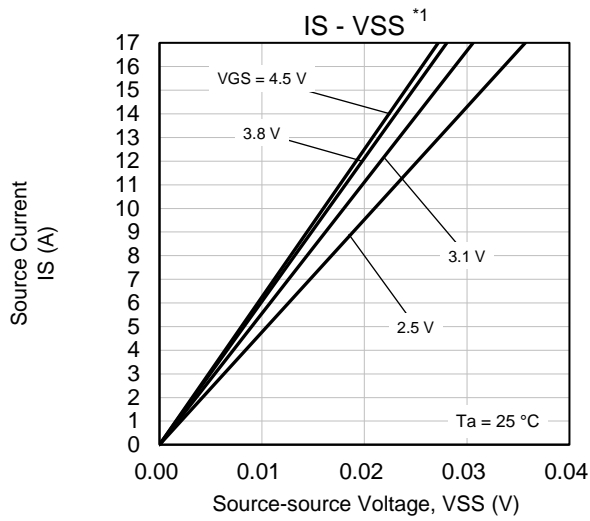
■ Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



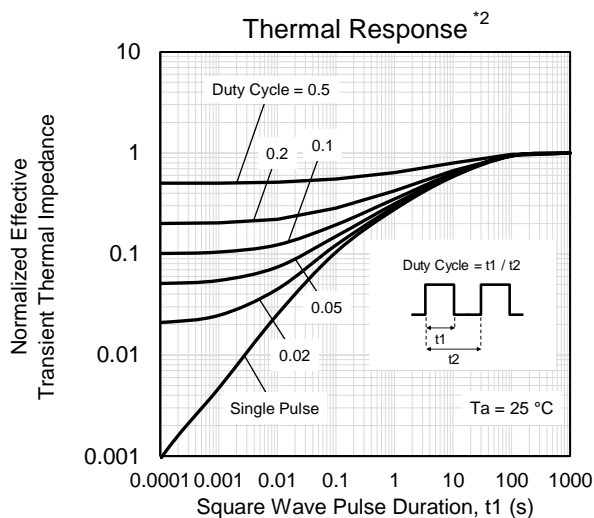
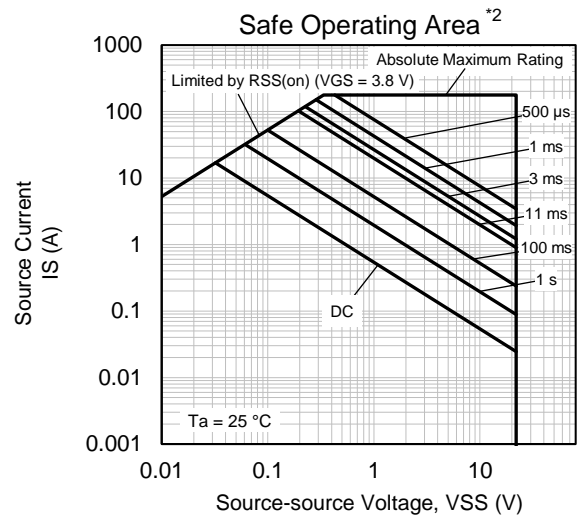
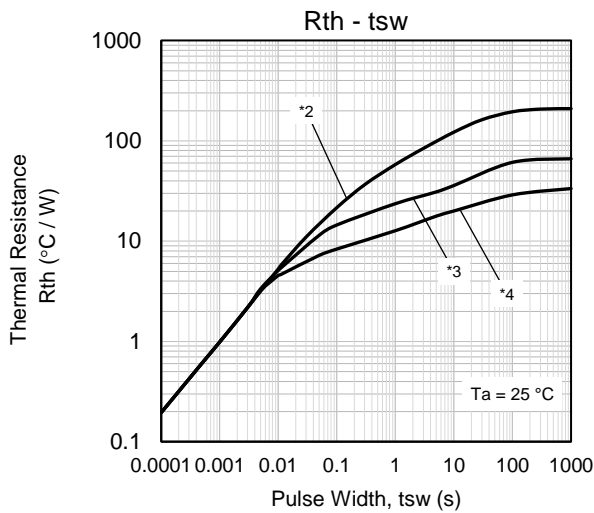
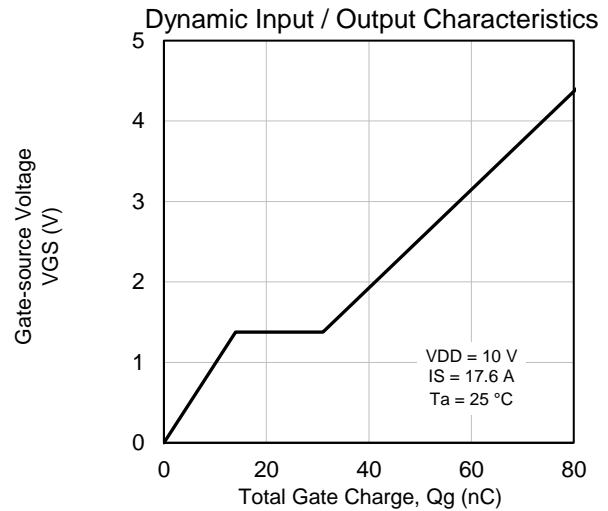
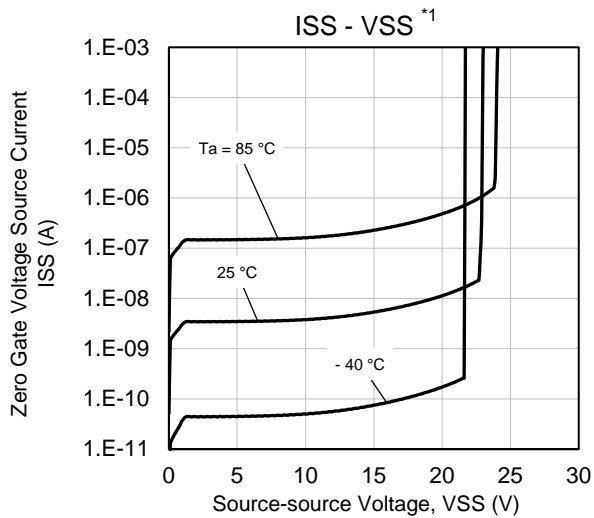
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC    Ta = 25 °C ± 3 °C

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H1C	> 1k to ≤ 2k	V

## 9. TECHNICAL DATA (Reference)



## TECHNICAL DATA (Reference)



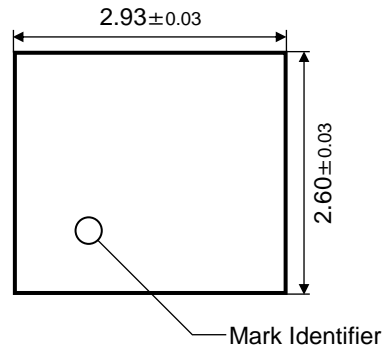
### Note

- \*1 Pulse measurement.
- \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board partially covered with copper pad  
(41 mm<sup>2</sup> area, 36 µm thickness).
- \*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board fully covered with copper pad  
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- \*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

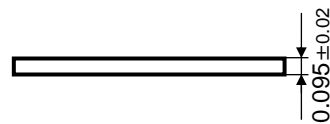
## 10. OUTLINE

(Top View)

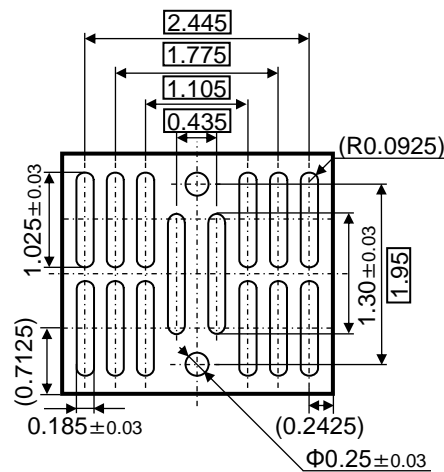
Unit: mm



(Front View)

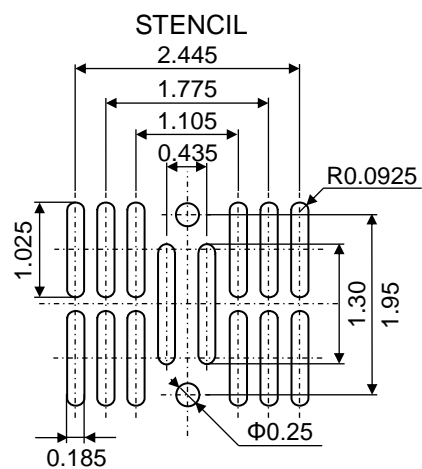
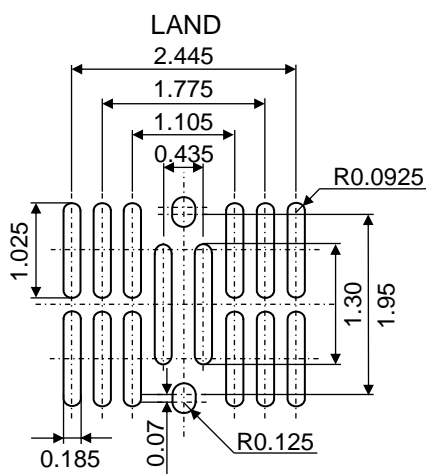


(Bottom View)



## 11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2025.3.5	1.00	1. Initially issued.



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