#### **Dual N-channel MOSFET**

# **KFC4B12070NL Datasheet**

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### 1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

#### 2. FEATURES

- Source-source On-state Resistance: RSS(on) typ = 25 m $\Omega$  (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

#### 3. MARKING SYMBOL: KU

#### 4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

#### 5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

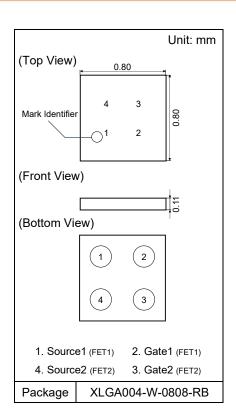
Parameter		Symbol	Rating	Unit	
Source-source Voltage		VSS	12	V	
Gate-source Voltage		VGS	± 8	V	
	DC *1	IS1	3.1		
Source Current	DC *2	IS2	5.4	۸	
	DC *3	IS3	6.6	Α	
	Pulsed *4	ISp	31		
	DC *1	PD1	0.34		
Total Power Dissipation	DC *2	PD2	1.00	W	
	DC *3	PD3	1.50		
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C	

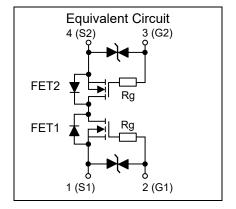
#### 6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
	Rth1 *1	368	
Thermal Resistance (ch-a)	Rth2 *2	125	°C / W
	Rth3 *3	84	

Note \*1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (19 mm² area, 36 µm thickness).

- \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (615 mm² area, 36 µm thickness).
- \*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
- \*4  $t = 10 \mu s$ , Duty Cycle  $\leq 1 \%$ .





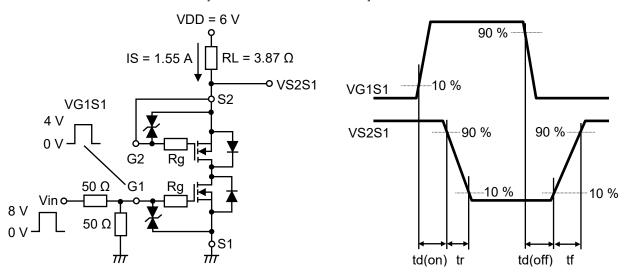
# B12070NL DATASHEET

#### 7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit	
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V	
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1	μA	
Cata aguiras Lagkaga Current	IGSS1	VGS = ± 8 V, VSS = 0 V			± 5		
Gate-source Leakage Current	IGSS2	VGS = ± 5 V, VSS = 0 V			± 0.5	μA	
Gate-source Threshold Voltage	Vth	IS = 0.05 A, VSS = 6 V	0.35	0.90	1.40	V	
	RSS(on)1	IS = 1.55 A, VGS = 4.5 V	21	24	31		
Sauras asuras On atata Basistanas	RSS(on)2	IS = 1.55 A, VGS = 3.8 V	22	25	34	0	
Source-source On-state Resistance	RSS(on)3	IS = 1.55 A, VGS = 3.1 V	25	29	43	mΩ	
	RSS(on)4	IS = 1.55 A, VGS = 2.5 V	26	36	83		
Body Diode Forward Voltage	VF(s-s)	IF = 1.55 A, VGS = 0 V		0.7	1.0	V	
Input Capacitance *1	Ciss			390			
Output Capacitance *1	Coss	VSS = 10 V, VGS = 0 V, f = 1 kHz		84		pF	
Reverse Transfer Capacitance *1	Crss			70			
Turn-on Delay Time *1,*2	td(on)	VDD = 6 V, VGS = 0 to 4 V		0.2			
Rise Time *1, *2	tr	IS = 1.55 A		0.3		μs	
Turn-off Delay Time *1, *2	td(off)	VDD = 6 V, VGS = 4 to 0 V		1.2			
Fall Time *1, *2	tf	IS = 1.55 A		0.7		μs	
Total Gate Charge *1	Qg	VDD = 6 V		4.3			
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		0.9		nC	
Gate-drain Charge *1	Qgd	IS = 3.1 A		1.1			
Gate Resistance *1	Rg	f = 1 MHz	600	1000	1400	Ω	

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

- \*1 Guaranteed by design, not subject to production testing.
- \*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



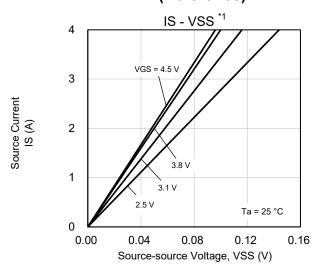
#### 8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

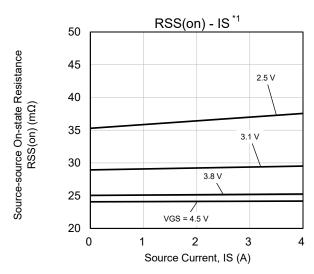
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H2	> 2k to ≤ 4k	V

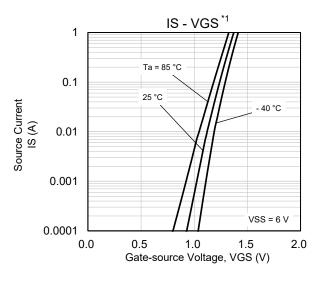


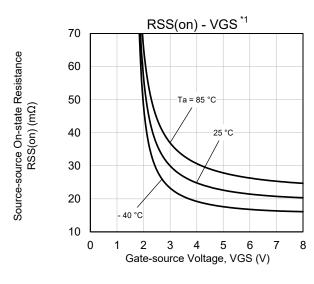
#### 9. TECHNICAL DATA (Reference)

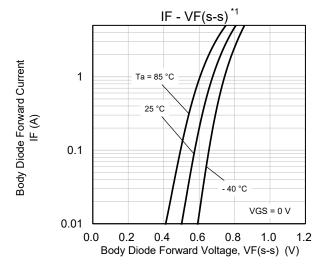
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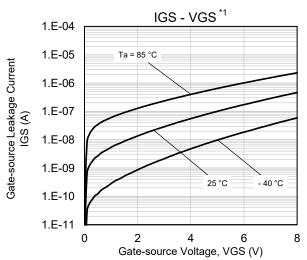








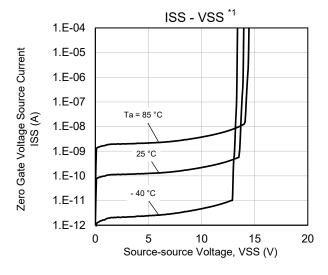


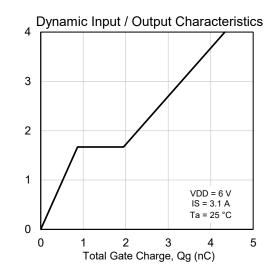


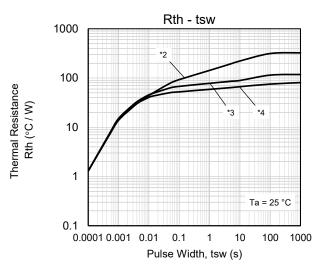
Gate-source Voltage VGS (V)

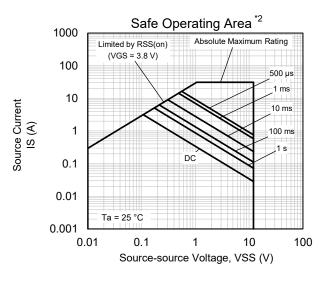


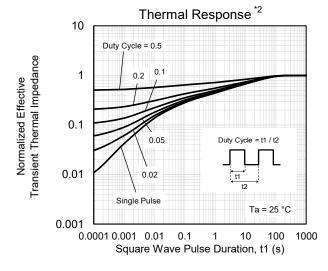
#### **TECHNICAL DATA (Reference)**











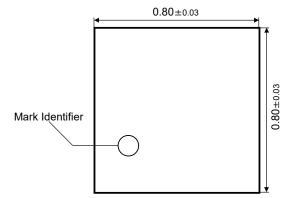
#### Note

- \*1 Pulse measurement.
- \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (19 mm² area, 36 µm thickness).
- \*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (615 mm² area, 36 μm thickness).
- \*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

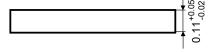
Unit: mm

#### 10. OUTLINE

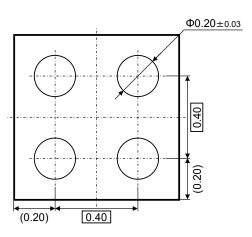
(Top View)



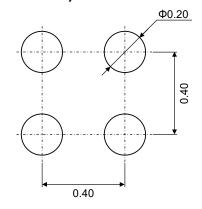
(Front View)



(Bottom View)



#### 11. LAND & STENCIL PATTERN (Reference)



Unit: mm

#### Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

#### 12. REVISION HISTORY

Date	Revision	Description
2024.2.6	1.00	1. Initially issued.
2025.3.14	2.00	Updated MARKING SYMBOL.
		2. Updated ELECTRICAL CHARACTERISTICS.
		3. Added TECHNICAL DATA.
2025.7.7	2.01	1. Changed Package.



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