

Dual N-channel MOSFET

KFC6B21B70L

Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: $R_{SS(on)}$ typ = 4.6 m Ω (V_{GS} = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: X7

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

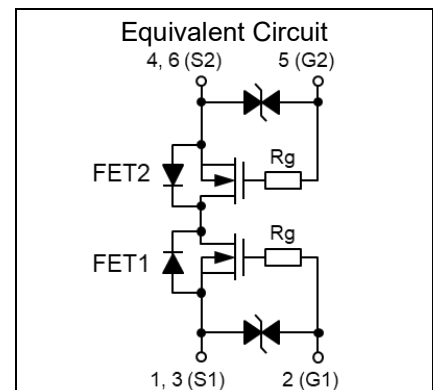
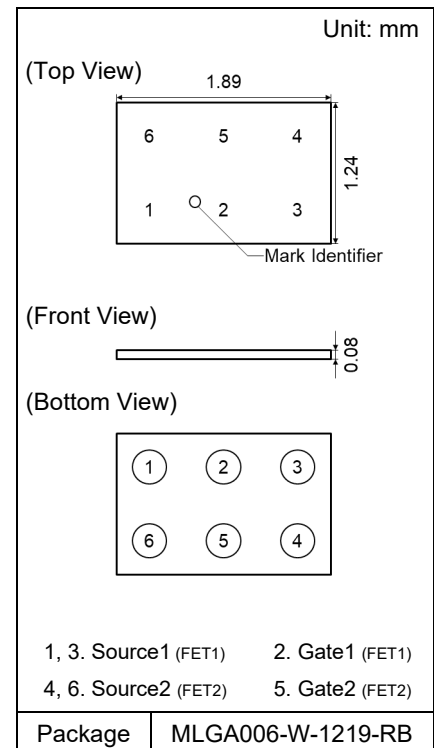
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	12	V
Gate-source Voltage		VGS	± 10.5	V
Source Current	DC ^{*1}	IS1	9.0	A
	DC ^{*2}	IS2	15.1	
	DC ^{*3}	IS3	19.4	
	Pulsed ^{*4}	ISp	90	
Total Power Dissipation	DC ^{*1}	PD1	0.50	W
	DC ^{*2}	PD2	1.40	
	DC ^{*3}	PD3	2.60	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 ^{*1}	250	°C / W
	Rth2 ^{*2}	89	
	Rth3 ^{*3}	48	

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (22 mm² area, 36 μm thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (598 mm² area, 36 μm thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$.



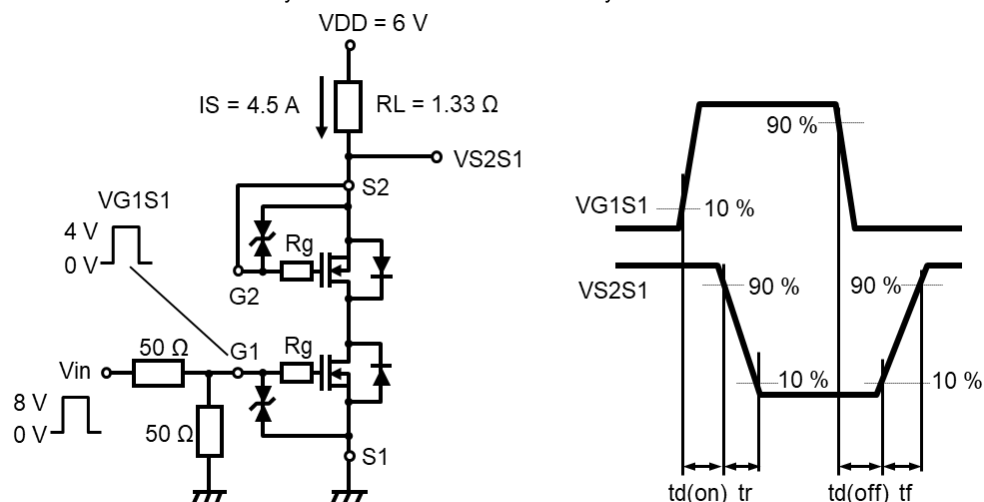
7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	$I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	12			V
Zero Gate Voltage Source Current	ISSS	$V_{SS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
Gate-source Leakage Current	IGSS1	$V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$			± 10	μA
	IGSS2	$V_{GS} = \pm 5\text{ V}$, $V_{SS} = 0\text{ V}$			± 1	
Gate-source Threshold Voltage	V _{th}	$I_S = 0.26\text{ mA}$, $V_{SS} = 6\text{ V}$	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	$I_S = 4.5\text{ A}$, $V_{GS} = 4.5\text{ V}$	2.9	4.2	5.5	m Ω
	RSS(on)2	$I_S = 4.5\text{ A}$, $V_{GS} = 3.8\text{ V}$	3.2	4.6	6.1	
	RSS(on)3	$I_S = 4.5\text{ A}$, $V_{GS} = 3.1\text{ V}$	3.4	5.4	7.8	
	RSS(on)4	$I_S = 4.5\text{ A}$, $V_{GS} = 2.5\text{ V}$	4.4	7.4	13.8	
Body Diode Forward Voltage	V _{F(s-s)}	$I_F = 4.5\text{ A}$, $V_{GS} = 0\text{ V}$		0.7	1.0	V
Input Capacitance ^{*1}	C _{iss}	$V_{SS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ kHz}$		1810		pF
Output Capacitance ^{*1}	C _{oss}			300		
Reverse Transfer Capacitance ^{*1}	C _{rss}			240		
Turn-on Delay Time ^{*1,*2}	t _{d(on)}	$V_{DD} = 6\text{ V}$, $V_{GS} = 0\text{ to }4\text{ V}$		2.1		μs
Rise Time ^{*1,*2}	t _r	$I_S = 4.5\text{ A}$		3.1		
Turn-off Delay Time ^{*1,*2}	t _{d(off)}	$V_{DD} = 6\text{ V}$, $V_{GS} = 4\text{ to }0\text{ V}$		8.8		μs
Fall Time ^{*1,*2}	t _f	$I_S = 4.5\text{ A}$		4.8		
Total Gate Charge ^{*1}	Q _g	$V_{DD} = 6\text{ V}$		15		nC
Gate-source Charge ^{*1}	Q _{gs}	$V_{GS} = 0\text{ to }4\text{ V}$		4.1		
Gate-drain Charge ^{*1}	Q _{gd}	$I_S = 9.0\text{ A}$		3.3		
Gate Resistance ^{*1}	R _g	$f = 1\text{ MHz}$	1100	2000	2900	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

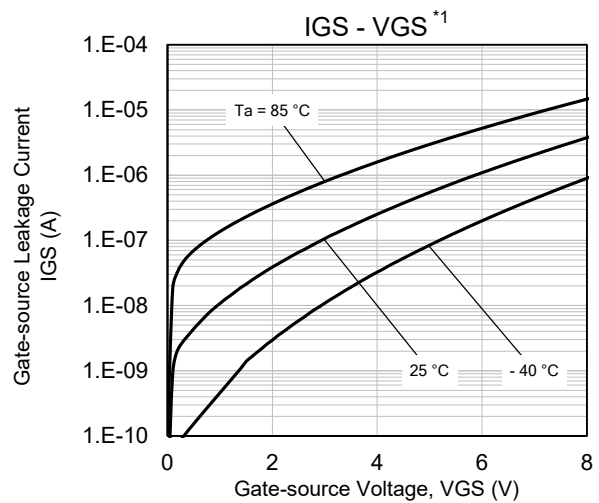
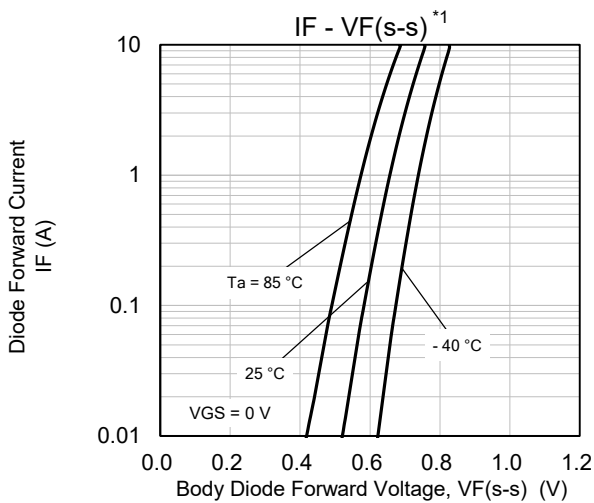
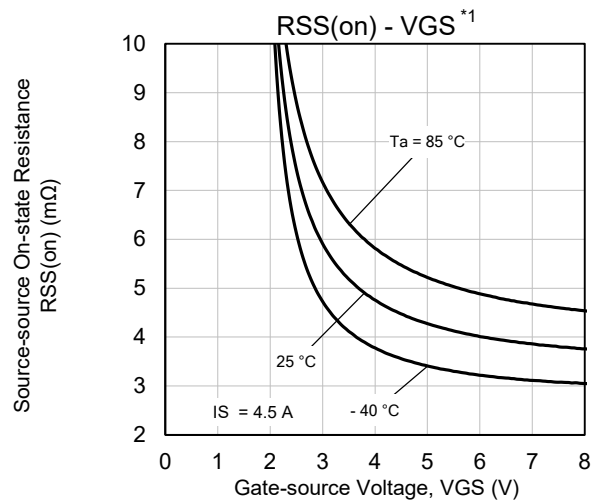
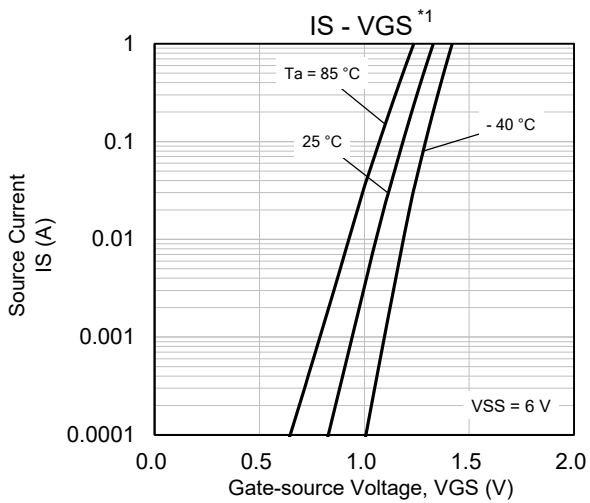
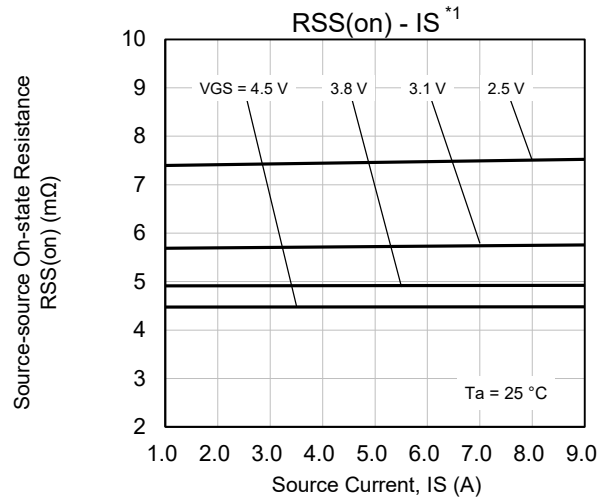
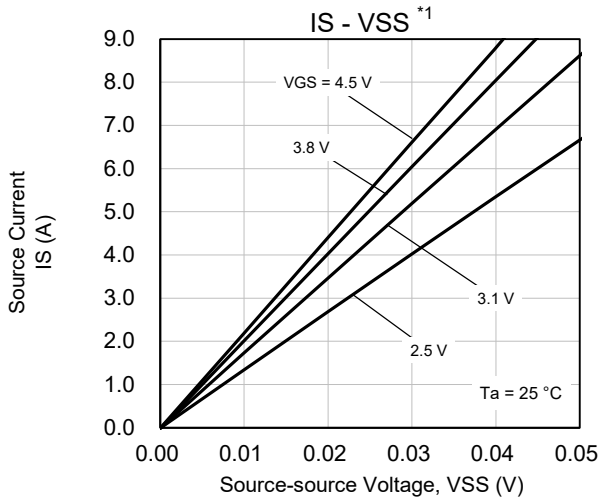
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



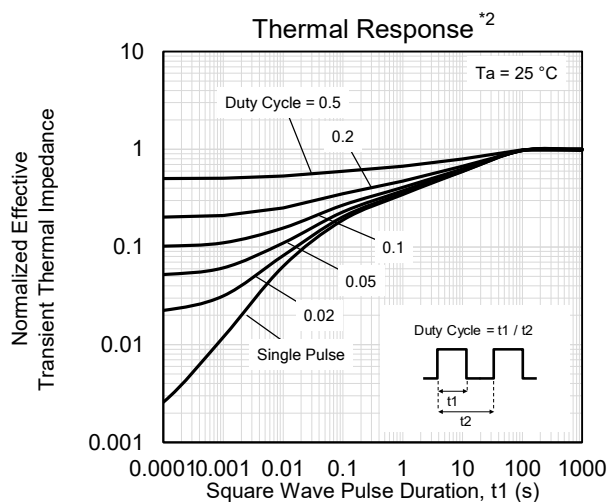
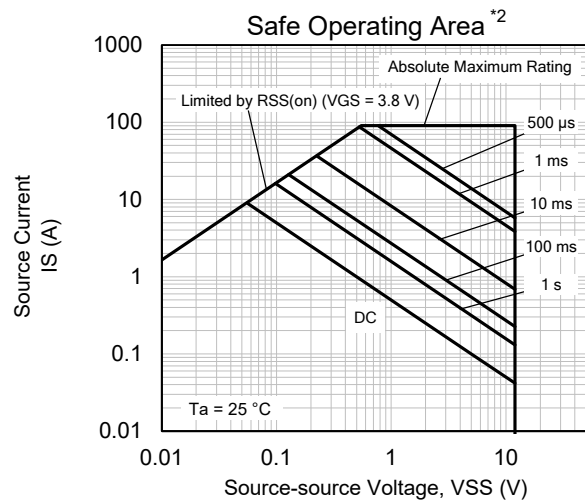
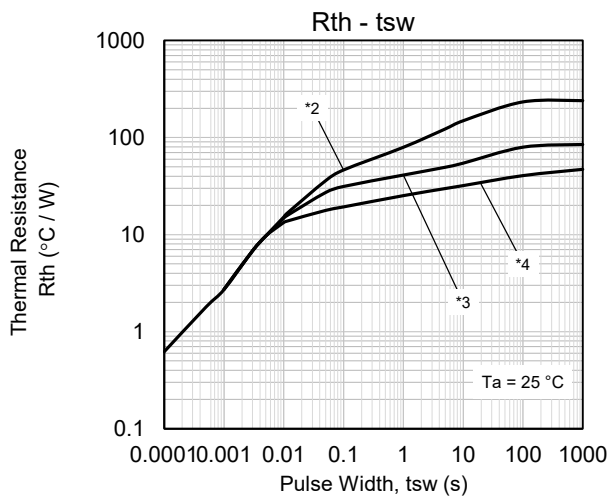
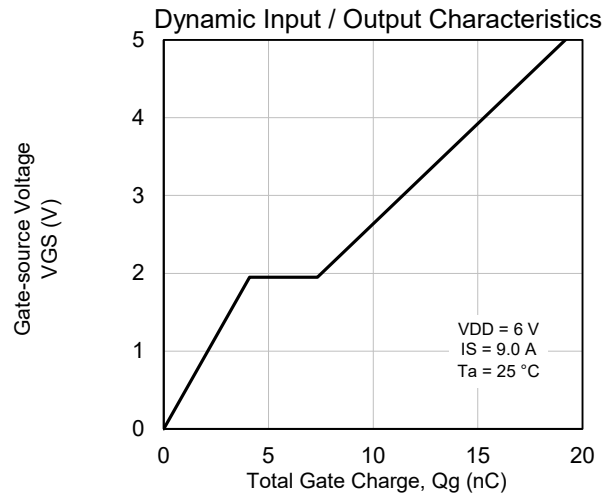
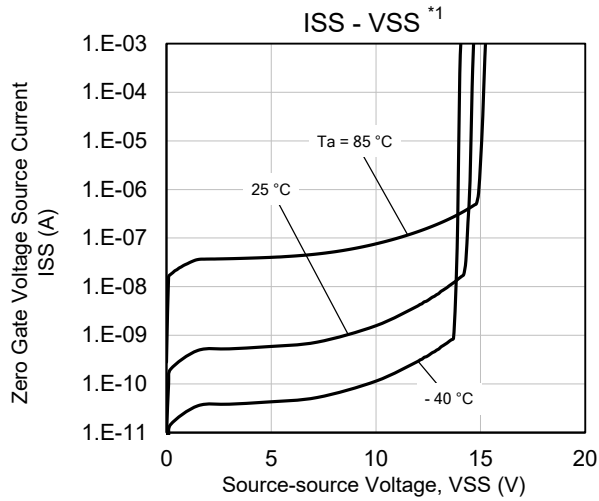
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	$C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$	H2	$> 2\text{ to } \leq 4$	kV

9. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



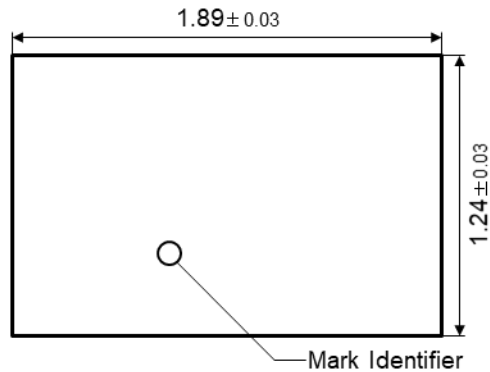
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad
(22 mm² area, 36 μm thickness).
- *3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
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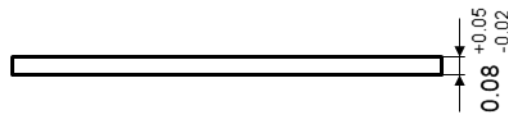
10. OUTLINE

(Top View)

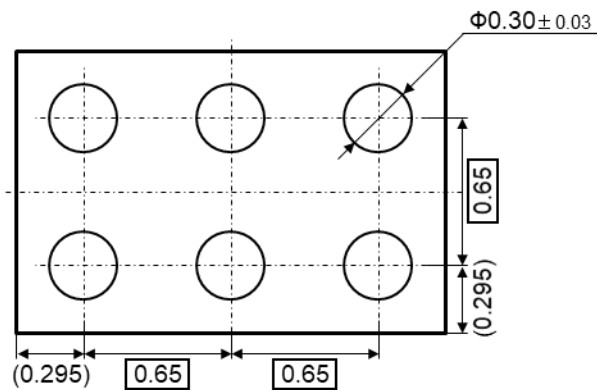
Unit: mm



(Front View)

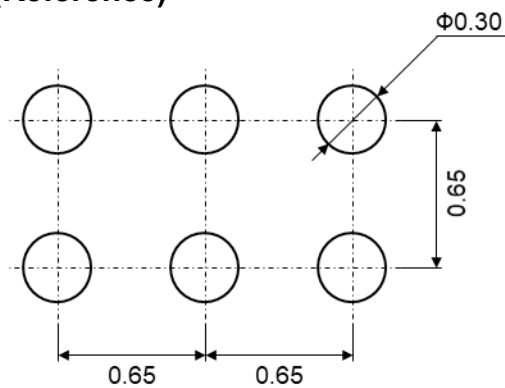


(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2023.8.9	1.00	1. Initially issued.

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