

Dual N-channel MOSFET

KFC7P23440L Datasheet

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1. GENERAL DESCRIPTION

Dual N-channel MOSFET

For lithium-ion secondary battery protection circuits

For load switching

2. FEATURES

- Low source-source ON Resistance: $R_{SS(on)}$ typ. = 2.0 m Ω (V_{GS} = 10 V)
- Low threshold voltage: 4.5 V drive
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL: Level 1)
- Metal package with enhanced thermal conduction design
- Minimized the junction to foot thermal resistance
- Compatible with conventional SMT assembly and test techniques

3. MARKING SYMBOL: AC

4. PACKAGING

Embossed type (Thermo-compression sealing): 6,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	30	V
Gate-source Voltage	VGS	± 20	
Source Current	DC *1	IS1	A
	DC *2	IS2	
	Pulsed *3	ISp	
Total Power Dissipation	DC *1	PD1	W
	DC *2	PD2	
Channel Temperature	Tch	150	$^\circ\text{C}$
Storage Temperature Range	Tstg	-55 to +150	

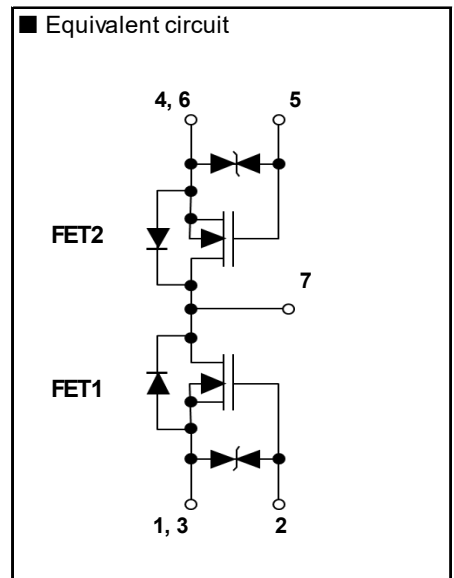
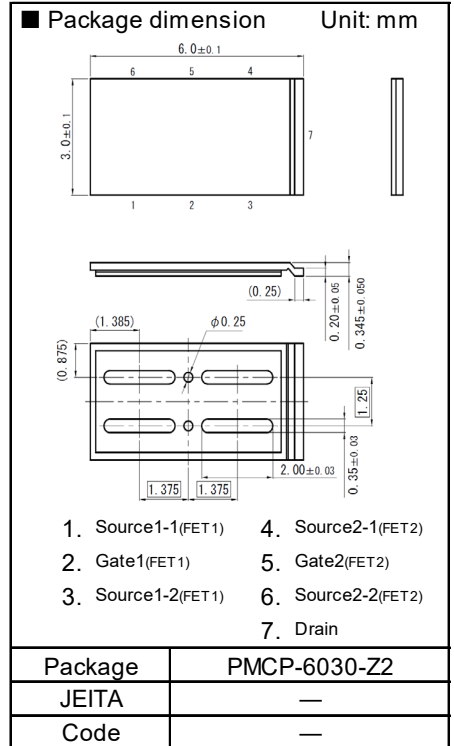
6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter			Symbol	Rating	Unit
Thermal Resistance	Junction to Ambient	DC *1	Rθja1	125	°C / W
		DC *2	Rθja2	52	

Note *1 Mounted on FR4 board (25.4mm x 25.4mm x t1.0mm) using the minimum recommended pad size (36 μm Copper).

*2 Mounted on FR4 board (25.4mm x 25.4mm x t1.0mm) coated with copper foil $\geq 500 \text{ mm}^2$ (36 μm Copper).

*3 $t = 10\mu\text{s}$, Duty Cycle $\leq 1\%$



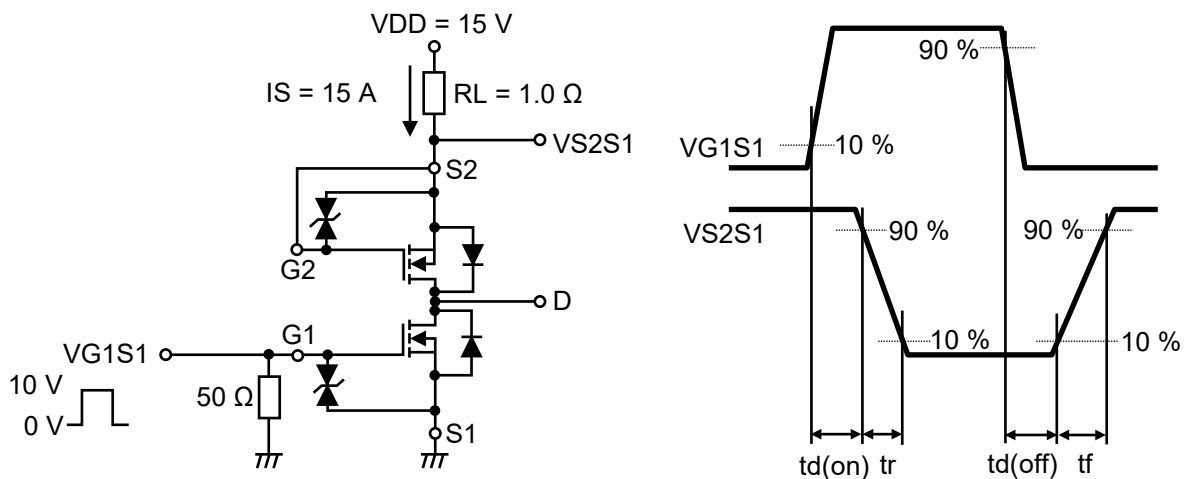
7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Source Current	ISSS	VSS = 30 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ± 20 V, VSS = 0 V			± 10	μA
Gate-source Threshold Voltage	Vth	IS = 2.68 mA, VSS = 10 V	1.0	2.0	3.0	V
Source-source On-state Resistance	RSS(on)1	IS = 15 A, VGS = 10 V	1.2	2.0	2.6	m Ω
	RSS(on)2	IS = 15 A, VGS = 8.0 V	1.3	2.2	3.3	
	RSS(on)3	IS = 15 A, VGS = 4.5 V	2.0	3.4	5.1	
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 MHz		4800		pF
Output Capacitance *1	Coss			690		
Reverse Transfer Capacitance *1	Crss			440		
Turn-on Delay Time *1,*2	td(on)	VDD = 15 V, VGS = 0 to 10 V IS = 15 A		75		ns
Rise Time *1,*2	tr			430		
Turn-off Delay Time *1,*2	td(off)	VDD = 15 V, VGS = 10 to 0 V IS = 15 A		220		ns
Fall Time *1,*2	tf			170		
Total Gate Charge *1	Qg	VDD = 15 V VGS = 0 to 10 V IS = 30 A		85		nC
Gate-source Charge *1	Qgs			15		
Gate-drain Charge *1	Qgd			10		
Body Diode Forward Voltage	VF(S-S)	IF = 15 A, VGS = 0 V		0.8	1.2	V

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

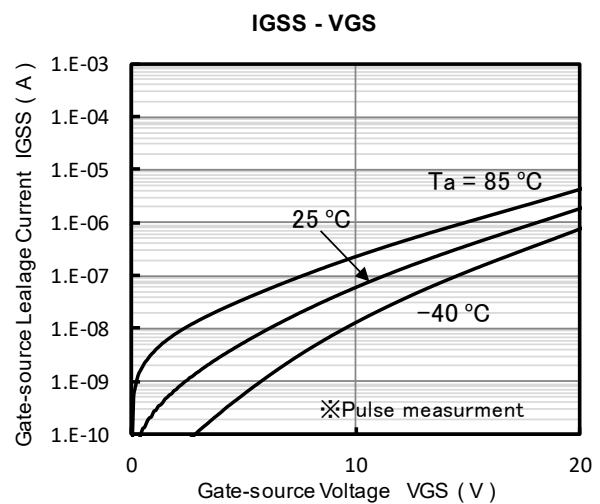
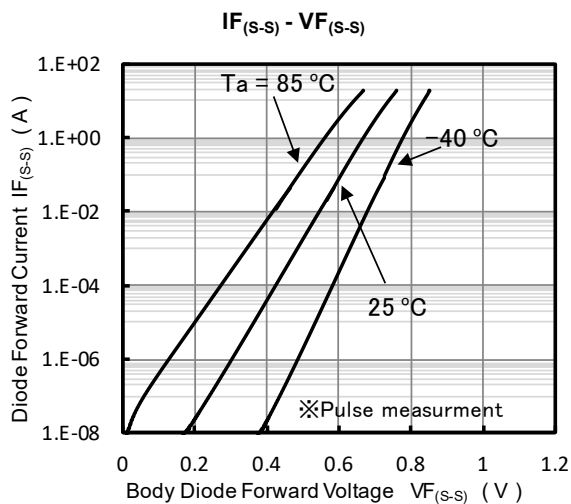
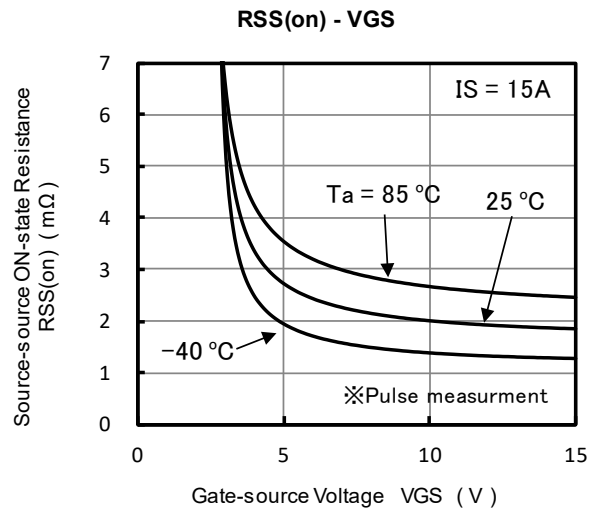
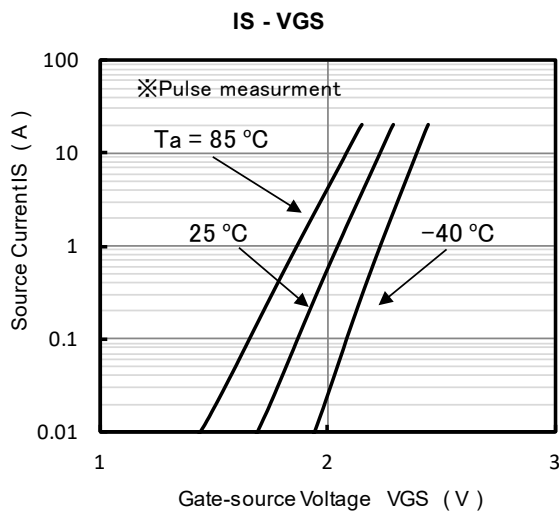
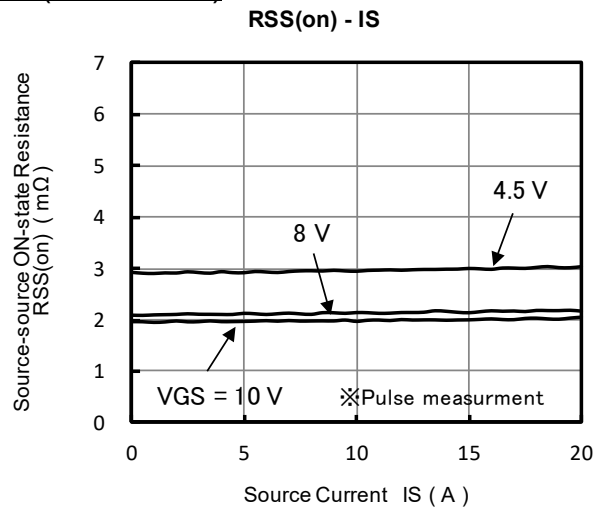
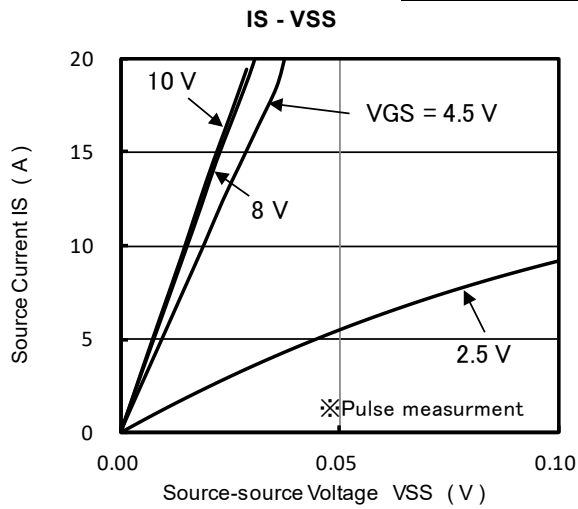
*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



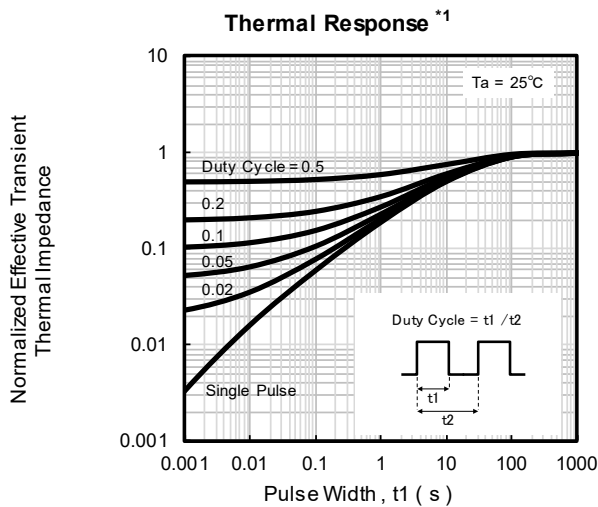
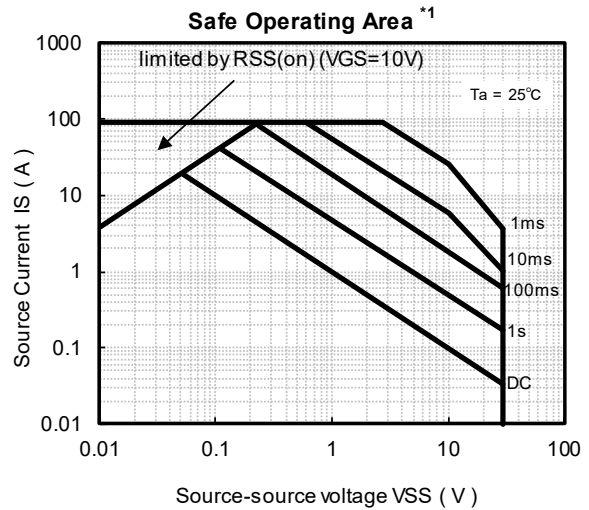
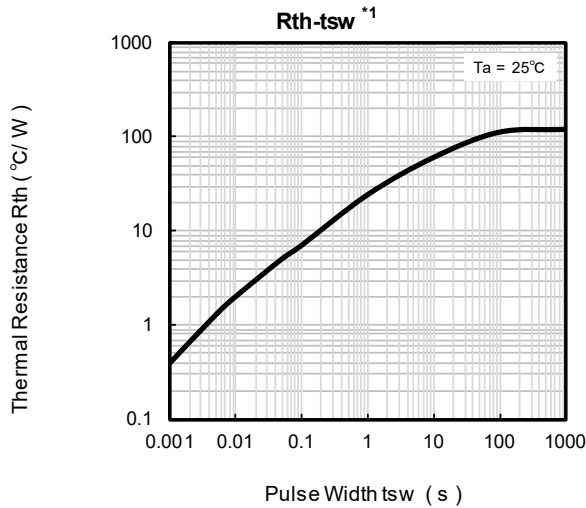
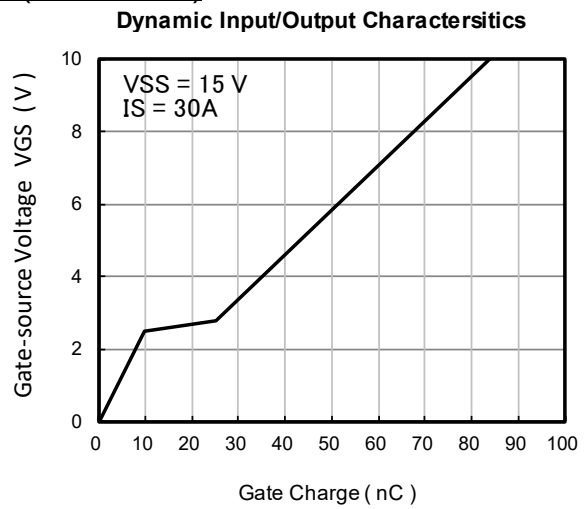
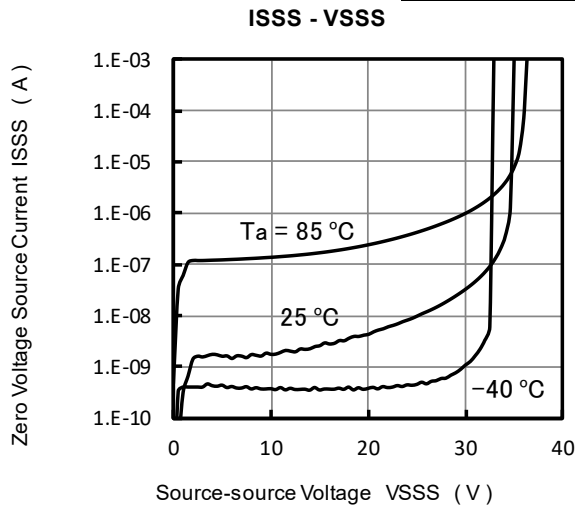
8. TECHNICAL DATA (Reference)

Technical Data (reference)



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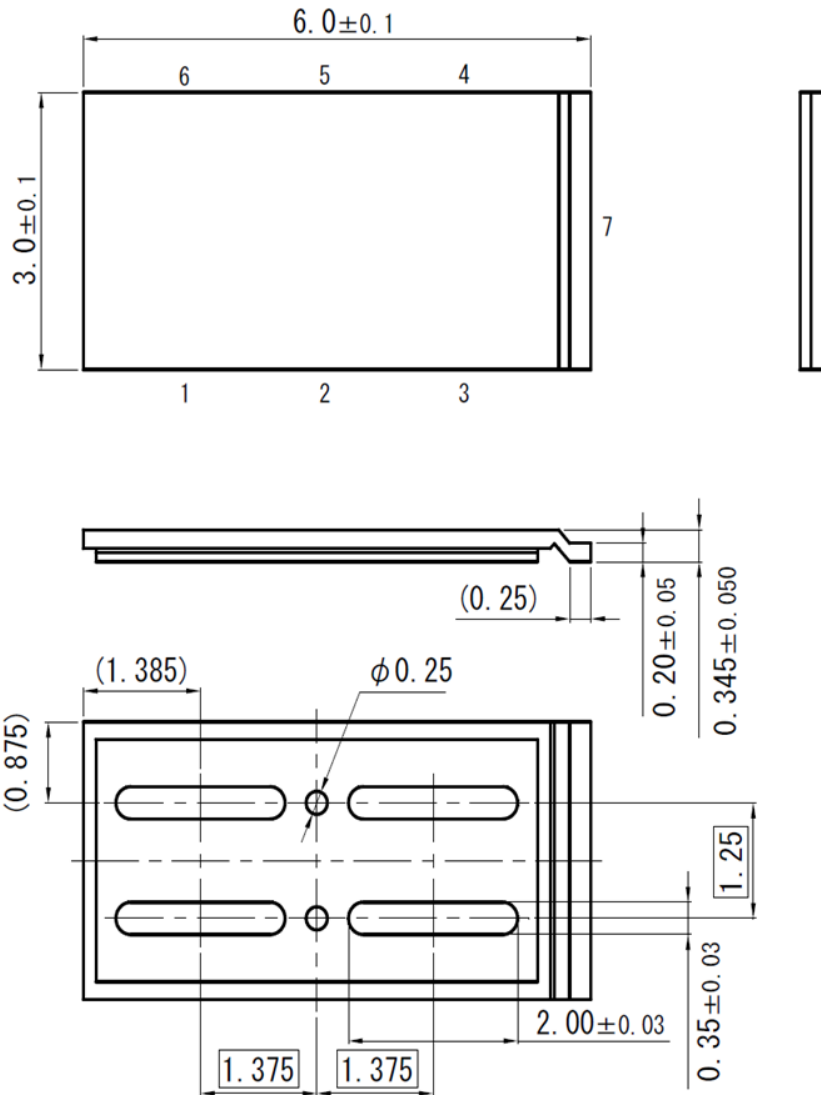


Note

^{*1} Mounted on FR4 board (25.4mm x 25.4mm x t1.0mm) using the minimum recommended pad size (36 μm Copper).

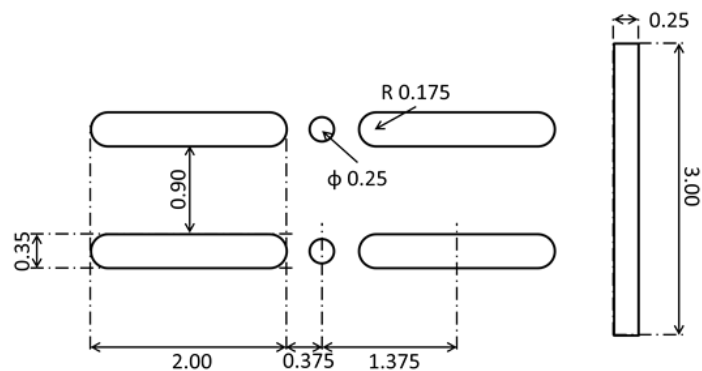
9. OUTLINE

Unit: mm



10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.3.8	1.00	1. Initially issued.
2021.08.31	1.01	1. Changed document name from Product Standards to Datasheet. 2. Added important notice in Land Pattern. 3. Added special attention and precautions notes.

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