Gate resistor installed
Dual N-channel MOSFET

KFC4B22070L
Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
For lithium-ion secondary battery protection circuits

2. FEATURES

- Low source-source ON Resistance: RSS (on) typ. = 17.5 mΩ (VGS = 4.5 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1)

3. MARKING SYMBOL: 14

4. PACKAGING

Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

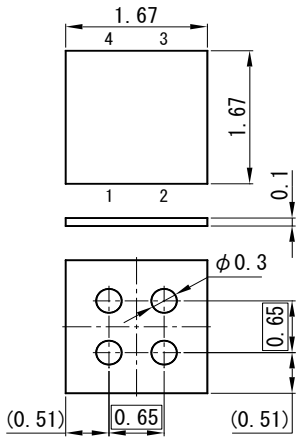
Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	24	V
Gate-source Voltage		VGS	±12	V
Source Current	DC	IS *1	6	A
	Pulsed	ISp *2	60	
Total Power Dissipation	DC	PD *1	1.5	W
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth *1	83	°C / W

Note *1 Mounted on Ceramic substrate (70 mm x 70 mm x t1.0 mm).
*2 t = 10 μs, Duty Cycle ≤ 1 %

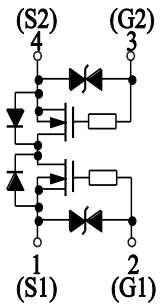
Unit: mm



1. Source (FET1) 3. Gate (FET2)
2. Gate (FET1) 4. Source (FET2)

Package	MLGA004-W-1717-RA
JEITA	—
Code	—

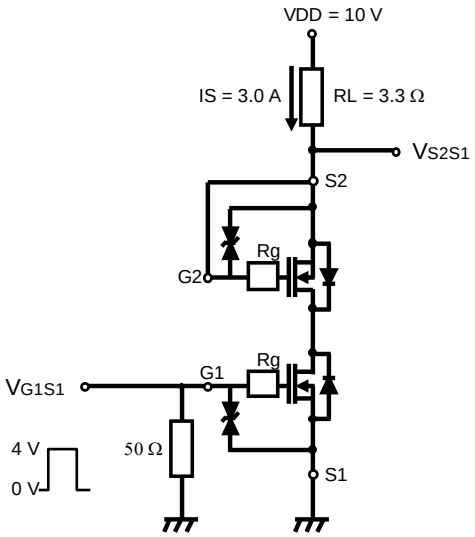
Equivalent circuit

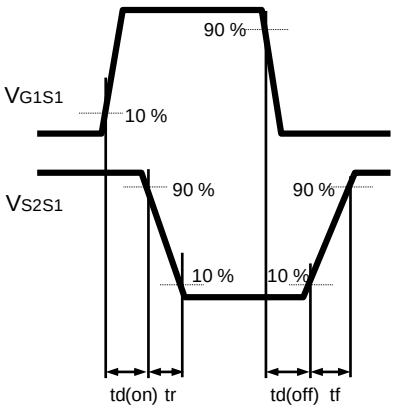


7. ELECTRLCAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	24			V
Zero Gate Voltage Source Current	ISSS	VSS = 24 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	IS = 1.0 mA, VSS = 10 V	0.4	0.9	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 3.0 A, VGS = 4.5 V	12.0	17.5	22.0	mΩ
	RSS(on)2	IS = 3.0 A, VGS = 3.1 V	13.0	20.0	28.0	
	RSS(on)3	IS = 3.0 A, VGS = 2.5 V	15.0	23.0	37.0	
Body Diode Forward Voltage	VF(s-s)	IF = 6.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		1780		pF
Output Capacitance *1	Coss			410		
Reverse Transfer Capacitance *1	Crss			407		
Turn-on Delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4 V		0.8		μs
Rise Time *1,*2	tr	IS = 3.0 A		1.5		
Turn-off Delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4 to 0 V		6.0		μs
Fall Time *1,*2	tf	IS = 3.0 A		3.0		
Total Gate Charge *1	Qg	VDD = 10 V		15.0		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		4.1		
Gate-drain Charge *1	Qgd	IS = 6.0 A		3.8		

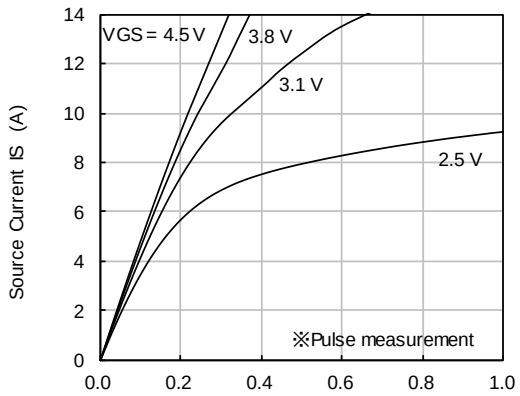
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Guaranteed by design, not subject to production testing
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



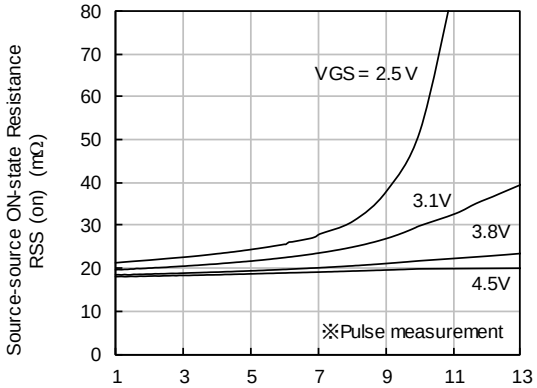


8. TECHNICAL DATA (Reference)

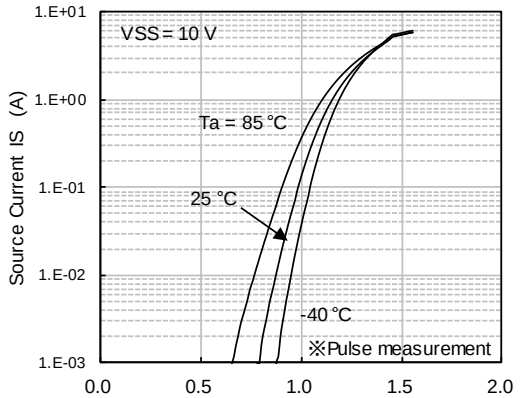
IS - VSS



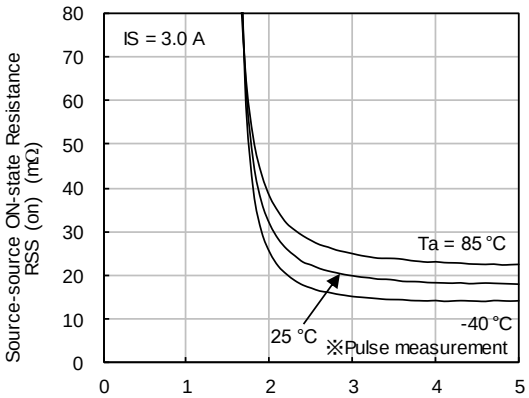
RSS(on) - IS



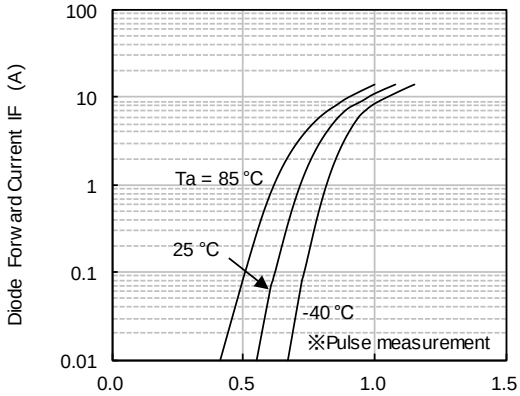
IS - VGS



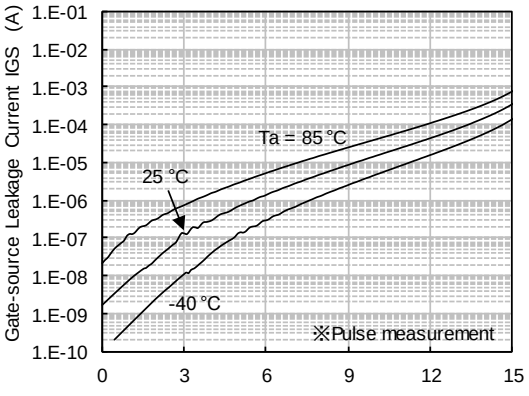
RSS(on) - VGS



IF - VF

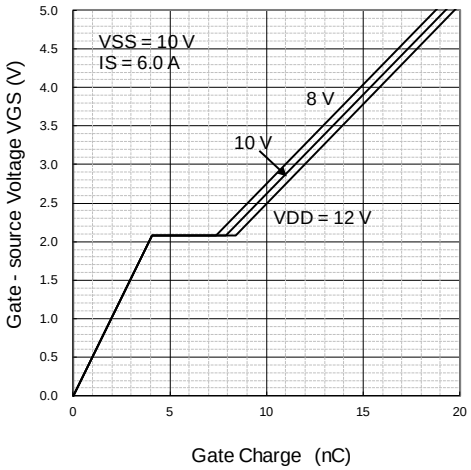


IGS - VGS

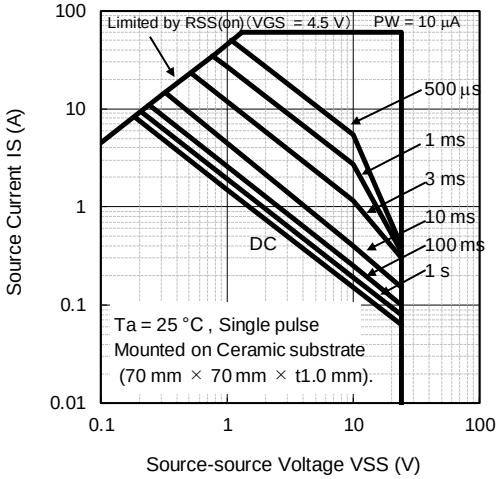


TECHNICAL DATA (Reference)

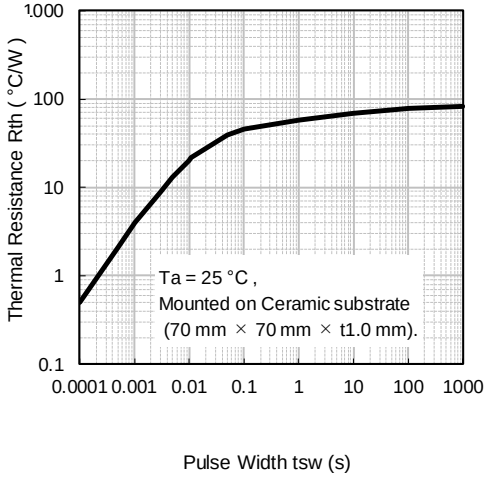
Dynamic Input/Output Characteristics



Safe Operating Area

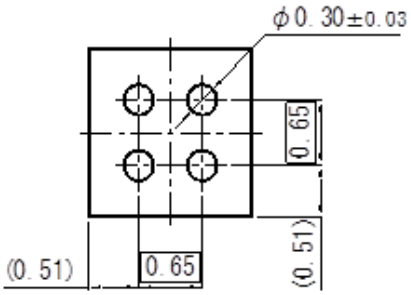


Rth - tsw



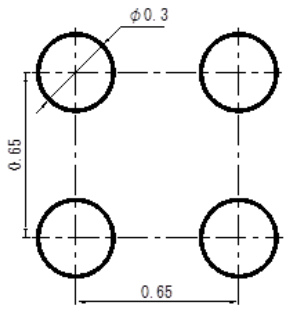
9. OUTLINE

Unit: mm



10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.2.3	1.00	1. Initially issued.
2021.08.31	1.01	1. Changed document name from Product Standards to Datasheet. 2. Added important notice in Land Pattern. 3. Added special attention and precautions notes.

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