

Dual N-channel MOSFET

KFCAB22900L Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: $R_{SS(on)}$ typ = 1.4 m Ω (V_{GS} = 10 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: R4

4. PACKAGING

Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

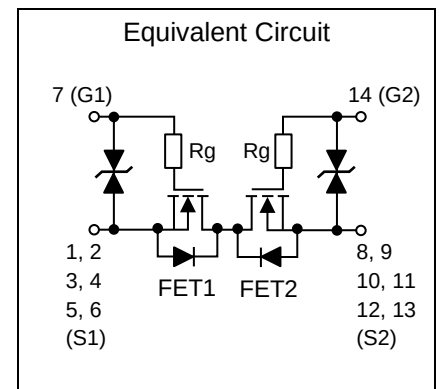
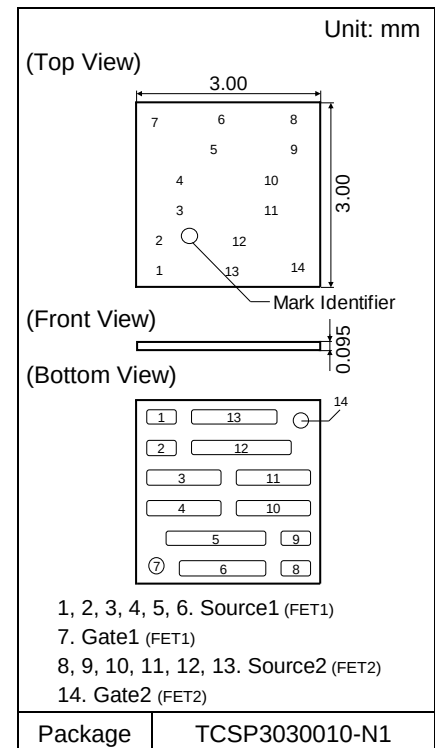
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	24	V
Gate-source Voltage	VGS	+ 16 / - 14	V
Source Current	DC *1	IS1	A
	DC *2	IS2	
	DC *3	IS3	
	Pulsed *4	ISp	
Total Power Dissipation	DC *1	PD1	W
	DC *2	PD2	
	DC *3	PD3	
Operating Junction and Storage Temperature Range	Tj, Tstg	- 55 to + 150	$^\circ\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	216	$^\circ\text{C} / \text{W}$
	Rth2 *2	73	
	Rth3 *3	38	

- Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (34 mm² area, 36 μm thickness).
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (611 mm² area, 36 μm thickness).
- *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
- *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$.



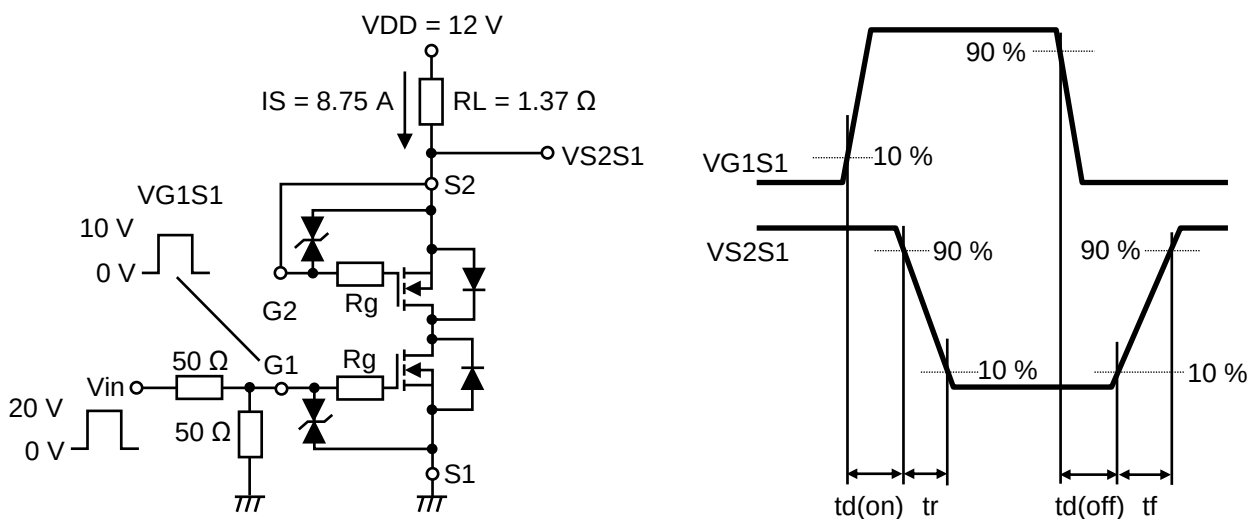
7. ELECTRICAL CHARACTERISTICS $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	24			V
Zero Gate Voltage Source Current	ISSS	VSS = 24 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS1	VGS = + 16 V, VSS = 0 V			10	μA
		VGS = - 14 V, VSS = 0 V			- 10	
	IGSS2	VGS = ± 8 V, VSS = 0 V			± 1	
Gate-source Threshold Voltage	Vth	IS = 1.34 mA, VSS = 10 V	1	2	3	V
Source-source On-state Resistance	RSS(on)1	IS = 8.75 A, VGS = 10 V	0.80	1.40	1.85	m Ω
	RSS(on)2	IS = 8.75 A, VGS = 8.0 V	0.90	1.55	2.35	
	RSS(on)3	IS = 8.75 A, VGS = 4.5 V	1.30	2.30	5.10	
Body Diode Forward Voltage	VF(s-s)	IF = 8.75 A, VGS = 0 V		0.74	1.00	V
Input Capacitance ^{*1}	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		5780		pF
Output Capacitance ^{*1}	Coss			710		
Reverse Transfer Capacitance ^{*1}	Crss			610		
Turn-on Delay Time ^{*1, *2}	td(on)	VDD = 12 V, VGS = 0 to 10 V		1.0		μs
Rise Time ^{*1, *2}	tr	IS = 8.75 A		1.5		
Turn-off Delay Time ^{*1, *2}	td(off)	VDD = 12 V, VGS = 10 to 0 V		9.0		μs
Fall Time ^{*1, *2}	tf	IS = 8.75 A		3.7		
Total Gate Charge ^{*1}	Qg	VDD = 12 V		110		nC
Gate-source Charge ^{*1}	Qgs	VGS = 0 to 10 V		15		
Gate-drain Charge ^{*1}	Qgd	IS = 17.5 A		27		
Gate Resistance ^{*1}	Rg	f = 1 MHz	400	700	1000	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

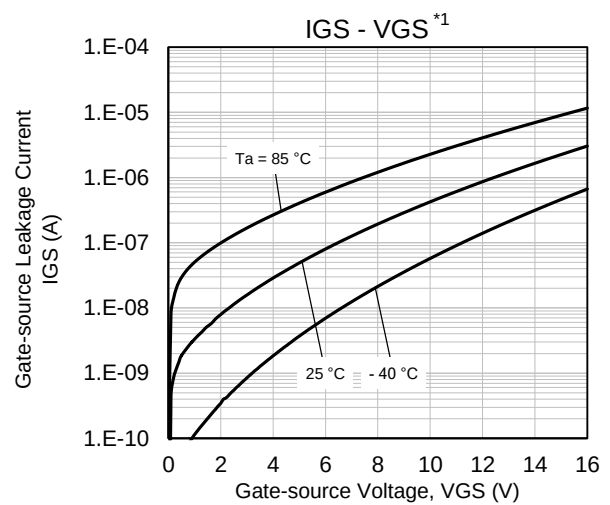
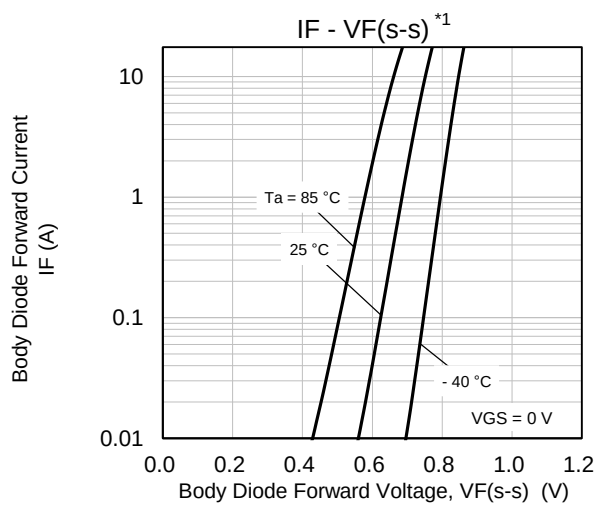
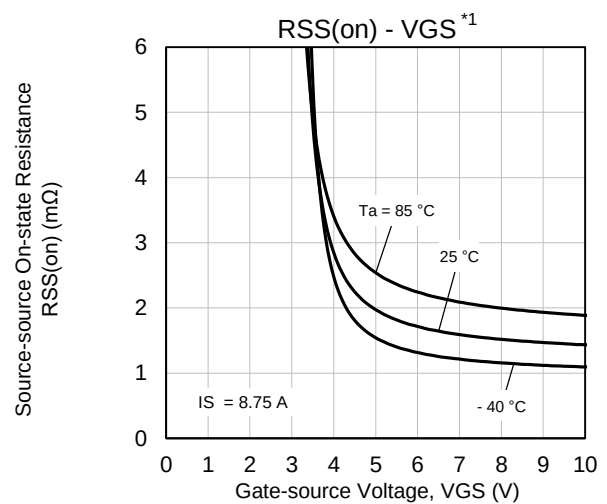
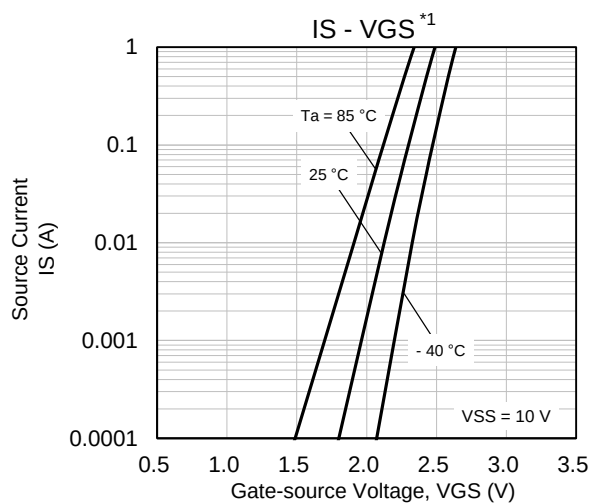
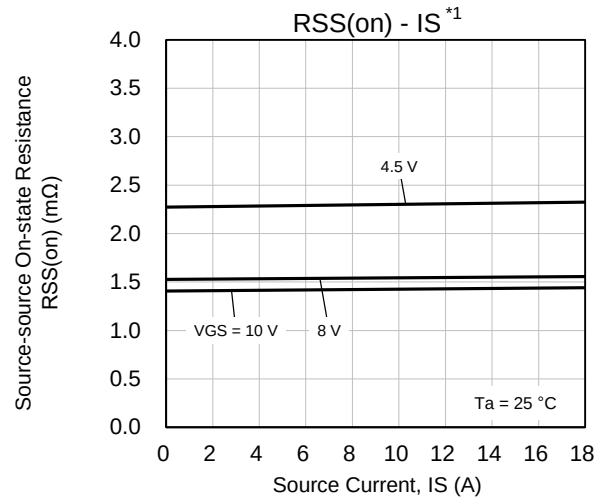
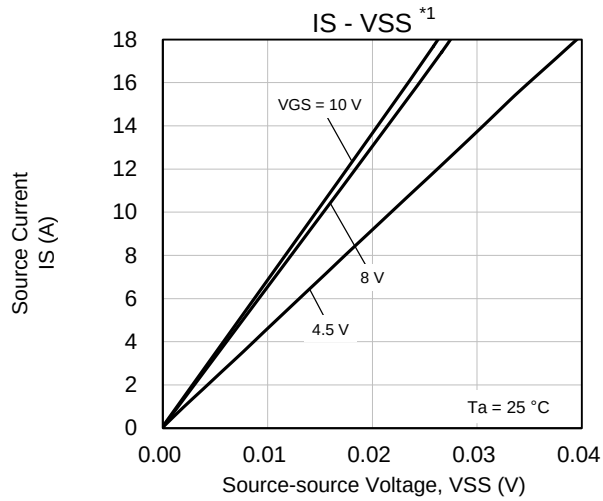
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



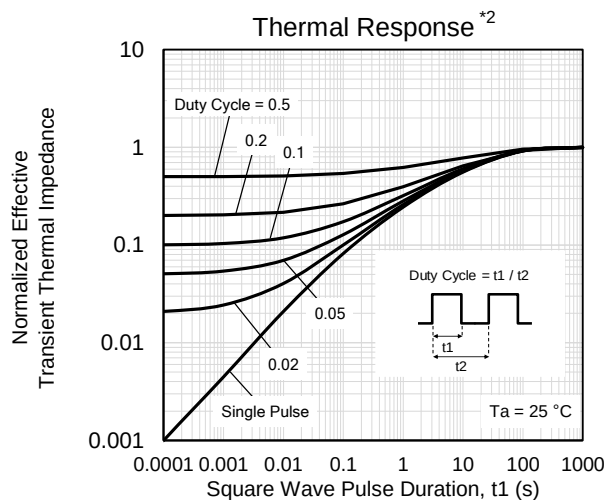
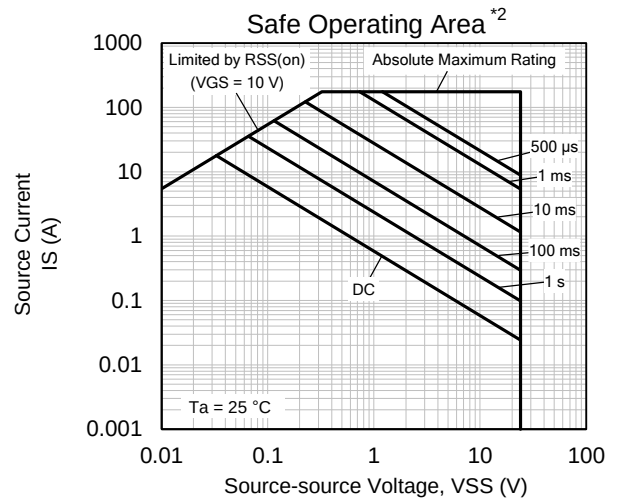
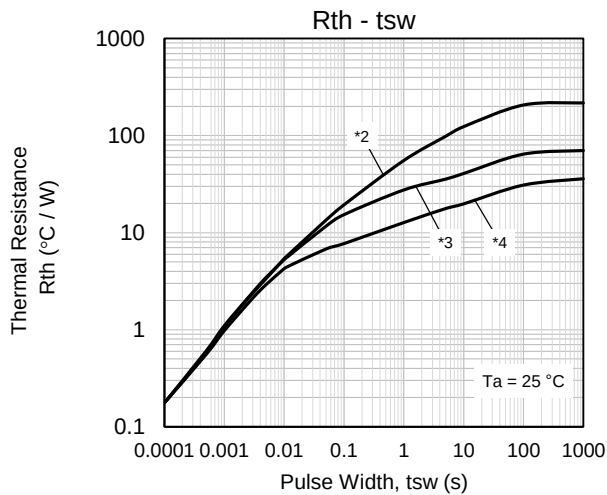
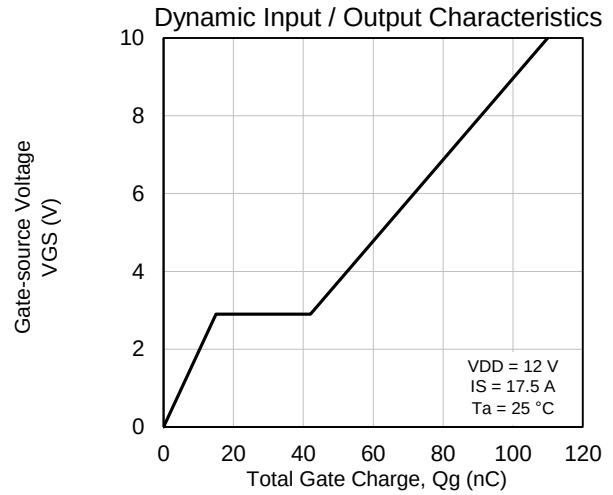
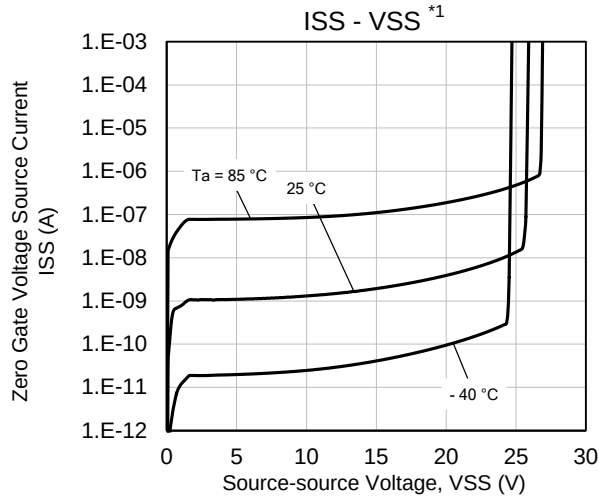
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 k Ω	H2	> 2 to ≤ 4	kV

9. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



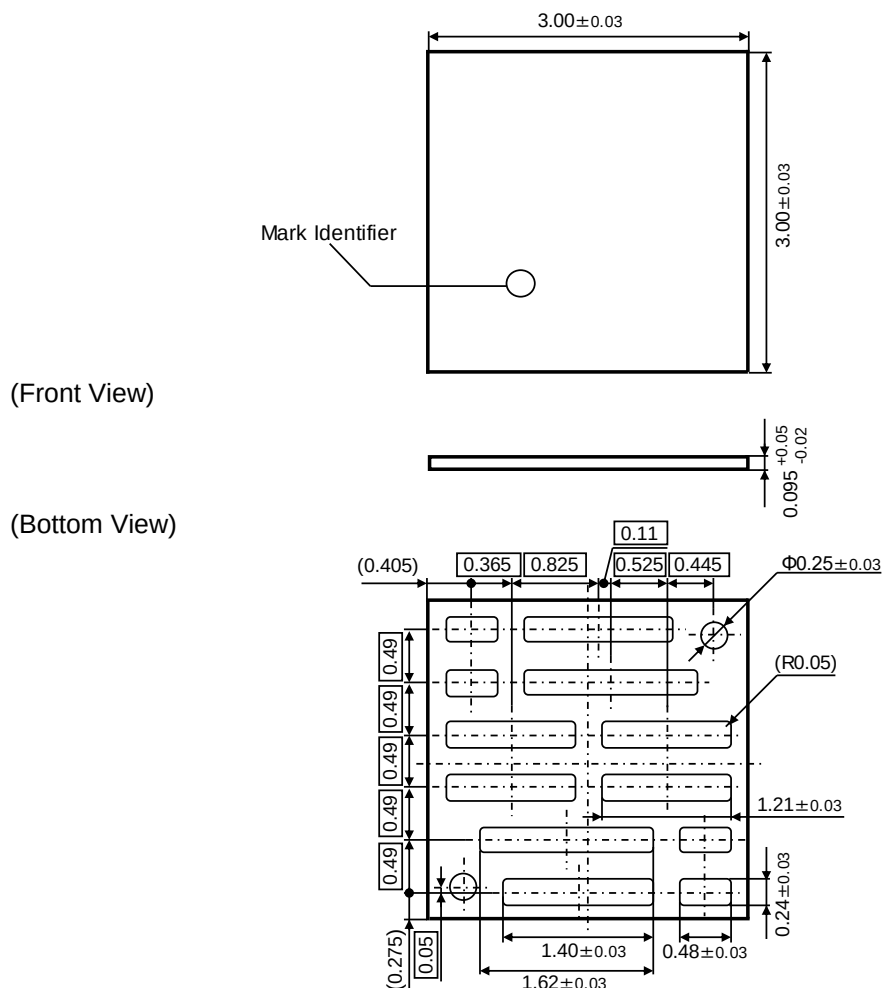
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (34 mm² area, 36 μm thickness).
- *3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (611 mm² area, 36 μm thickness).
- *4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

10. OUTLINE

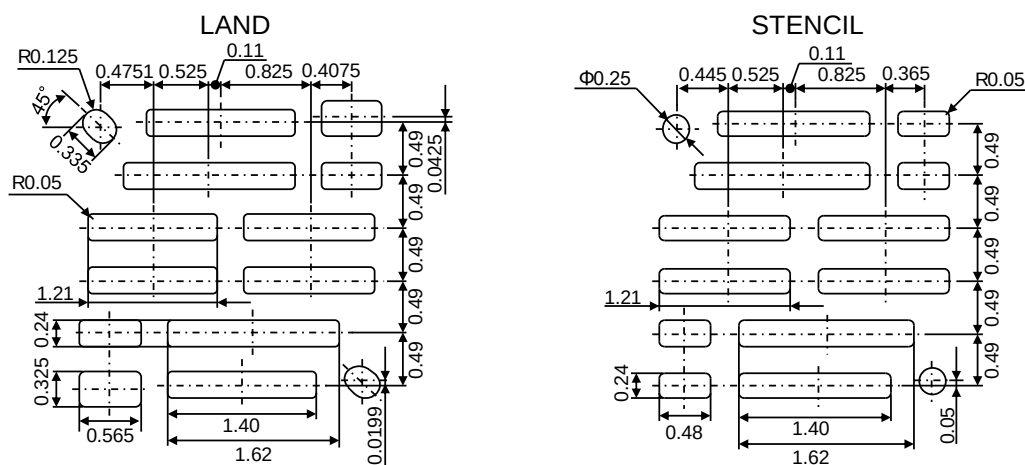
(Top View)

Unit: mm



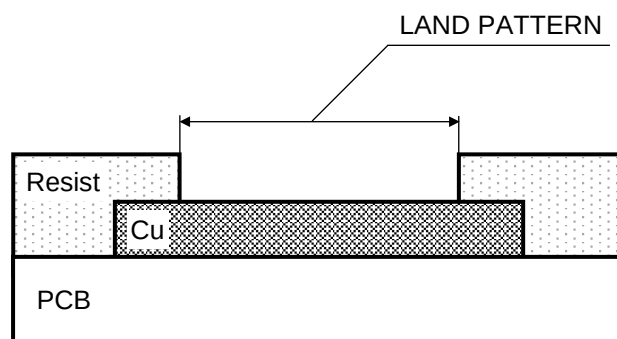
11. LAND ^{*1} & STENCIL PATTERN (Reference)

Unit: mm



Note *1 The definition of land pattern is referred to next page.

DEFINITION OF LAND PATTERN



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.11.9	1.00	1. Initially issued.
2022.2.16	1.01	1. Added definition of Land Pattern.

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