Gate resistor installed
Dual N-channel MOSFET

KFC4B22180L
Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
For lithium-ion secondary battery protection circuits

2. FEATURES

- Low source-source ON Resistance: RSS (on) typ. = 9.4 mΩ (VGS = 4.5 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1)

3. MARKING SYMBOL: 17

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

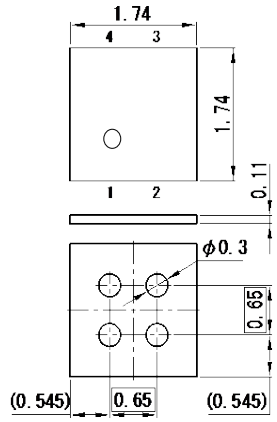
Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	20	V
Gate-source Voltage		VGS	±8	V
Source Current	DC	IS1 *1	5	A
		IS2 *2	10	
	Pulsed	ISp *3	50	
Total Power Dissipation	DC	PD1 *1	0.4	W
		PD2 *2	1.5	
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	312	°C / W
	Rth2 *2	83	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm) using the minimum recommended pad size (36μm Copper).
*2 Mounted on ceramic substrate (70 mm x 70 mm x t1.0 mm).
*3 t = 10 μs, Duty Cycle ≤ 1 %

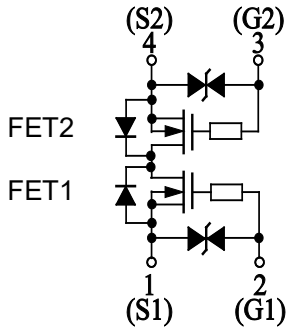
Unit: mm



1. Source (FET1) 3. Gate (FET2)
2. Gate (FET1) 4. Source (FET2)

Package	MLGA004-W-1717-RB
JEITA	—
Code	—

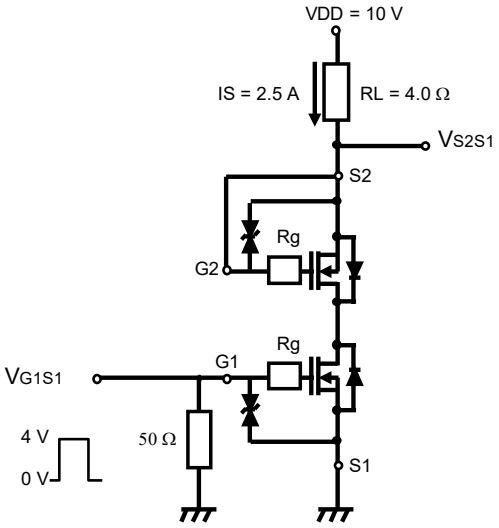
Equivalent circuit

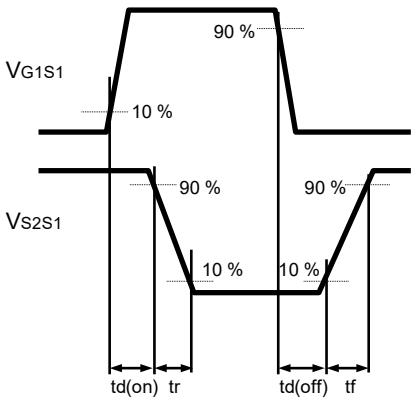


7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	20			V
Zero Gate Voltage Source Current	ISSS	VSS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS1	VGS = ±8 V, VSS = 0 V			±10.0	μA
	IGSS2	VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.64 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 2.5 A, VGS = 4.5 V	7.0	9.4	11.9	mΩ
	RSS(on)2	IS = 2.5 A, VGS = 3.8 V	7.3	10.0	12.9	
	RSS(on)3	IS = 2.5 A, VGS = 3.1 V	8.1	11.1	15.8	
	RSS(on)4	IS = 2.5 A, VGS = 2.5 V	8.6	13.4	22.6	
Body Diode Forward Voltage	VF(s-s)	IF = 2.5 A, VGS = 0 V		0.8	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		2440		pF
Output Capacitance *1	Coss			200		
Reverse Transfer Capacitance *1	Crss			160		
Turn-on Delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4 V		0.9		μs
Rise Time *1,*2	tr	IS = 2.5 A		1.6		
Turn-off Delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4 to 0 V		5.0		μs
Fall Time *1,*2	tf	IS = 2.5 A		2.4		
Total Gate Charge *1	Qg	VDD = 10 V		23		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		6		
Gate-drain Charge *1	Qgd	IS = 2.5 A		5		

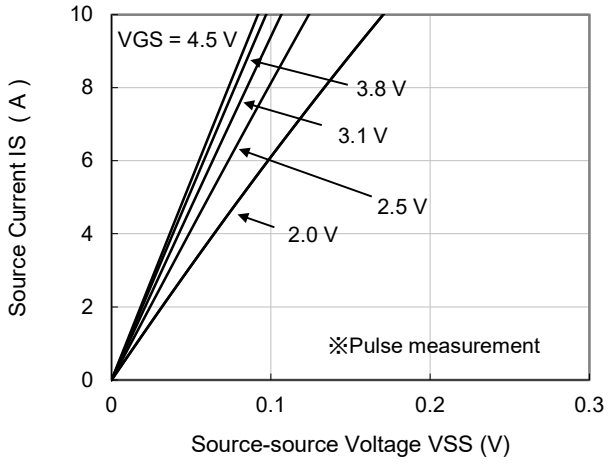
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Guaranteed by design, not subject to production testing
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



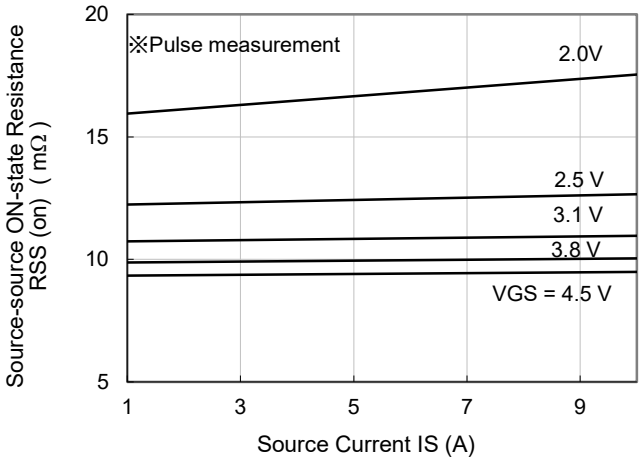


8. TECHNICAL DATA (Reference)

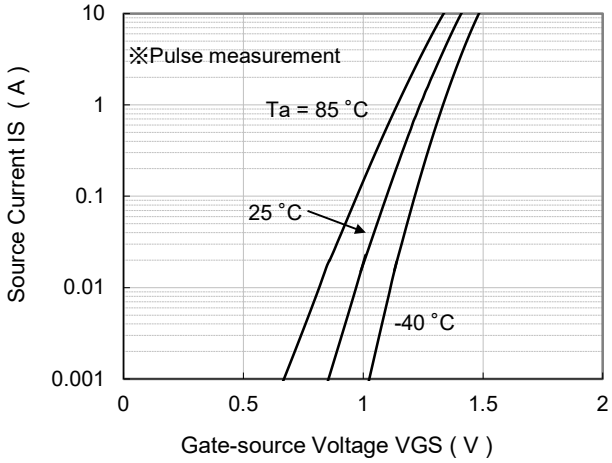
IS - VSS



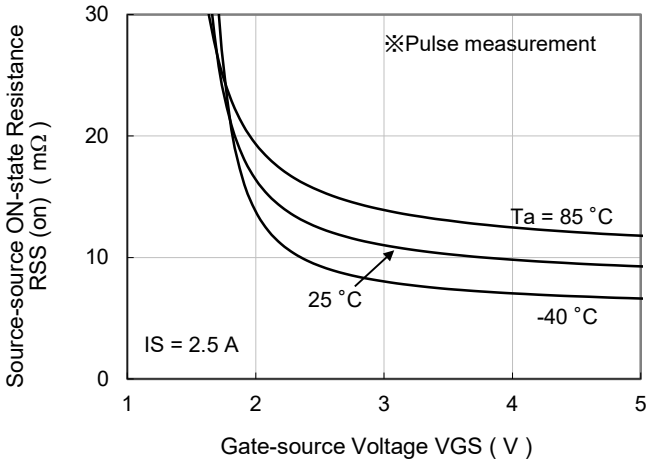
RSS(on) - IS



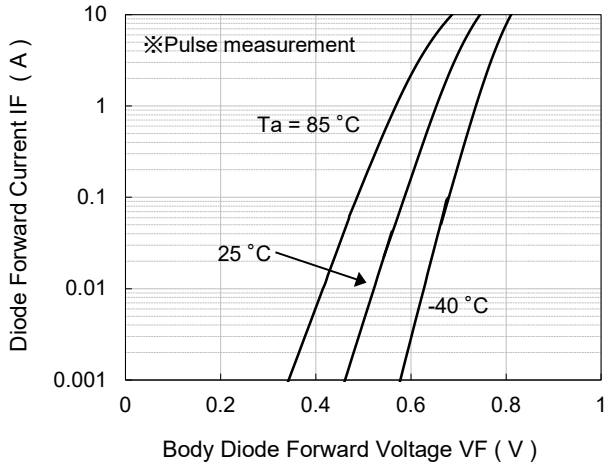
IS - VGS



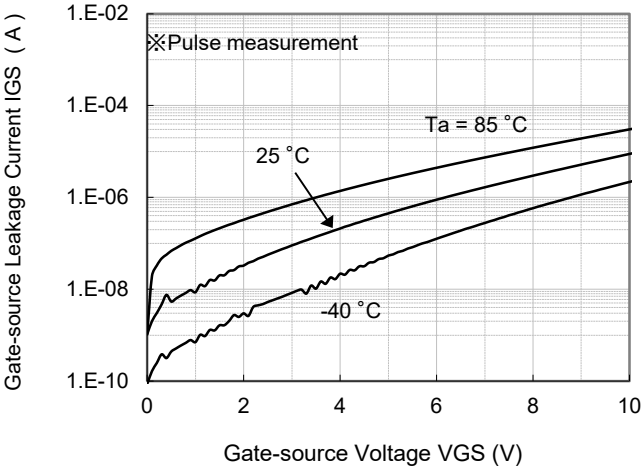
RSS(on) - VGS



IF - VF

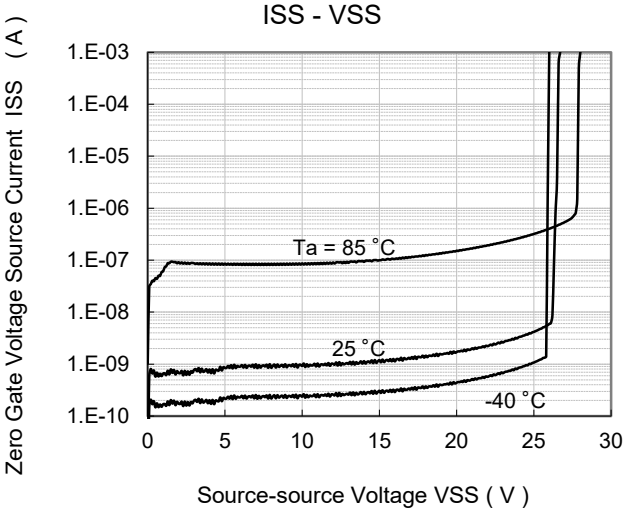


IGS - VGS

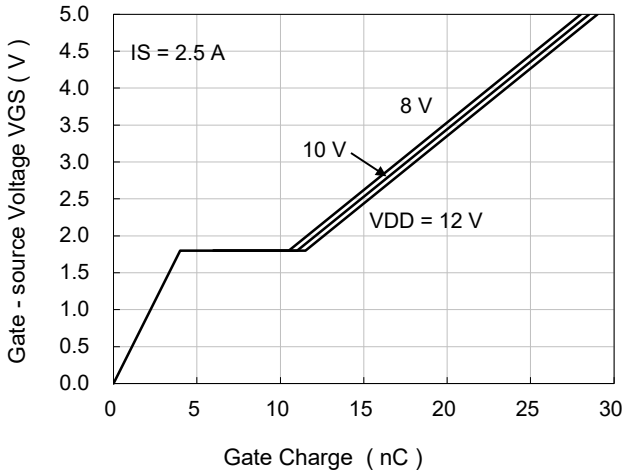


TECHNICAL DATA (Reference)

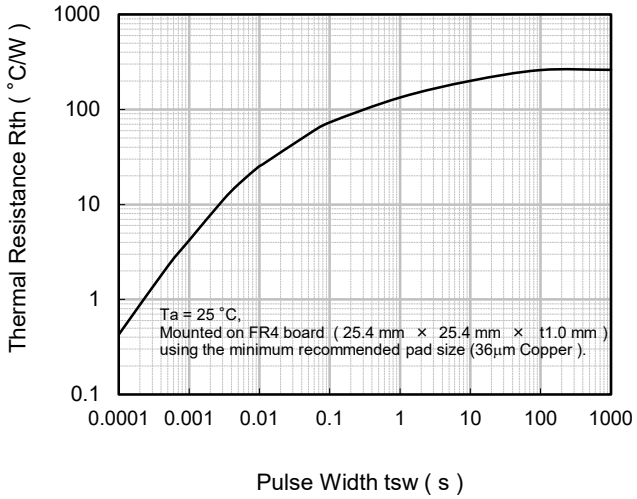
ISS - VSS



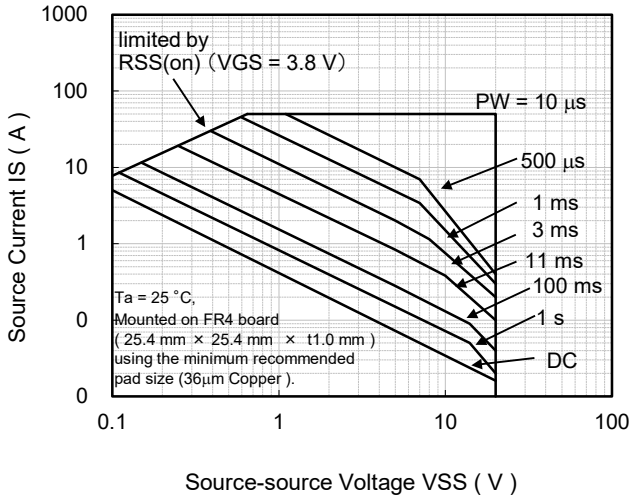
Dynamic Input/Output Characteristics



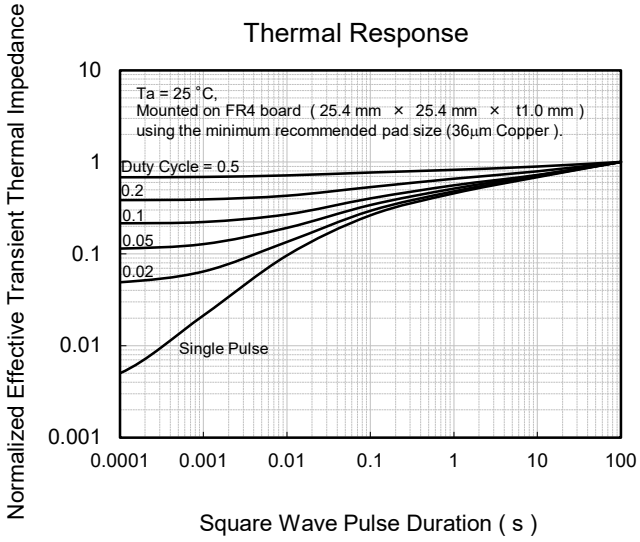
Rth - tsw



Safe Operating Area

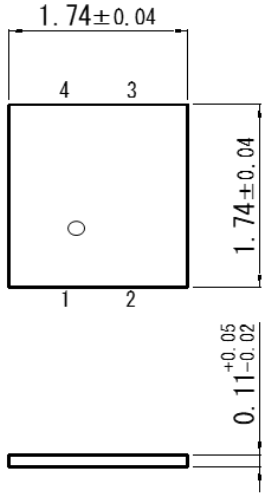


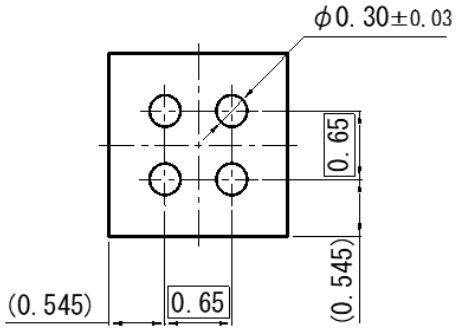
Thermal Response



9. OUTLINE

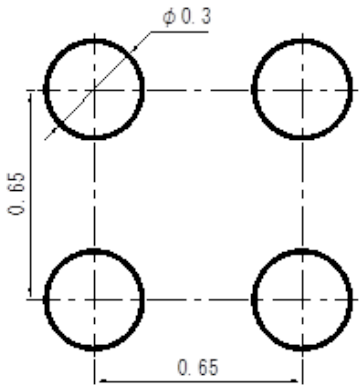
Unit: mm





10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.2.3	1.00	1. Initially issued.
2021.7.26	1.01	1. Revised Safe Operating Area in page 5.
2021.08.31	1.02	1. Changed document name from Product Standards to Datasheet. 2. Added important notice in Land Pattern. 3. Added special attention and precautions notes.

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