

Gate resistor installed Dual N-channel MOSFET

KFC4B21300L Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET For lithium-ion secondary battery protection circuits

2. FEATURES

- Source-source ON Resistance: Rss(on) typ. = 70 m Ω (VGS = 4.5 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1)

3. MARKING SYMBOL: 29

4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

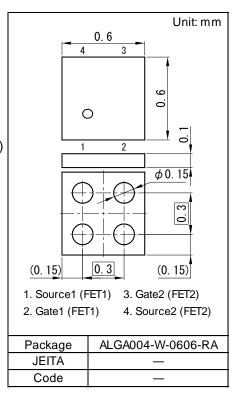
Parameter		Symbol	Rating	Unit	
Source-source Voltage		VSS	12	V	
Gate-source Voltage		VGS	±8	V	
Source Current (DC)		IS1 *1	1.5	Α	
		IS2*2	2	Α	
Source Current (Pulsed)		ISp *3	15	Α	
Total Power Dissipation	DC	PD1 *1	0.32	W	
		PD2*2	0.6	W	
Channel Temperature		Tch	150	°C	
Storage Temperature Range		Tstg	-55 to +150	°C	

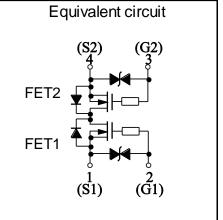
6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit	
Thermal Decistores (sh. s)	Rth1 *1	390	°C/W	
Thermal Resistance (ch-a)	Rth2 *2	208	°C/W	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm), using the minimum recommended pad size (36μm Copper).

- *2 Mounted on Ceramic substrate (70 mm x 70 mm x t1.0 mm).
- *3 $t = 10 \mu s$, Duty Cycle $\leq 1 \%$







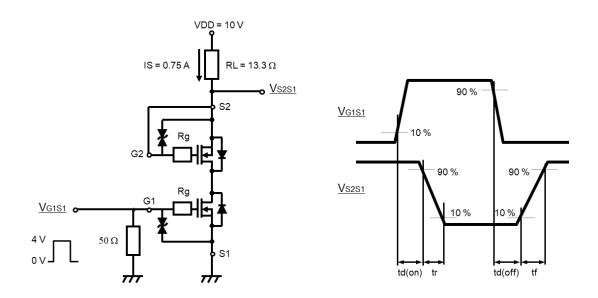
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit	
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V	
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μА	
Gate-Source Leakage Current	IGSS	$VGS = \pm 8 \text{ V}, VSS = 0 \text{ V}$			±10		
		$VGS = \pm 5 V$, $VSS = 0 V$			±1.0	μА	
Gate-source Threshold Voltage	Vth	IS = 0.03 mA, VSS = 10 V	0.35	0.90	1.40	V	
Source-source On-state Resistance	RSS(on)1	IS = 0.75 A, VGS = 4.5 V	55	70	95		
	RSS(on)2	IS = 0.75 A, VGS = 3.8 V	60	80	110	mΩ	
	RSS(on)3	IS = 0.75 A, VGS = 3.1 V	65	90	150		
	RSS(on)4	IS = 0.75 A, VGS = 2.5 V	70	115	225	1	
Body Diode Forward Voltage	VF(s-s)	IF = 0.75 A, VGS = 0 V		0.6	1.2	V	
Input Capacitance *1	Ciss			115			
Output Capacitance *1	Coss	VSS = 10 V, VGS = 0 V, f = 1 kHz		25		pF	
Reverse Transfer Capacitance *1	Crss			18			
Turn-on Delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4 V		0.10		_	
Rise Time *1,*2	tr	IS = 0.75 A		0.20		μS	
Turn-off Delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4 to 0 V		0.27			
Fall Time *1,*2	tf	IS = 0.75 A		0.22		μS	
Total Gate Charge *1	Qg	VDD = 10 V		1.7			
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		0.5		nC	
Gate-drain Charge *1	Qgd	IS = 0.75 A		0.45			

Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

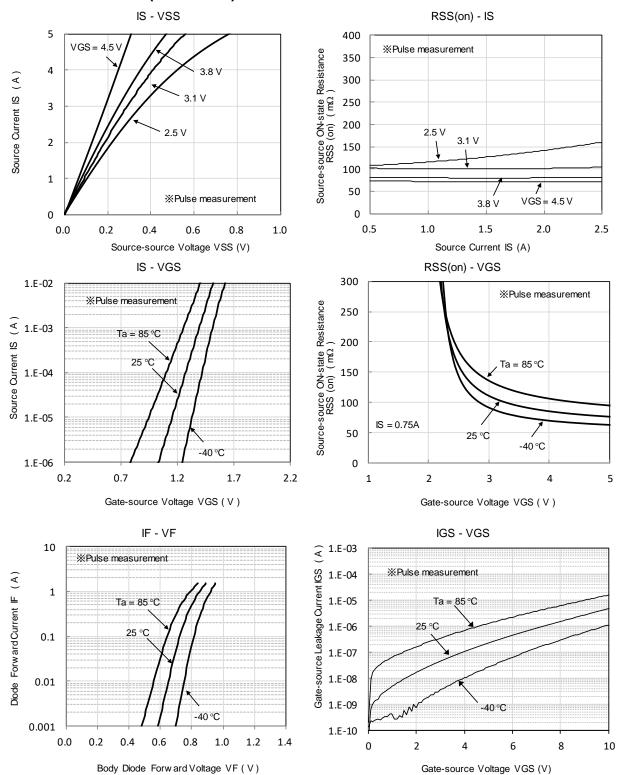
*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time Note



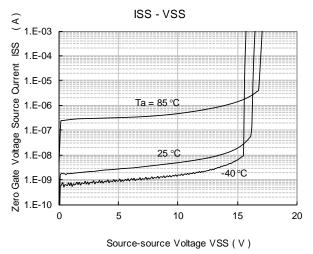


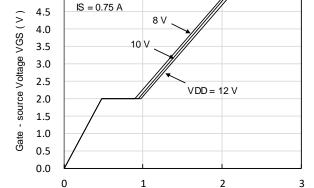
8. TECHNICAL DATA (Reference)





TECHNICAL DATA (Reference)

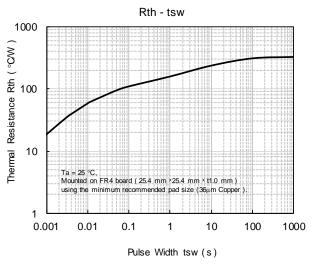


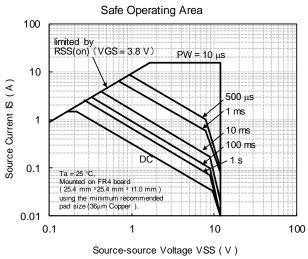


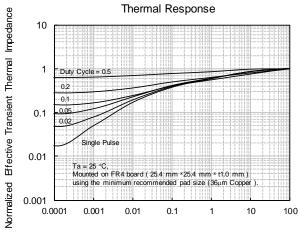
Gate Charge (nC)

Dynamic Input/Output Characteristics

5.0







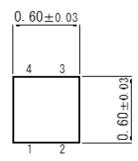
Square Wave Pulse Duration (s)

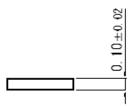


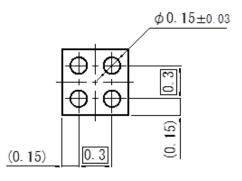


9. OUTLINE

Unit: mm

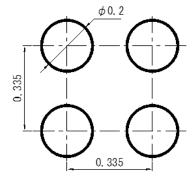






10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design. Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.



11. REVISION HISTORY

Date	Revision	Description	
2021.02.05	1.00	1. Initially issued.	
2021.08.31 1.01		Changed document name from Product Standards to Datasheet.	
	1.01	2. Added important notice in Land Pattern.	
		3. Added special attention and precautions notes.	



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