

Gate resistor installed Dual N-channel MOSFET

KFC4B21320L Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
For lithium-ion secondary battery protection circuits

2. FEATURES

- Low source-source ON Resistance: $R_{ss(on)}$ typ. = 36 m Ω (V_{GS} = 4.5 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1)

3. MARKING SYMBOL: 2D

4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

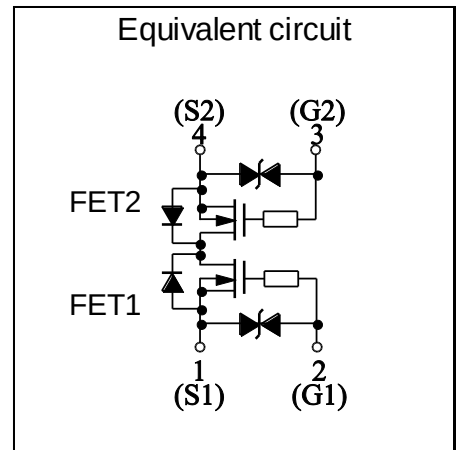
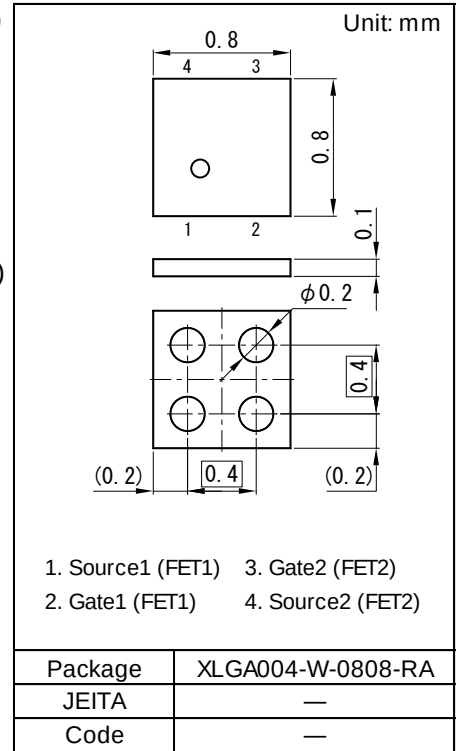
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	± 8	V
Source Current (DC)	IS1 ^{*1}	2.5	A
	IS2 ^{*2}	4	A
Source Current (Pulsed)	ISp ^{*3}	25	A
Total Power Dissipation	PD1 ^{*1}	0.34	W
	PD2 ^{*2}	0.9	W
Channel Temperature	Tch	150	$^\circ\text{C}$
Storage Temperature Range	Tstg	-55 to +150	$^\circ\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 ^{*1}	368	$^\circ\text{C} / \text{W}$
	Rth2 ^{*2}	139	$^\circ\text{C} / \text{W}$

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm), using the minimum recommended pad size (36 μm Copper).
 - *2 Mounted on Ceramic substrate (70 mm x 70 mm x t1.0 mm).
 - *3 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$



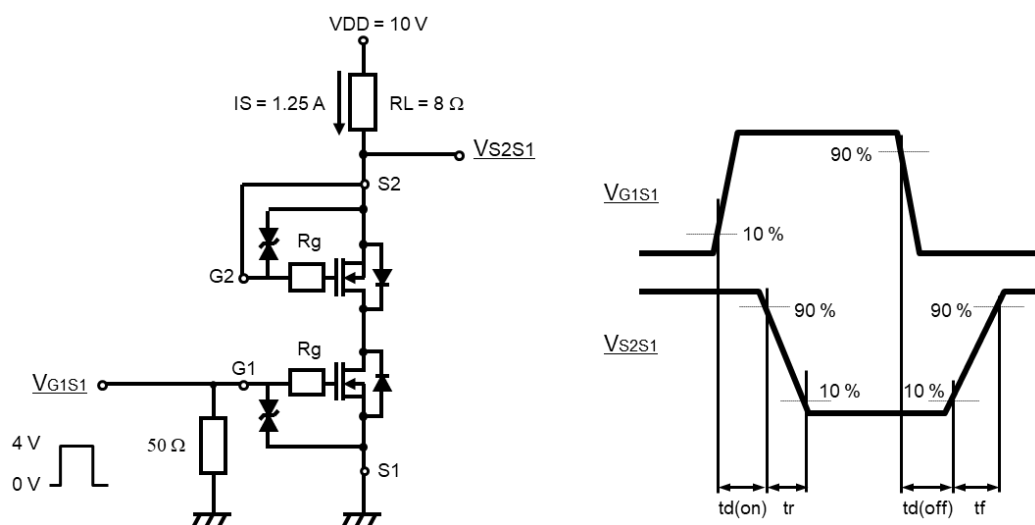
7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	$I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	12			V
Zero Gate Voltage Source Current	ISSS	$V_{SS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$			1.0	μA
Gate-Source Leakage Current	IGSS	$V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$			± 10	μA
		$V_{GS} = \pm 5\text{ V}$, $V_{SS} = 0\text{ V}$			± 1.0	
Gate-source Threshold Voltage	Vth	$I_S = 0.07\text{ mA}$, $V_{SS} = 10\text{ V}$	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	$I_S = 1.25\text{ A}$, $V_{GS} = 4.5\text{ V}$	27	36	48	m Ω
	RSS(on)2	$I_S = 1.25\text{ A}$, $V_{GS} = 3.8\text{ V}$	29	39	53	
	RSS(on)3	$I_S = 1.25\text{ A}$, $V_{GS} = 3.1\text{ V}$	32	45	75	
	RSS(on)4	$I_S = 1.25\text{ A}$, $V_{GS} = 2.5\text{ V}$	35	58	115	
Body Diode Forward Voltage	VF(s-s)	$I_F = 1.25\text{ A}$, $V_{GS} = 0\text{ V}$		0.6	1.2	V
Input Capacitance ^{*1}	Ciss	$V_{SS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ kHz}$		205		pF
Output Capacitance ^{*1}	Coss			50		
Reverse Transfer Capacitance ^{*1}	Crss			40		
Turn-on delay Time ^{*1,*2}	td(on)	$V_{DD} = 10\text{ V}$, $V_{GS} = 0\text{ to }4\text{ V}$ $I_S = 1.25\text{ A}$		0.10		μs
Rise Time ^{*1,*2}	tr			0.15		
Turn-off delay Time ^{*1,*2}	td(off)	$V_{DD} = 10\text{ V}$, $V_{GS} = 4\text{ to }0\text{ V}$ $I_S = 1.25\text{ A}$		0.50		μs
Fall Time ^{*1,*2}	tf			0.30		
Total Gate Charge ^{*1}	Qg	$V_{DD} = 10\text{ V}$		3.5		nC
Gate-source Charge ^{*1}	Qgs	$V_{GS} = 0\text{ to }4\text{ V}$		0.8		
Gate-drain Charge ^{*1}	Qgd	$I_S = 1.25\text{ A}$		1.0		

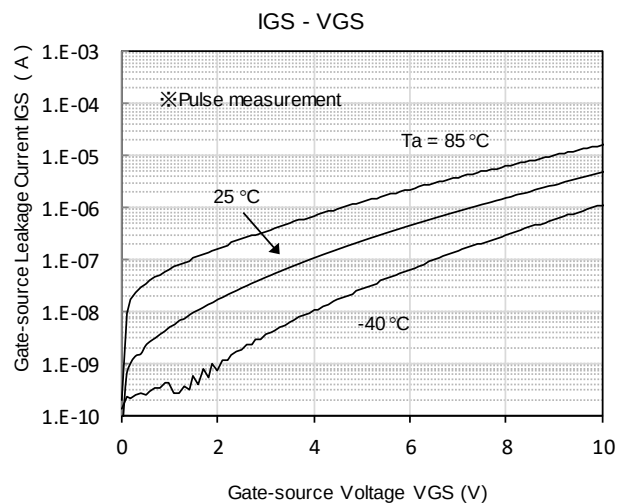
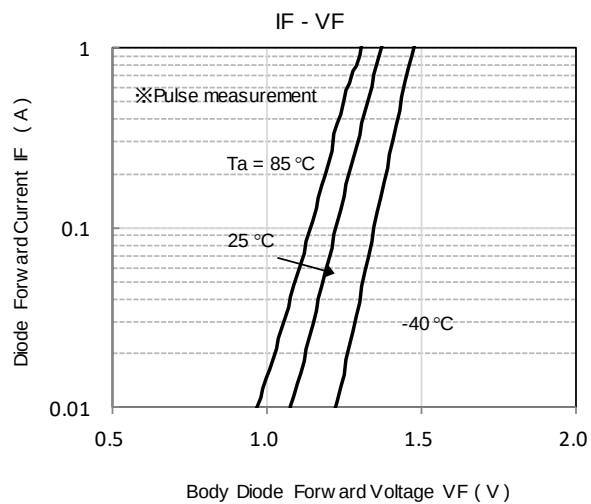
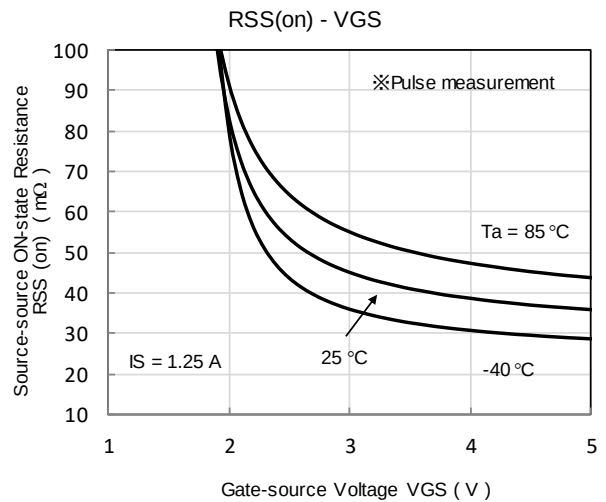
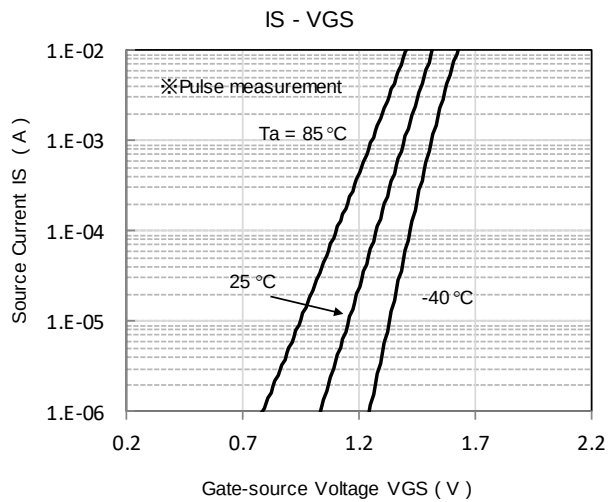
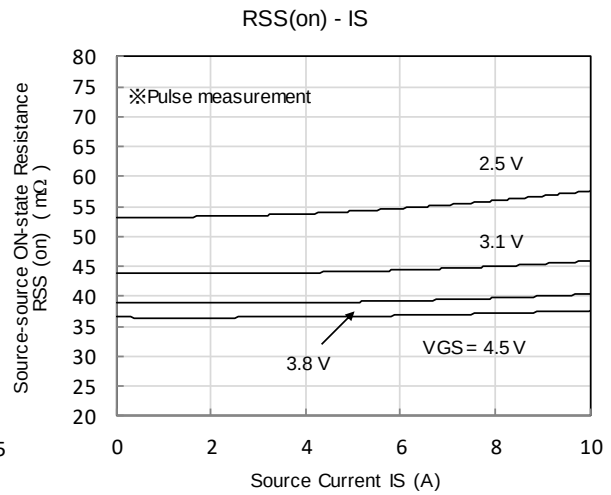
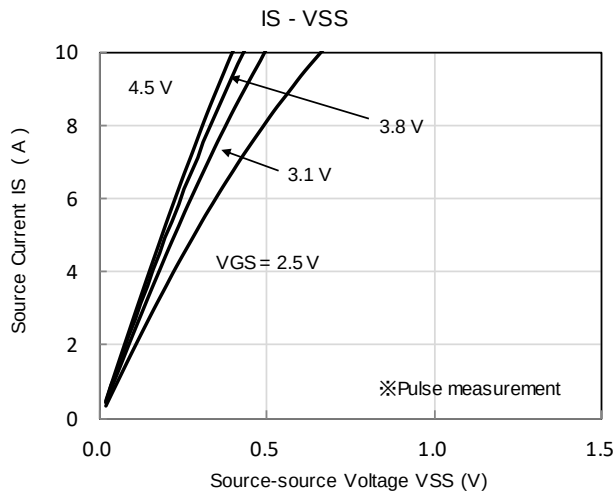
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing

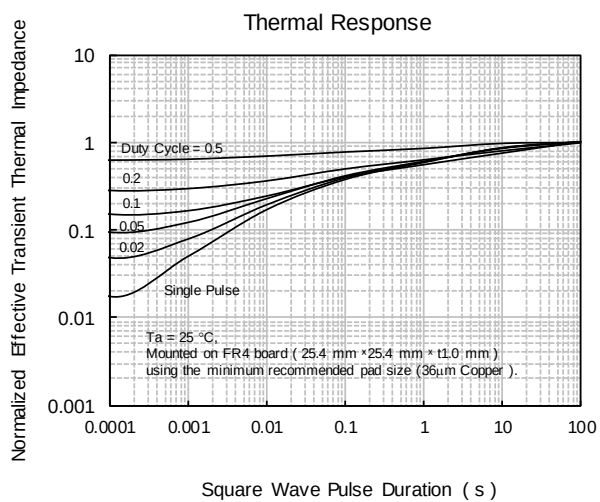
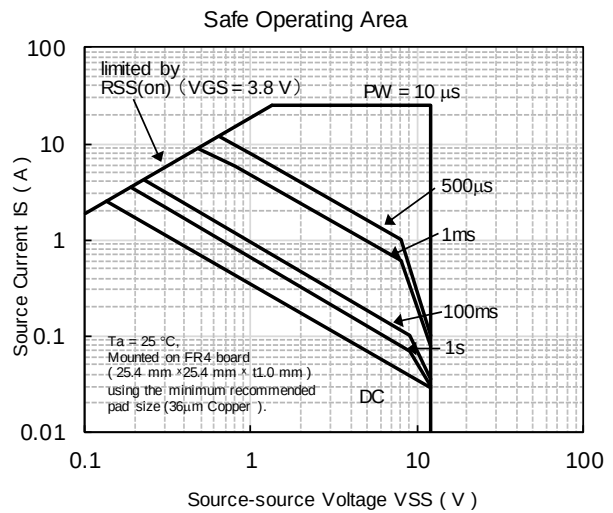
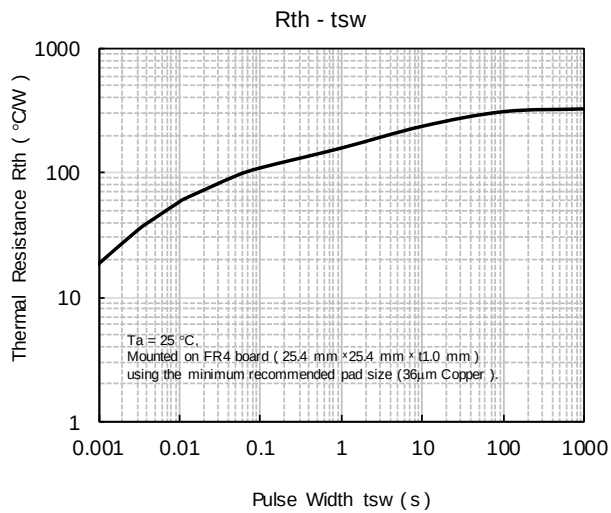
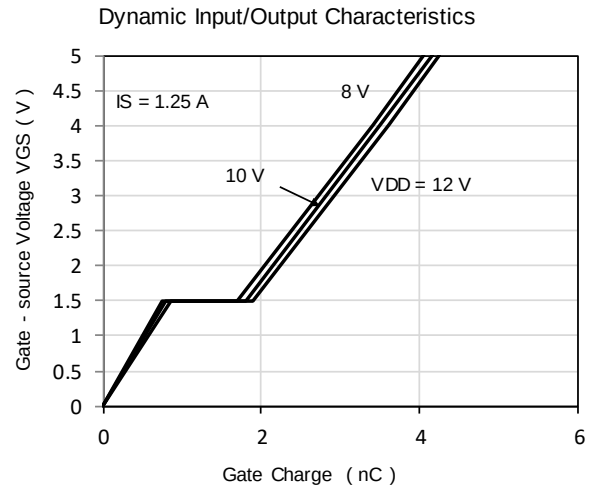
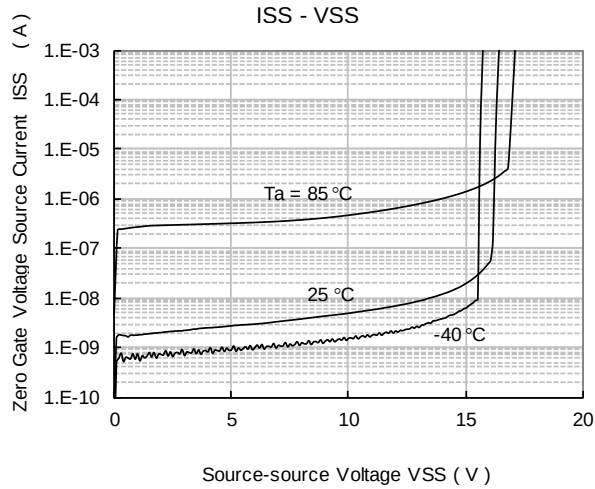
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



8. TECHNICAL DATA (Reference)

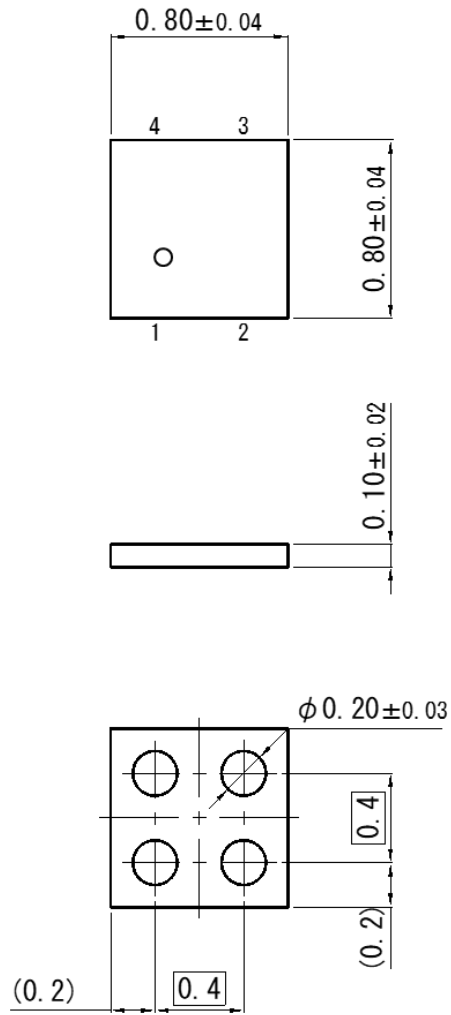


TECHNICAL DATA (Reference)



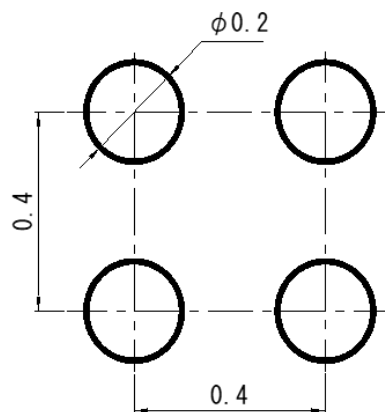
9. OUTLINE

Unit: mm



10. LAND PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.02.05	1.00	1. Initially issued.
2021.08.31	1.01	1. Changed document name from Product Standards to Datasheet. 2. Added important notice in Land Pattern. 3. Added special attention and precautions notes.

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