Gate resistor installed
Dual N-channel MOSFET

KFCAB21A50L
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET

For lithium-ion secondary battery protection circuits

2. FEATURES

- Source-source On-state Resistance: RSS(on) typ. = 2.2 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: UA

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	12	V
Gate-source Voltage		VGS	±8	V
Source Current	DC *1	IS1	13.5	A
	DC *2	IS2	25	
	DC *3	IS3	29	
	Pulsed *4	ISp	135	
Total Power Dissipation	DC *1	PD1	0.54	W
	DC *2	PD2	1.8	
	DC *3	PD3	3.5	
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	231	°C / W
	Rth2 *2	69.0	
	Rth3 *3	35.5	

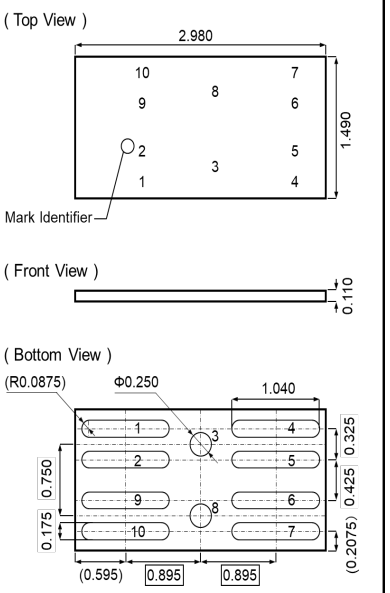
Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (42 mm^2 area, 36 μm thickness).

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (602 mm^2 area, 36 μm thickness).

*3 Mounted on Ceramic board (70 mm x 70 mm x t1.0 mm).

*4 t = 10 μs, Duty Cycle ≤ 1 %.

Unit: mm

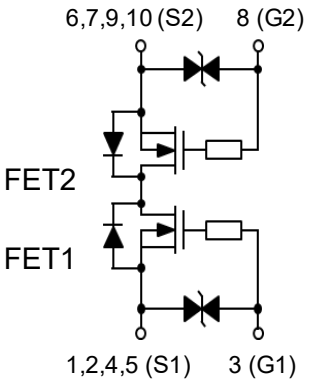


1,2,4,5. Source1 (FET1) 3. Gate1 (FET1)

6,7,9,10. Source2 (FET2) 8. Gate2 (FET2)

Package	TCSP1530011-N2
JEITA	—
Code	—

Equivalent circuit



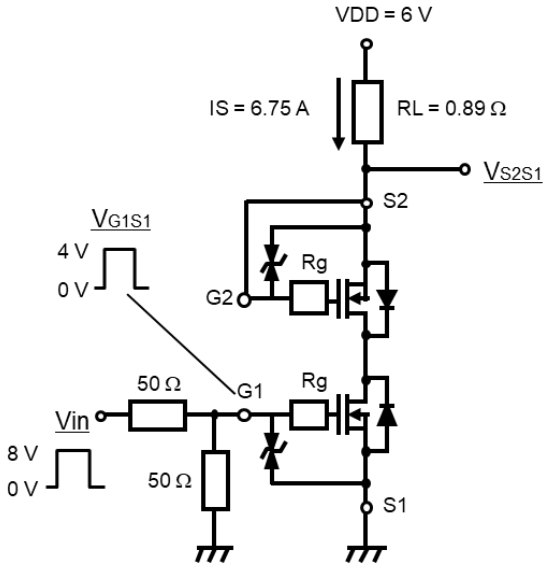
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

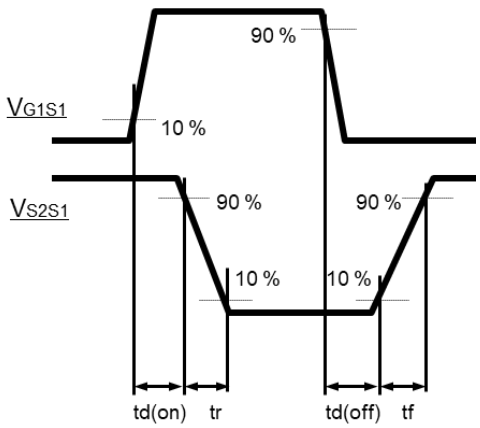
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS1	VGS = ±8 V, VSS = 0 V			±10	μA
	IGSS2	VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.79 mA, VSS = 6 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 6.75 A, VGS = 4.5 V	1.55	2.10	2.75	mΩ
	RSS(on)2	IS = 6.75 A, VGS = 3.8 V	1.60	2.20	2.85	
	RSS(on)3	IS = 6.75 A, VGS = 3.1 V	1.65	2.40	3.95	
	RSS(on)4	IS = 6.75 A, VGS = 2.5 V	1.90	3.10	6.10	
Body Diode Forward Voltage	VF(s-s)	IF = 6.75 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		4270		pF
Output Capacitance *1	Coss			690		
Reverse Transfer Capacitance *1	Crss			590		
Turn-on Delay Time *1,*2	td(on)	VDD = 6 V, VGS = 0 to 4 V		1.4		μs
Rise Time *1,*2	tr	IS = 6.75 A		2.5		
Turn-off Delay Time *1,*2	td(off)	VDD = 6 V, VGS = 4 to 0 V		6.0		μs
Fall Time *1,*2	tf	IS = 6.75 A		3.4		
Total Gate Charge *1	Qg	VDD = 6 V		33		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		11		
Gate-drain Charge *1	Qgd	IS = 13.5 A		6.0		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

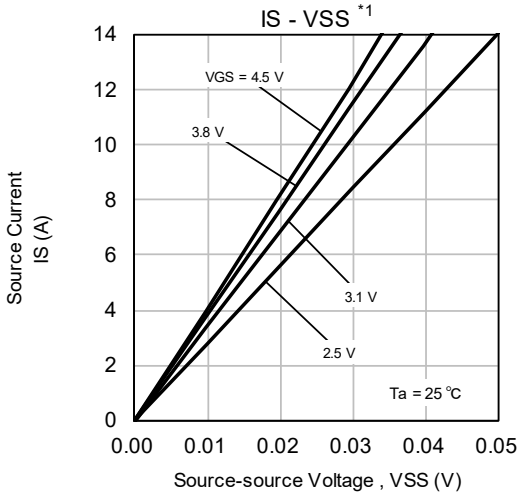
*1 Guaranteed by design, not subject to production testing

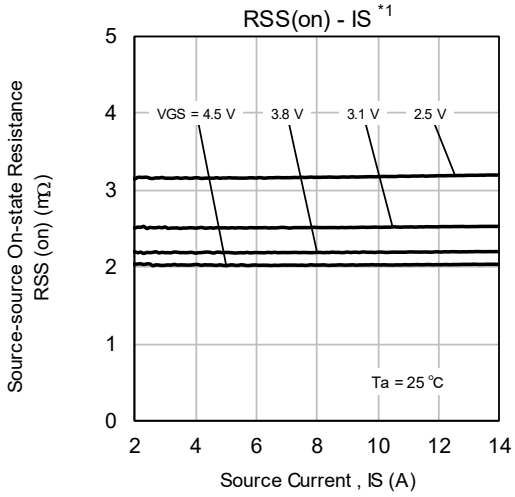
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

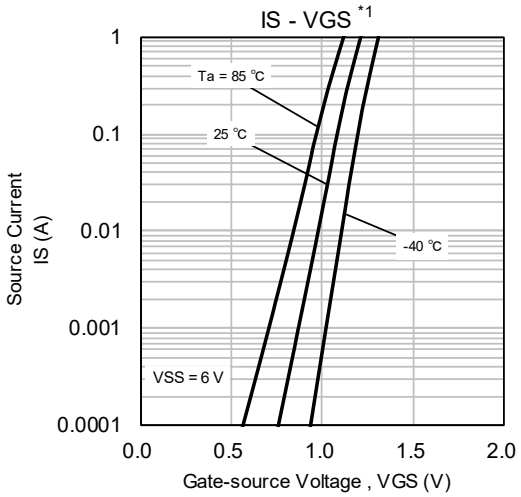


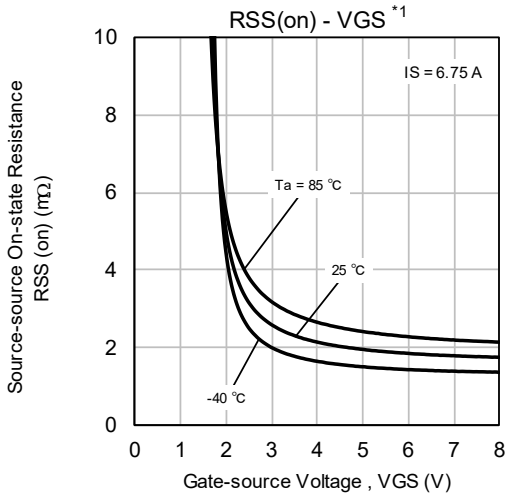


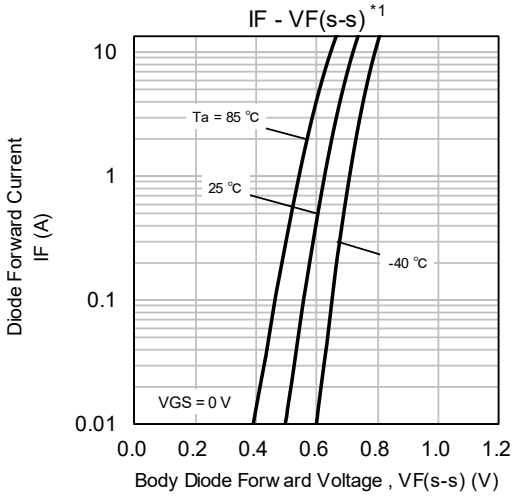
8. TECHNICAL DATA (Reference)

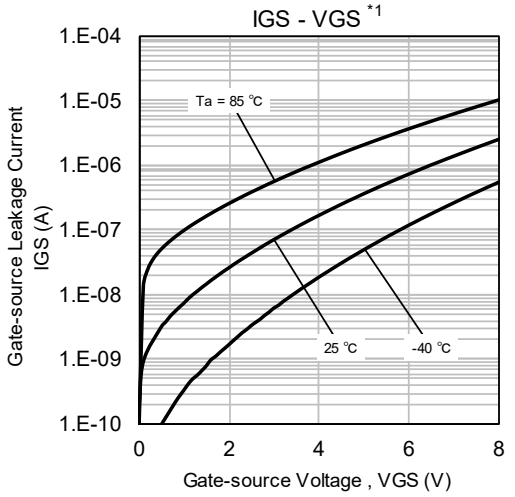












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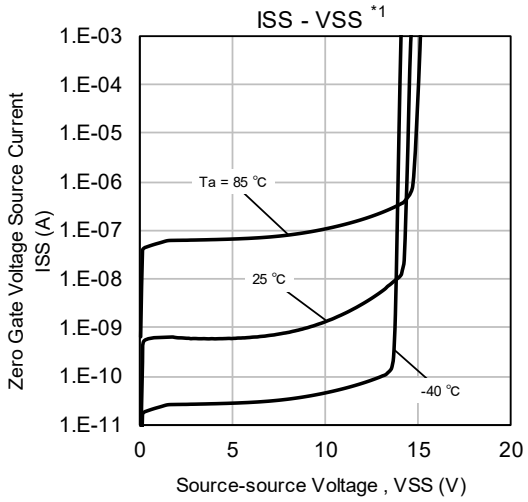
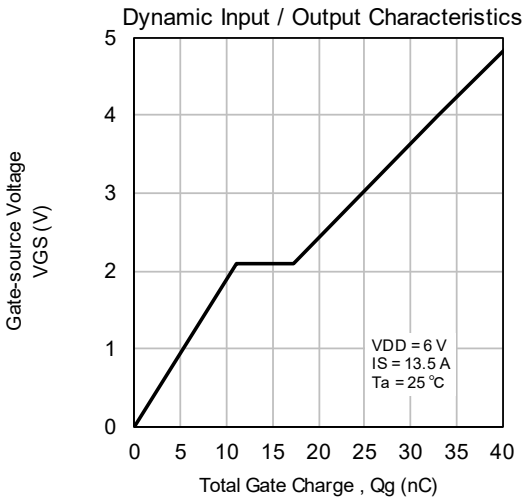
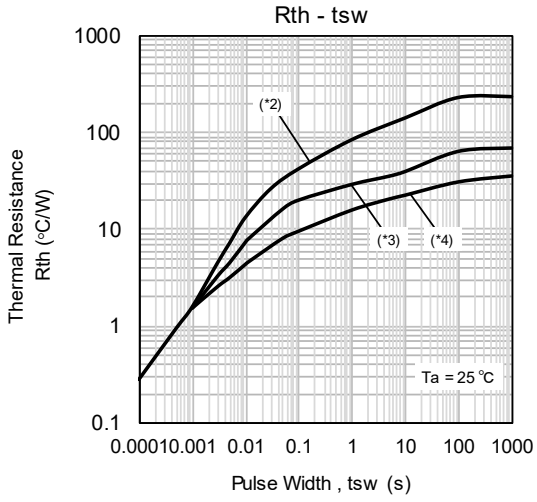
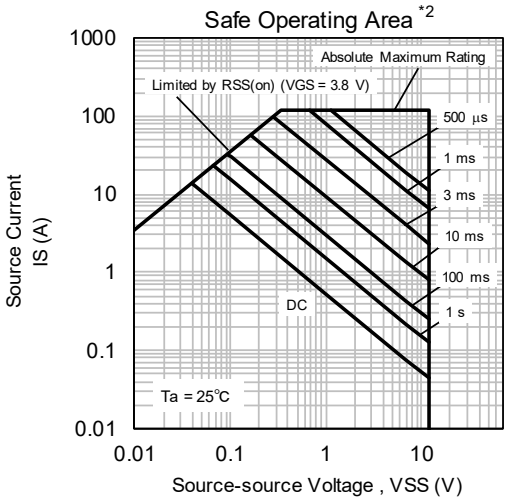
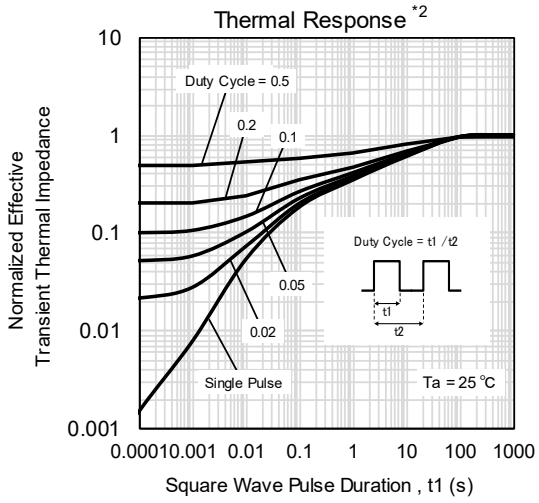










Note

*1 Pulse measurement.

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (42 mm^2 area, 36 µm thickness).

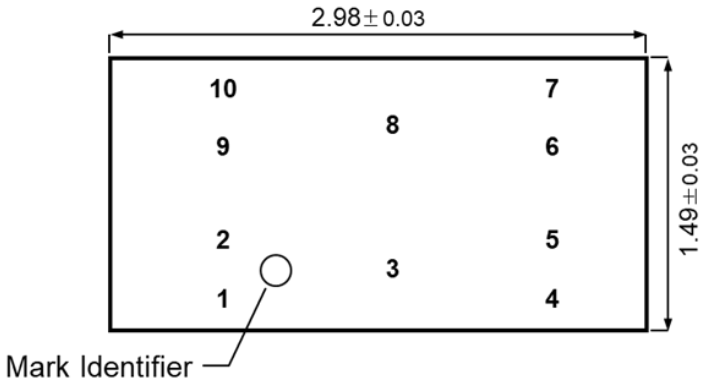
*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (602 mm^2 area, 36 µm thickness).

*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

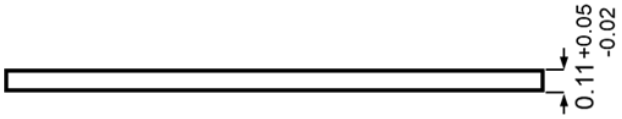
9. OUTLINE

Unit: mm

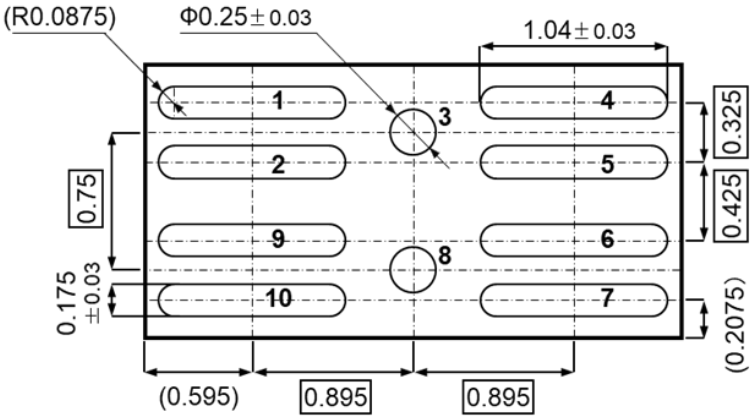
(Top View)



(Front View)

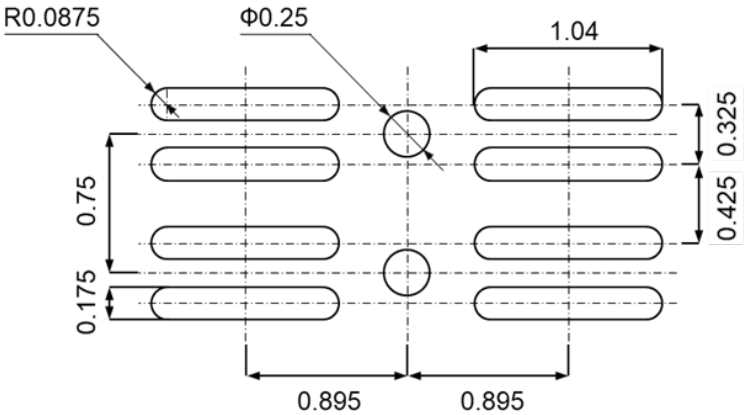


(Bottom View)



10. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.2.10	1.00	1. Initially issued.
2021.08.31	1.01	1. Changed document name from Product Standards to Datasheet. 2. Added important notice in Land Pattern. 3. Added special attention and precautions notes.

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