

Gate resistor installed Dual N-channel MOSFET

KFCAB21860L Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
For lithium-ion secondary battery protection circuits

2. FEATURES

- Source-source ON Resistance: $R_{SS(on)}$ typ. = 1.5 m Ω (V_{GS} = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: WH

4. PACKAGING

Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

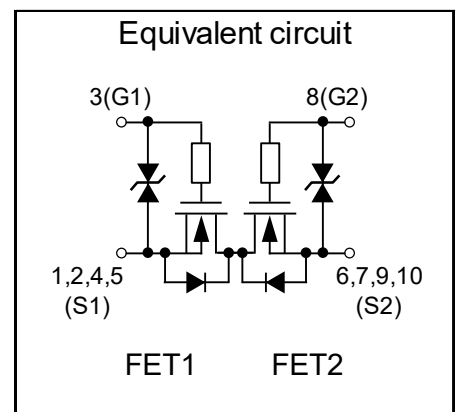
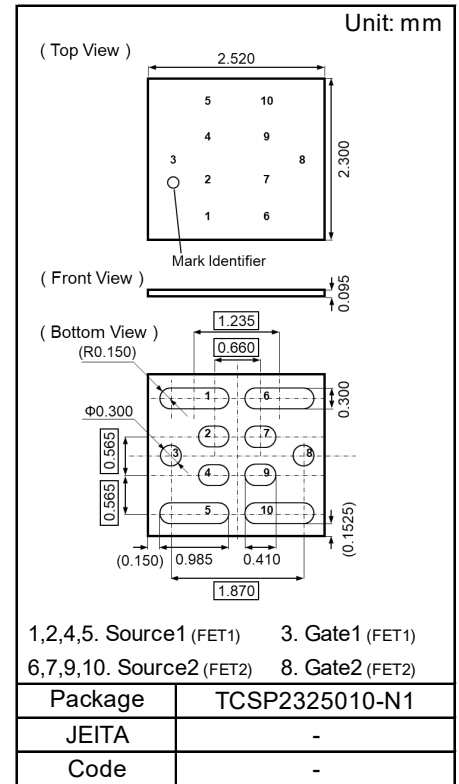
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25\text{ }^{\circ}\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	± 8	V
Source Current	DC	IS1 *1	17
		IS2 *2	30
		IS3 *3	40.5
	Pulsed *4	ISp	170
Total Power Dissipation	DC	PD1 *1	0.58
		PD2 *2	1.77
		PD3 *3	3.20
Channel Temperature	Tch	150	$^{\circ}\text{C}$
Storage Temperature Range	Tstg	-55 to +150	$^{\circ}\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth *1	215	$^{\circ}\text{C} / \text{W}$
	Rth *2	71	
	Rth *3	39	

- Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm)
FR4 board partially covered with copper pad (42 mm² area, 36 μm thickness).
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (604 mm² area, 36 μm thickness).
- *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
- *4 $t = 10\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$



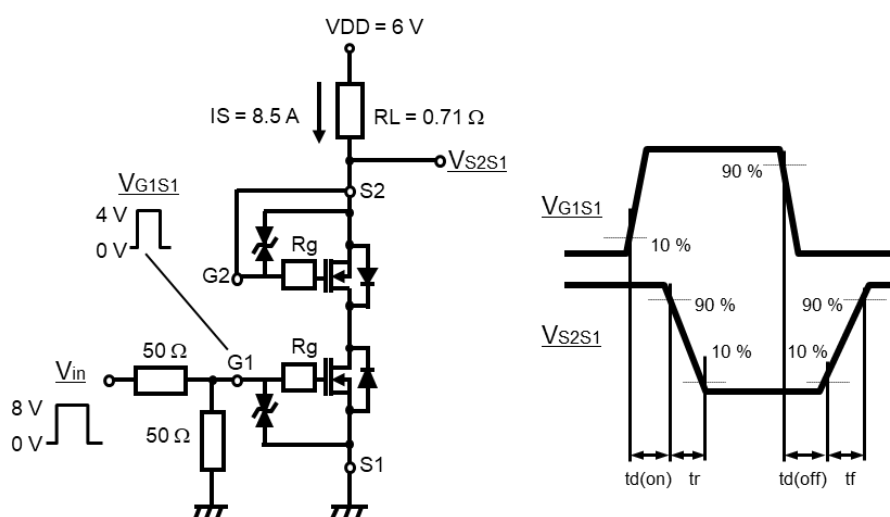
7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS1	VGS = ±8 V, VSS = 0 V			±10	μA
	IGSS2	VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 1.04 mA, VSS = 6 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 8.5 A, VGS = 4.5 V	1.00	1.35	1.75	mΩ
	RSS(on)2	IS = 8.5 A, VGS = 3.8 V	1.10	1.50	1.95	
	RSS(on)3	IS = 8.5 A, VGS = 3.1 V	1.15	1.70	2.80	
	RSS(on)4	IS = 8.5 A, VGS = 2.75 V	1.20	1.95	3.80	
	RSS(on)5	IS = 8.5 A, VGS = 2.5 V	1.40	2.25	4.50	
Body Diode Forward Voltage	VF(s-s)	IF = 8.5 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		5390		pF
Output Capacitance *1	Coss			890		
Reverse Transfer Capacitance *1	Crss			770		
Turn-on Delay Time *1,*2	td(on)	VDD = 6 V, VGS = 0 to 4 V		1.6		μs
Rise Time *1,*2	tr	IS = 8.5 A		2.6		
Turn-off Delay Time *1,*2	td(off)	VDD = 6 V, VGS = 4 to 0 V		7.5		μs
Fall Time *1,*2	tf	IS = 8.5 A		4.0		
Total Gate Charge *1	Qg	VDD = 6 V		45		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		12		
Gate-drain Charge *1	Qgd	IS = 17 A		9		

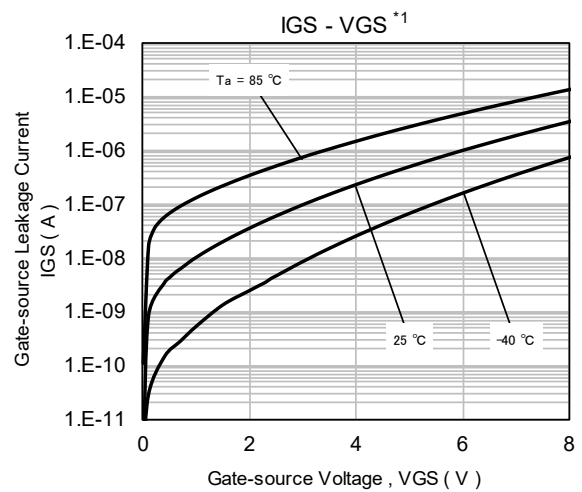
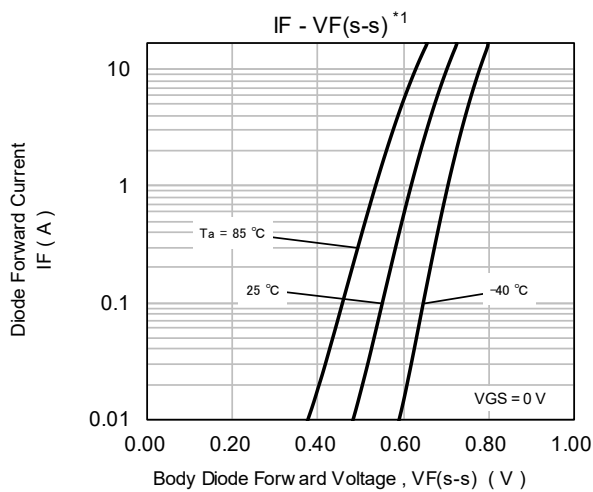
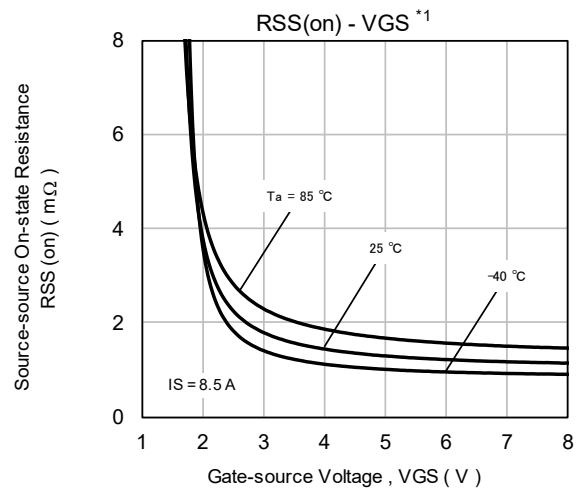
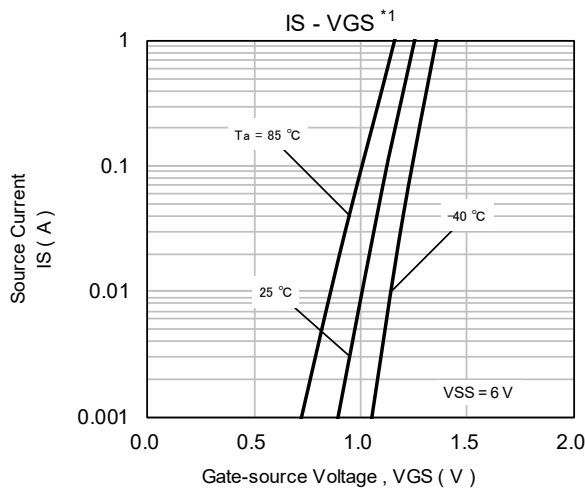
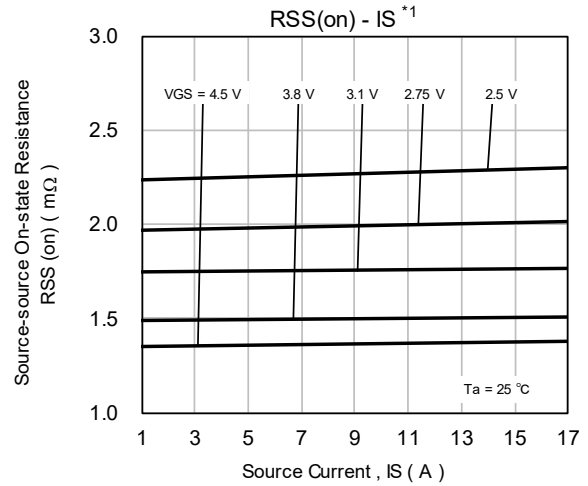
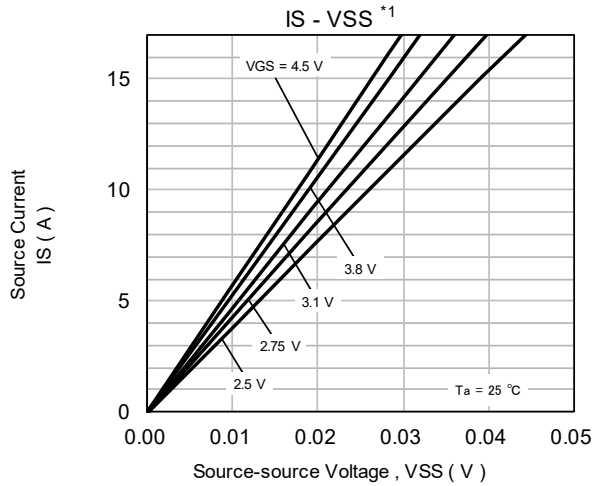
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing

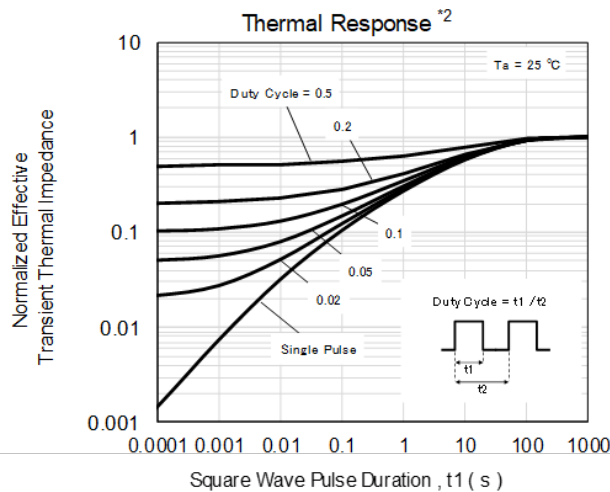
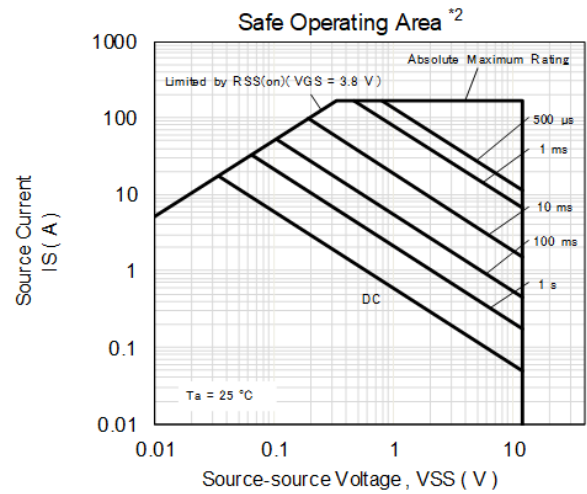
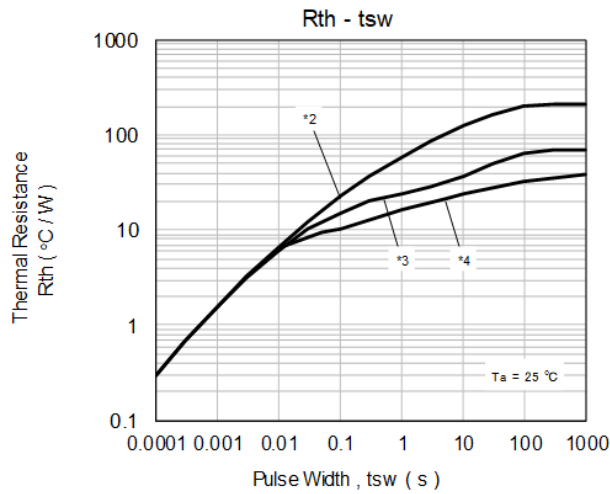
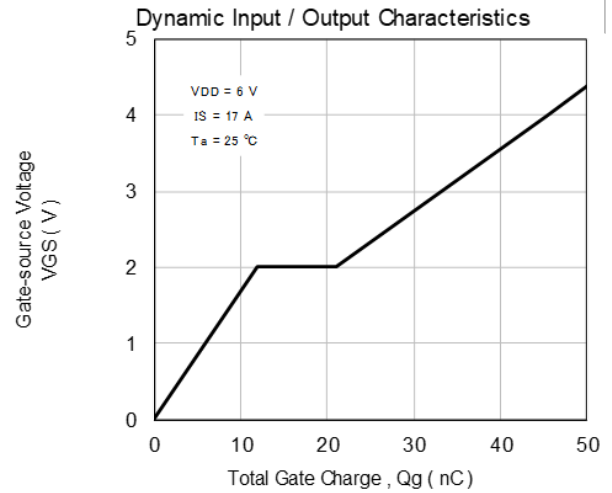
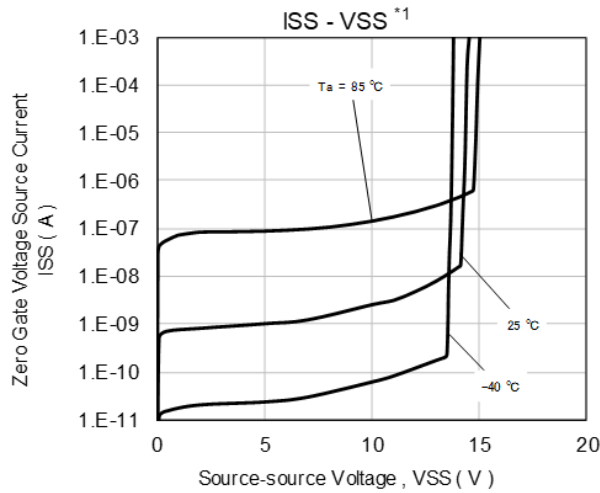
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



8. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



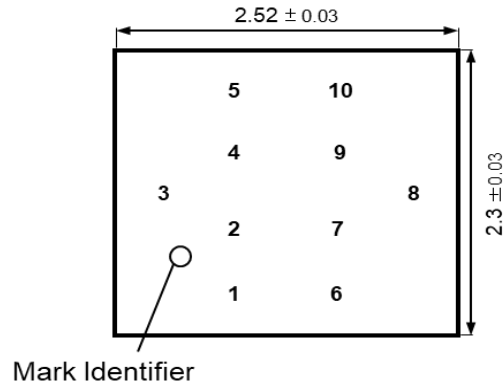
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board partially covered with copper pad
(42 mm² area, 36 µm thickness).
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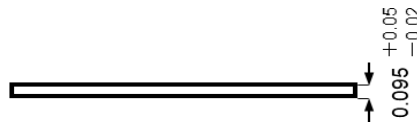
9. OUTLINE

Unit: mm

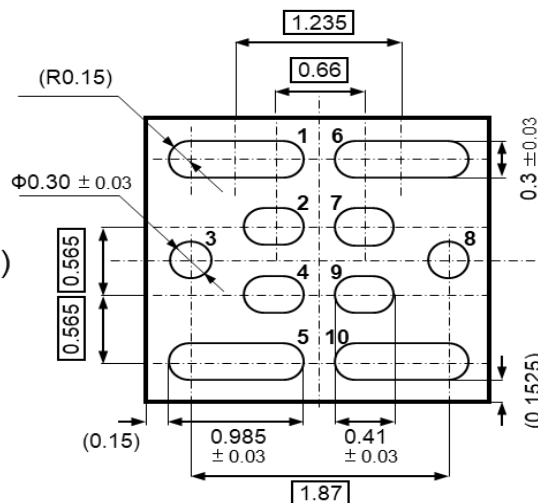
(Top View)



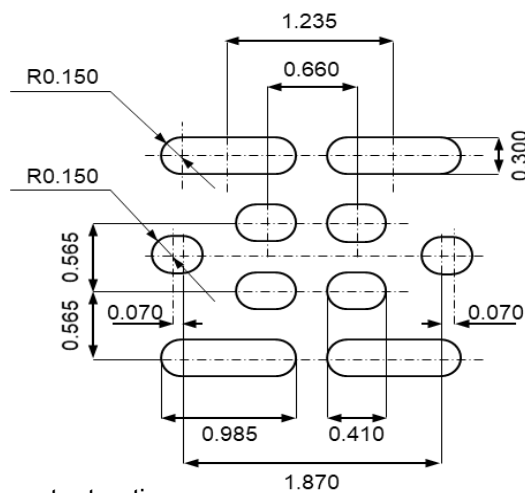
(Front View)



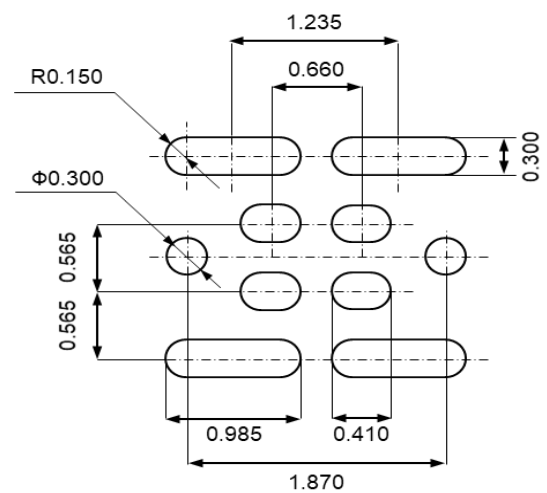
(Bottom View)



10. LAND PATTERN (Reference) Unit: mm



11. STENCIL PATTERN (Reference) Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.2.3	1.00	1. Initially issued.
2021.08.31	1.01	1. Changed document name from Product Standards to Datasheet. 2. Added important notice in Land Pattern. 3. Added special attention and precautions notes.

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