Single N-channel MOSFET

KFK4B02910L
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Gate resistor installed Single N-channel MOSFET
for lithium-ion secondary battery protection circuits.

2. FEATURES

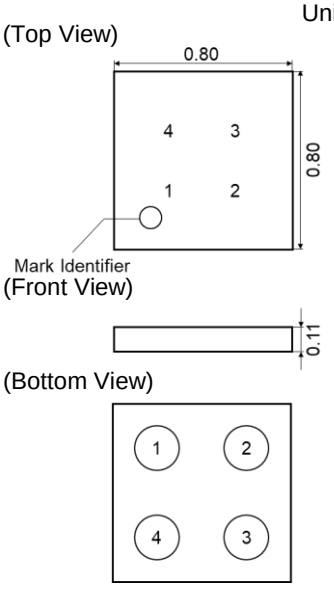
- Drain-source On-state Resistance: RDS(on) typ = 22 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: T9

4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

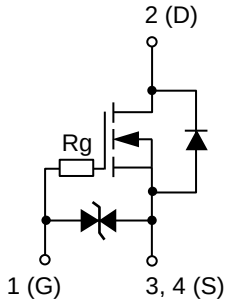
Unit: mm



1. Gate
2. Drain
3. Source
4. Source

Package	XLGA004-W-0808-RA02

Equivalent Circuit



5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	22	V
Gate-source Voltage		VGS	± 12	V
Drain Current	DC *1	ID1	3.7	A
	DC *2	ID2	5.8	
	DC *3	ID3	7.6	
	Pulsed *4	IDp	37.0	
Total Power Dissipation	DC *1	PD1	0.41	W
	DC *2	PD2	1.00	
	DC *3	PD3	1.71	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	300	°C / W
	Rth2 *2	125	
	Rth3 *3	73	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (65.7 mm^2 area, 36 µm thickness).
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (619 mm^2 area, 36 µm thickness).
*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
*4 t = 10 µs, Duty Cycle ≤ 1 %.

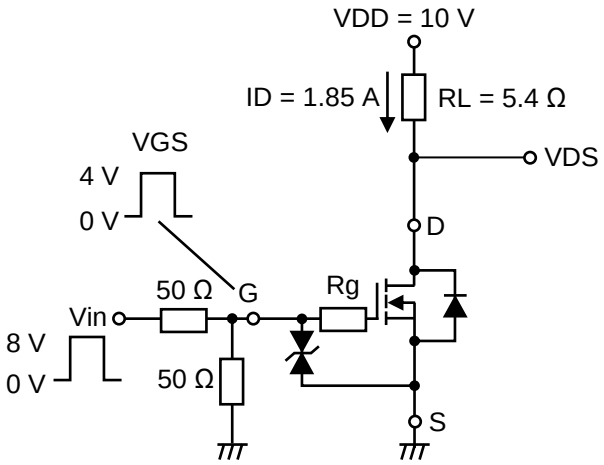
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

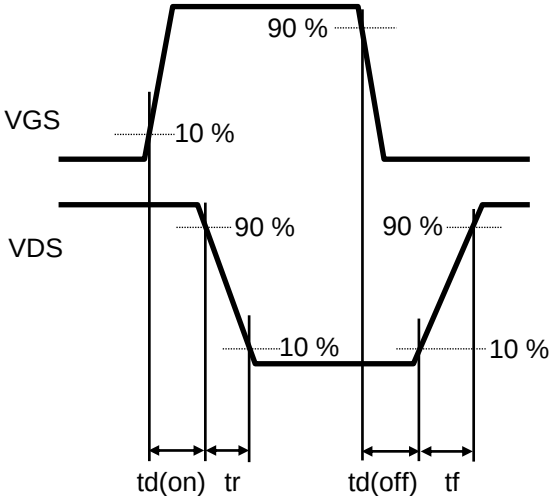
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	22			V
Zero Gate Voltage Drain Current	IDSS	VDS = 22 V, VGS = 0 V			1	µA
Gate-source Leakage Current	IGSS	VGS = ± 8 V, VDS = 0 V			± 10	µA
Gate-source Threshold Voltage	Vth	ID = 84 µA, VDS = 10 V	0.35	0.9	1.4	V
Drain-source On-state Resistance	RDS(on)1	ID = 1.85 A, VGS = 4.5 V	16	21	27	mΩ
	RDS(on)2	ID = 1.85 A, VGS = 3.8 V	17	22	28	
	RDS(on)3	ID = 1.85 A, VGS = 3.1 V	17	25	32	
	RDS(on)4	ID = 1.85 A, VGS = 2.5 V	18	31	61	
Body Diode Forward Voltage	VF(s-d)	IF = 1.85 A, VGS = 0 V		0.75	1.00	V
Input Capacitance *1	Ciss	VDS = 10 V, VGS = 0 V f = 1 kHz		540		pF
Output Capacitance *1	Coss			80		
Reverse Transfer Capacitance *1	Crss			70		
Turn-on Delay Time *1, *2	td(on)	VDD = 10 V, VGS = 0 to 4 V ID = 1.85 A		170		ns
Rise Time *1, *2	tr			290		
Turn-off Delay Time *1, *2	td(off)	VDD = 10 V, VGS = 4 to 0 V ID = 1.85 A		730		
Fall Time *1, *2	tf			530		
Total Gate Charge *1	Qg	VDD = 10 V, VGS = 4 V ID = 3.7 A		5.0		nC
Gate-source Charge *1	Qgs			1.2		
Gate-drain Charge *1	Qgd			1.6		
Gate Resistance *1	Rg	f = 1 MHz	400	700	1000	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

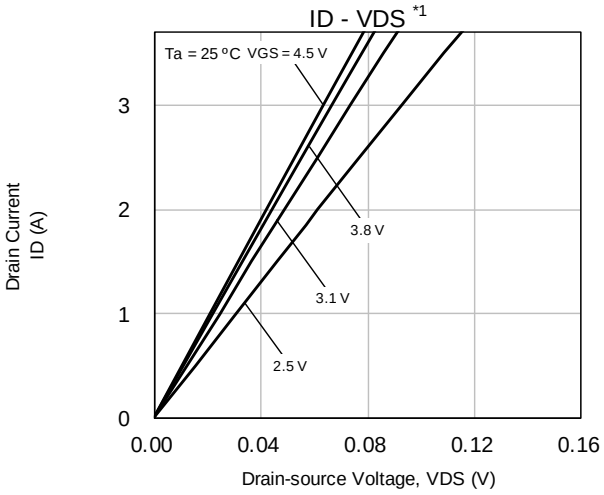


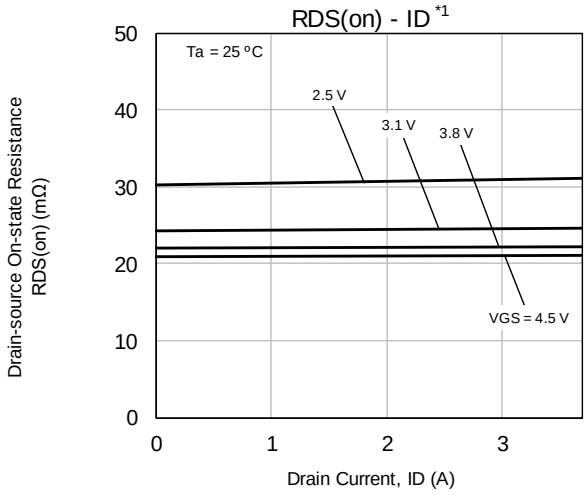


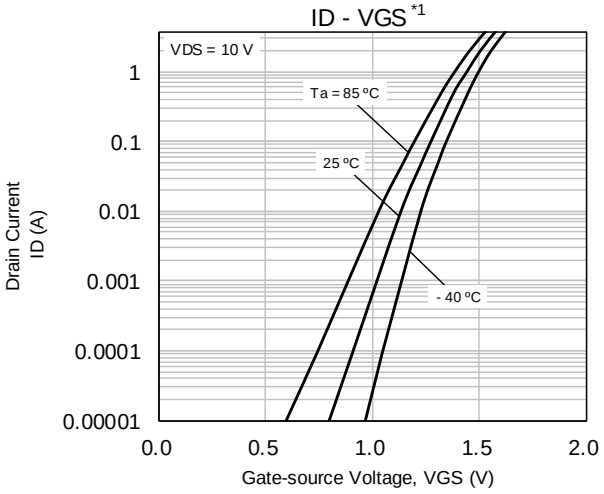
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

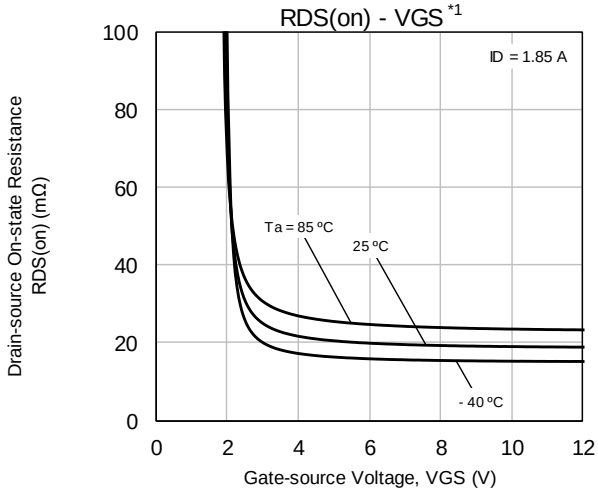
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H2	> 2 to ≤ 4	kV

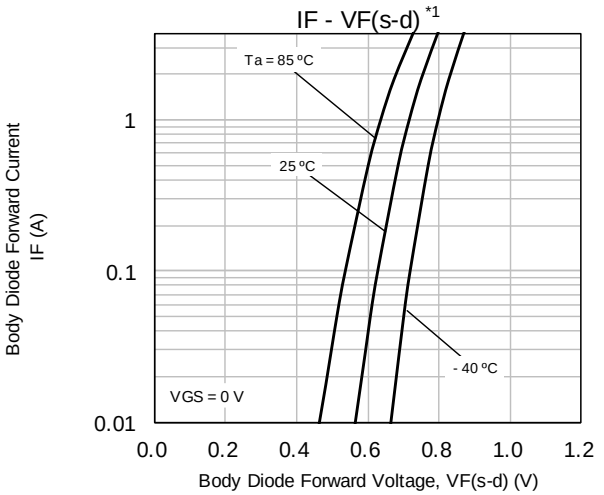
9. TECHNICAL DATA (Reference)

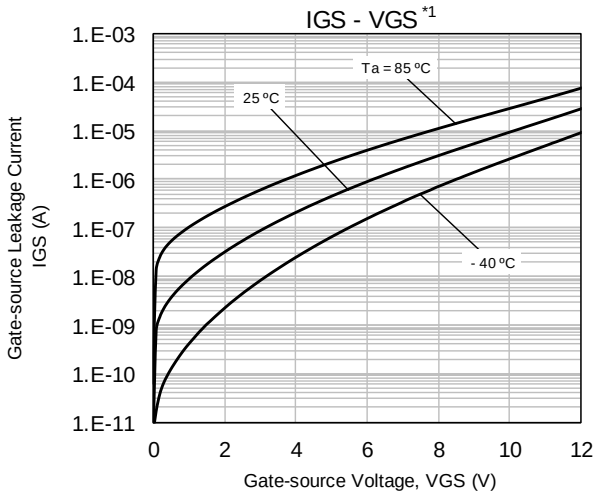












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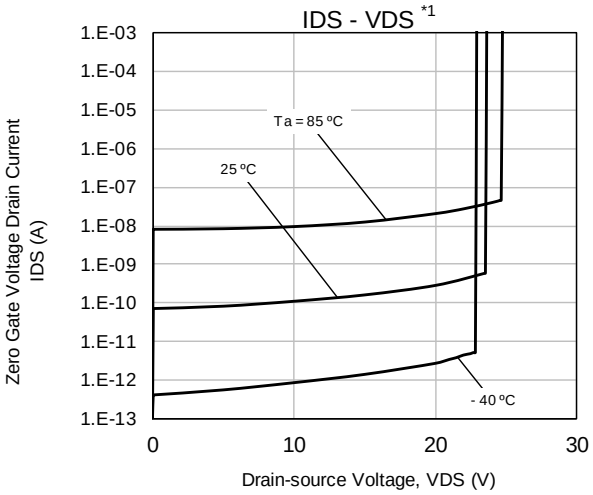

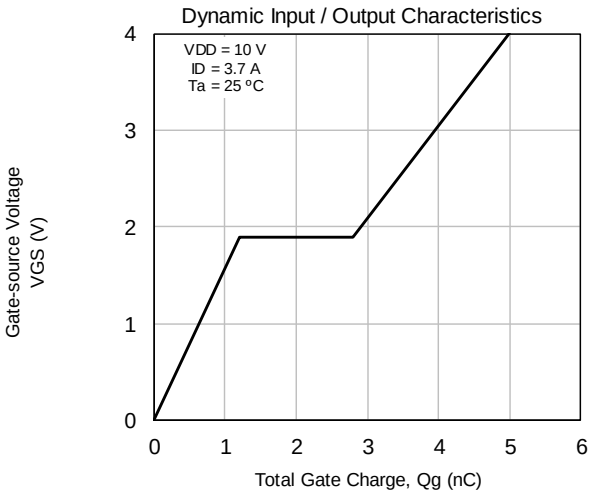

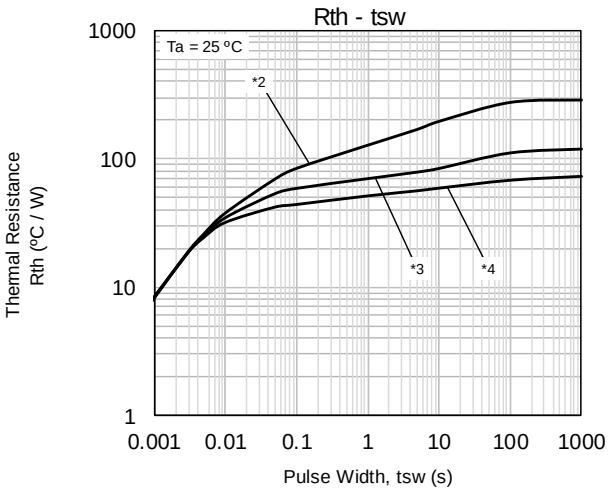

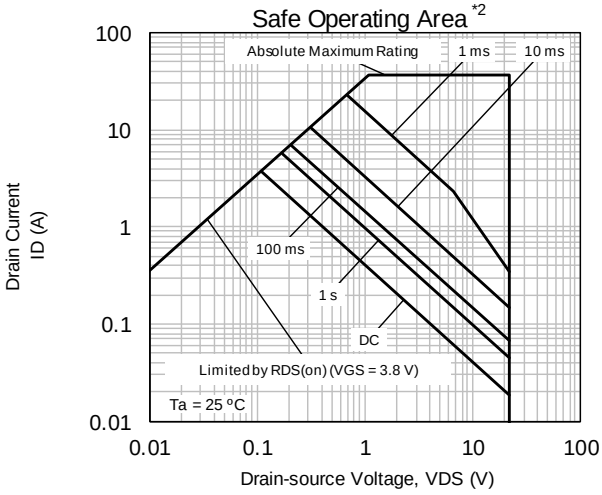

Note

*1 Pulse measurement.

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (65.7 mm^2 area, 36 µm thickness).

*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
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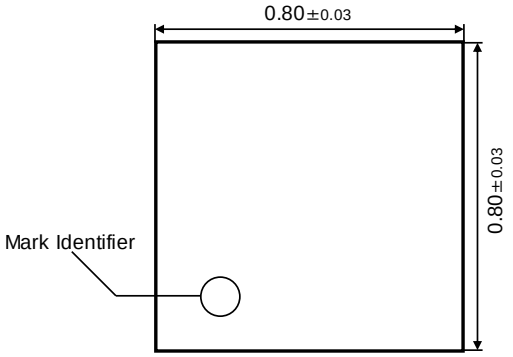
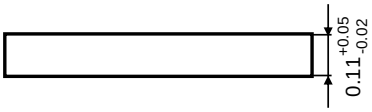
*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

10. OUTLINE

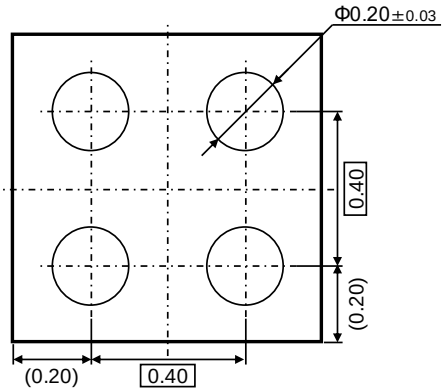
(Top View) Unit: mm



(Front View)

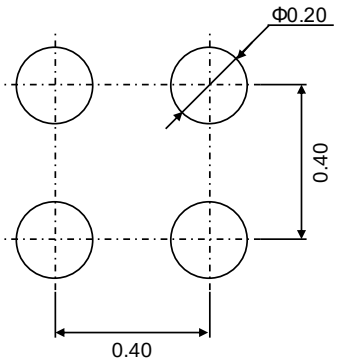


(Bottom View)



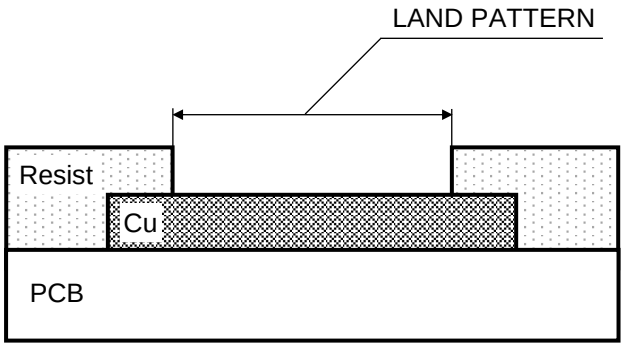
11. LAND *1 & STENCIL PATTERN (Reference)

Unit: mm



Note *1 The definition of land pattern is referred to next page.

DEFINITION OF LAND PATTERN



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2022.8.22	1.00	1. Initially issued.

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