Single N-channel MOSFET

KFK4A12035NL
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

1. GENERAL DESCRIPTION

Single N-channel MOSFET.

2. FEATURES

- Drain-source On-state Resistance: RDS(on) typ = 28 mΩ (VGS = 4.5 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

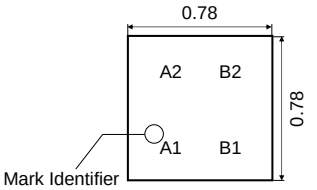
3. MARKING SYMBOL: TE

4. PACKAGING

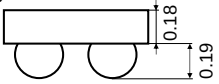
Embossed type (Thermo-compression sealing): 13,000 pcs / reel (standard)

Unit: mm

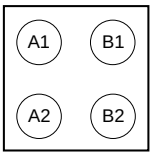
(Top View)



(Front View)



(Bottom View)

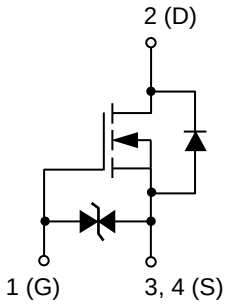


A1. Gate B1. Drain

A2, B2. Source

Package	XBGA004-W-0808AQB

Equivalent Circuit



5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	12	V
Gate-source Voltage		VGS	+ 8 / - 4	V
Drain Current	DC *1	ID1	3.4	A
	DC *2	ID2	5.3	
	DC *3	ID3	6.8	
	Pulsed *4	IDp	34	
Total Power Dissipation	DC *1	PD1	0.43	W
	DC *2	PD2	1.00	
	DC *3	PD3	1.65	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	290	°C / W
	Rth2 *2	125	
	Rth3 *3	76	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (65.7 mm^2 area, 36 µm thickness).

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (619 mm^2 area, 36 µm thickness).

*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

*4 t = 10 µs, Duty Cycle ≤ 1 %.

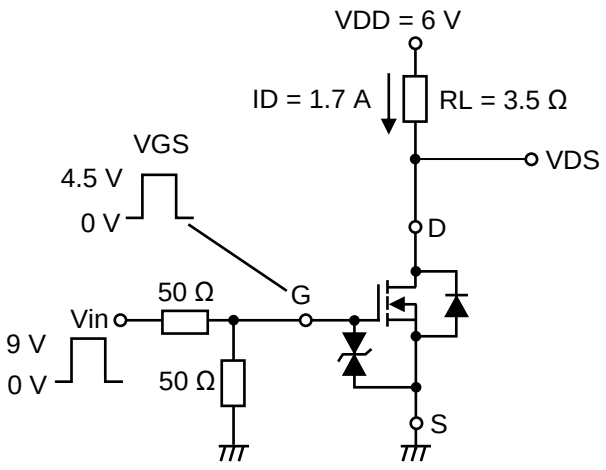
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

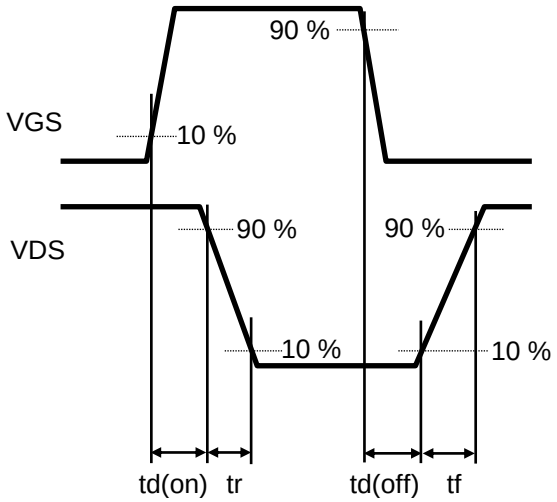
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Drain Current	IDSS	VDS = 12 V, VGS = 0 V			1	µA
Gate-source Leakage Current	IGSS	VGS = + 8 V, VDS = 0 V			10	µA
		VGS = - 4 V, VDS = 0 V			- 1	
Gate-source Threshold Voltage	Vth	ID = 0.20 mA, VDS = 6 V	0.3	0.51	0.72	V
Drain-source On-state Resistance	RDS(on)1	ID = 1.7 A, VGS = 4.5 V	21	28	35	mΩ
	RDS(on)2	ID = 1.7 A, VGS = 2.5 V	26	35	44	
	RDS(on)3	ID = 0.5 A, VGS = 1.8 V	33	44	60	
	RDS(on)4	ID = 0.25 A, VGS = 1.5 V	41	53	91	
Body Diode Forward Voltage	VF(s-d)	IF = 1.7 A, VGS = 0 V		0.71	0.89	V
Input Capacitance *1	Ciss	VDS = 10 V, VGS = 0 V f = 1 MHz		250		pF
Output Capacitance *1	Coss			95		
Reverse Transfer Capacitance *1	Crss			65		
Turn-on Delay Time *1, *2	td(on)	VDD = 6 V, VGS = 0 to 4.5 V ID = 1.7 A		7		ns
Rise Time *1, *2	tr			6		
Turn-off Delay Time *1, *2	td(off)	VDD = 6 V, VGS = 4.5 to 0 V ID = 1.7 A		100		
Fall Time *1, *2	tf			80		
Total Gate Charge *1	Qg	VDD = 6 V, VGS = 4.5 V ID = 3.4 A		3.7		nC
Gate-source Charge *1	Qgs			0.5		
Gate-drain Charge *1	Qgd			0.7		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

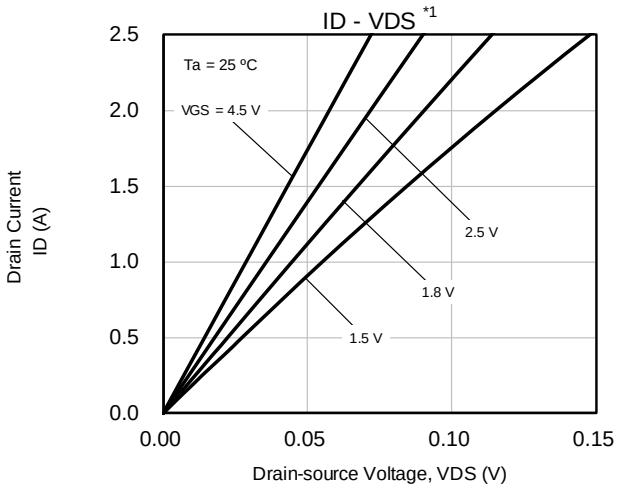


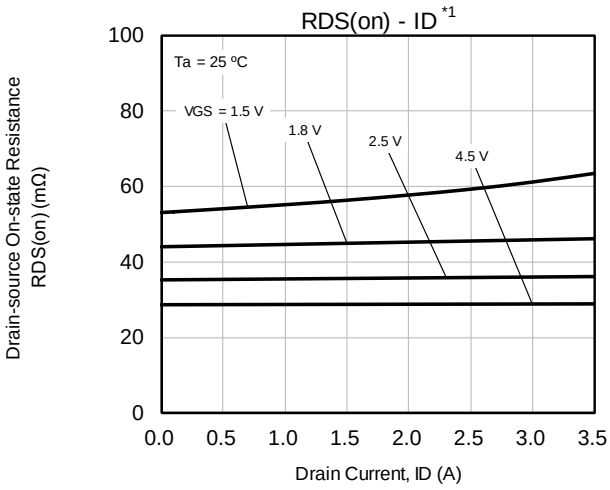


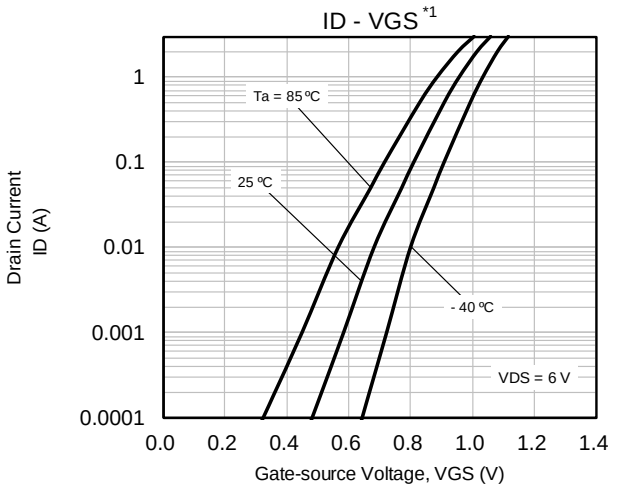
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

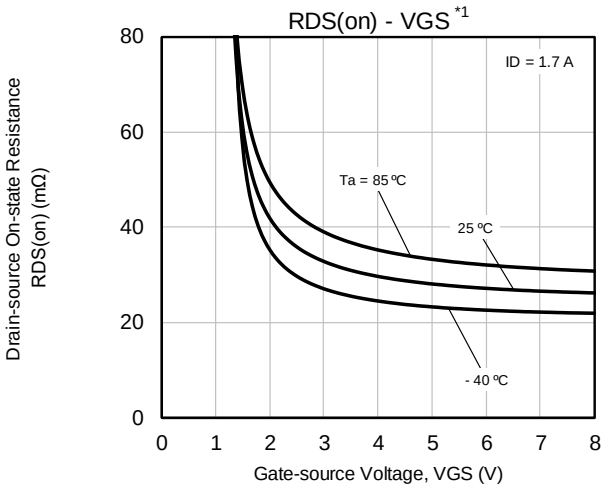
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H2	> 2k to ≤ 4k	V

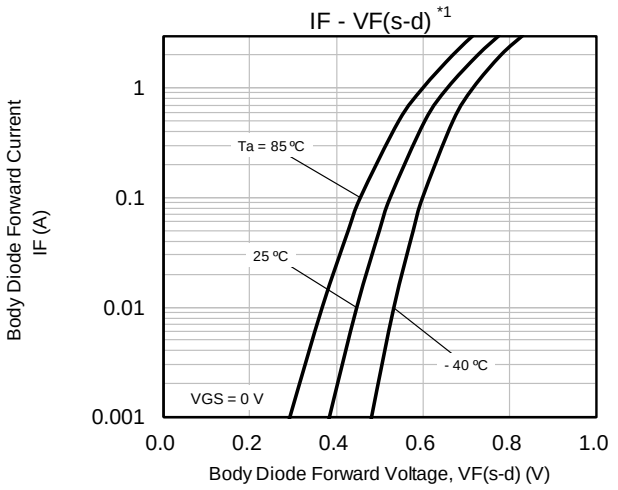
9. TECHNICAL DATA (Reference)

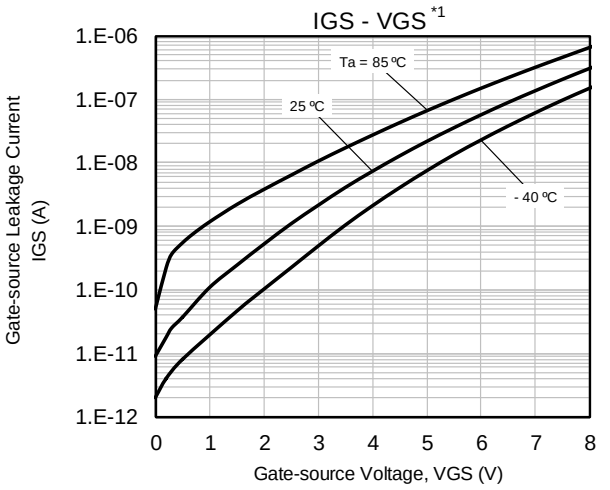




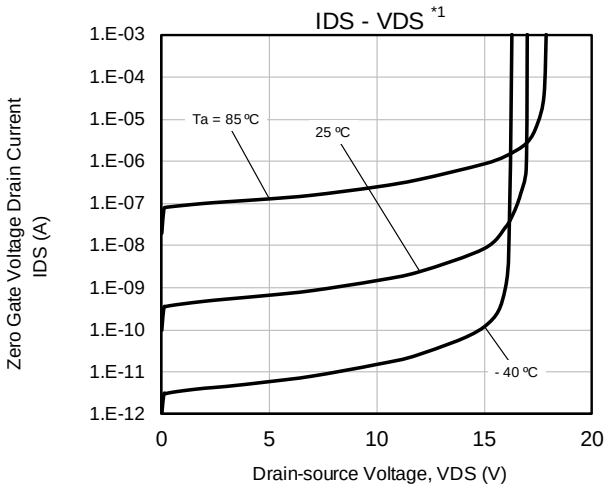


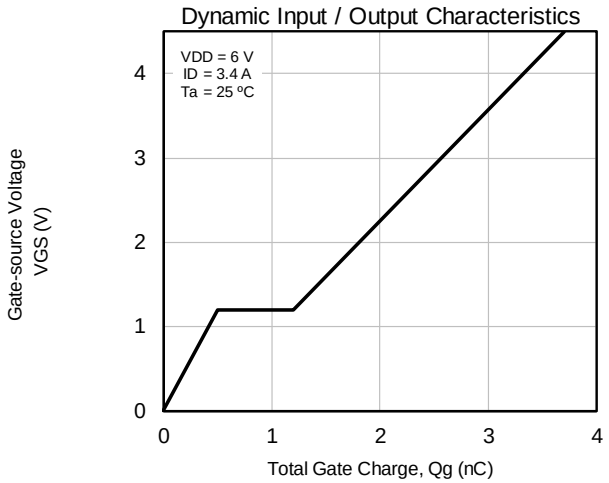


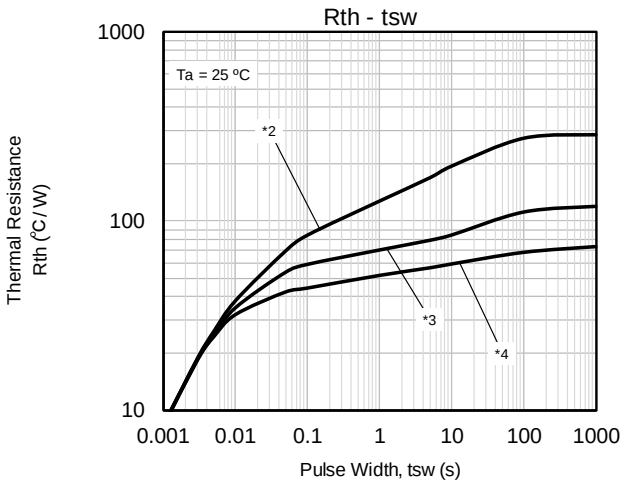


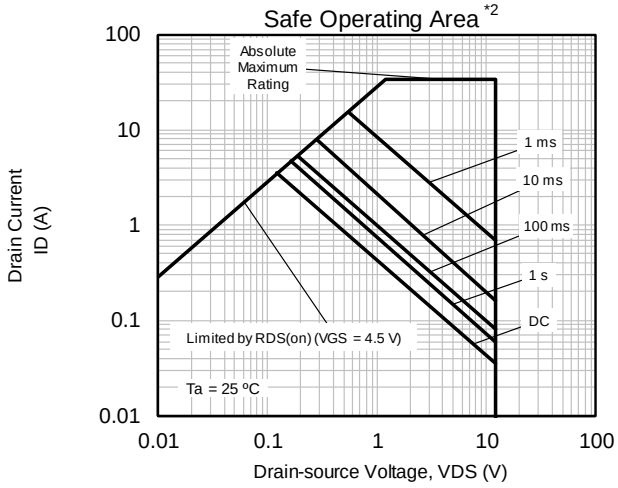


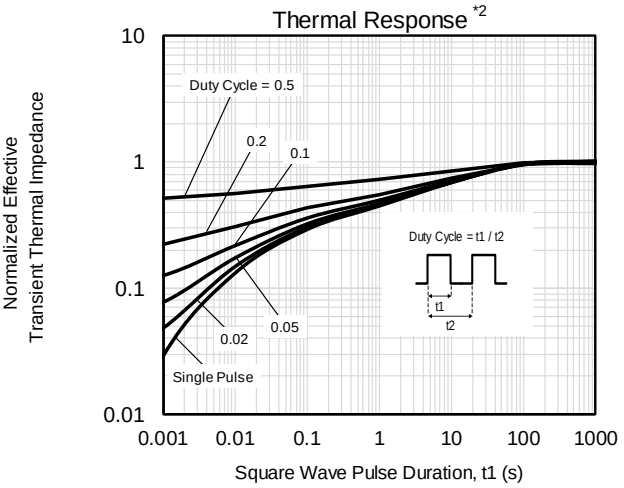
TECHNICAL DATA (Reference)











Note

*1 Pulse measurement.

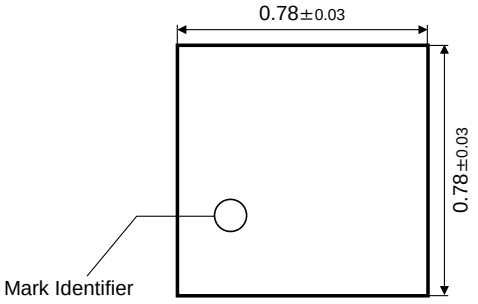
*2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board partially covered with copper pad
(65.7 mm^2 area, 36 µm thickness).

*3 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board fully covered with copper pad
(619 mm^2 area, 36 µm thickness).

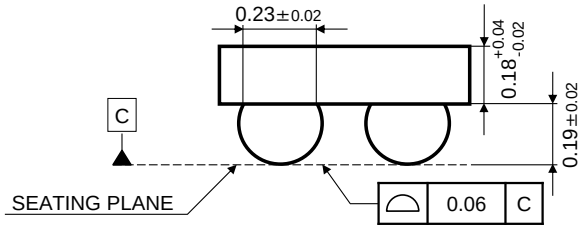
*4 Mounted on ceramic board (70 mm × 70 mm × t1.0 mm).

10. OUTLINE

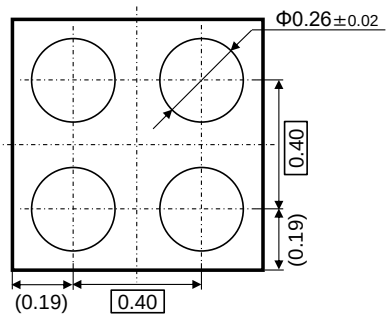
(Top View) Unit: mm



(Front View)

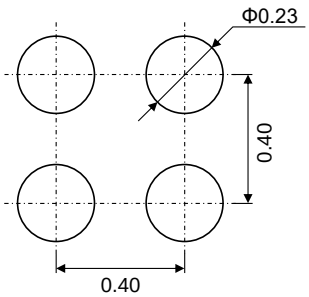


(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. MANUFACTURING LOCATION

Fabrication Site	TPSCo / Toyama
Packaging Site	TPSCo / Niigata

- Fabrication Site

  TPSCo / Toyama

  Company: Tower Partners Semiconductor Co., Ltd.

  Address: 271 Higashi-kaihotsu, Tonami City, Toyama JAPAN

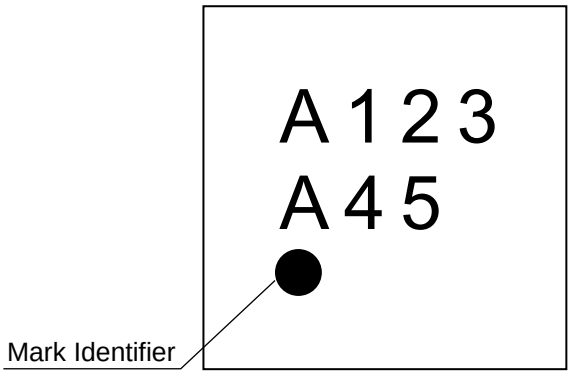
- Packaging Site

  TPSCo / Niigata

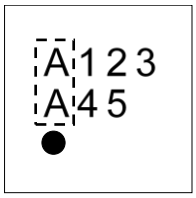
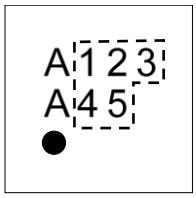
  Company: Tower Partners Semiconductor Co., Ltd.

  Address: 4-5-1 Kuribara, Myoko City, Niigata JAPAN

13. MARK LAYOUT

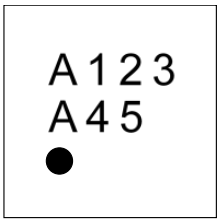


- Description of format

	Marking Symbol	Diffusion lot ID
Diagram		

Note Actual font of the product symbols may differ slightly from the one shown in this specification.

- Factory Distinction Mark

		Fabrication Site
		TPSCo / Toyama
Packaging Site	TPSCo / Niigata	

14. REVISION HISTORY

Date	Revision	Description
2023.3.13	1.00	1. Initially issued.
2023.5.9	1.01	1. Revised TECHNICAL DATA.

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