

Dual N-channel MOSFET

KFCAB22020NL Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: $R_{SS(on)}$ typ = 1.90 m Ω (V_{GS} = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: RL

4. PACKAGING

Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

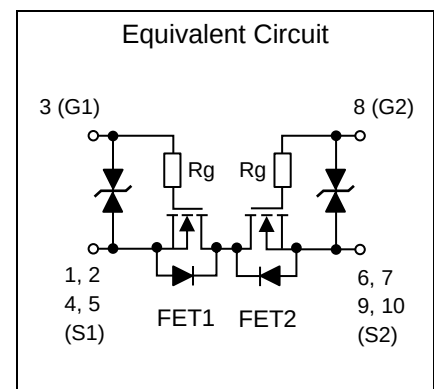
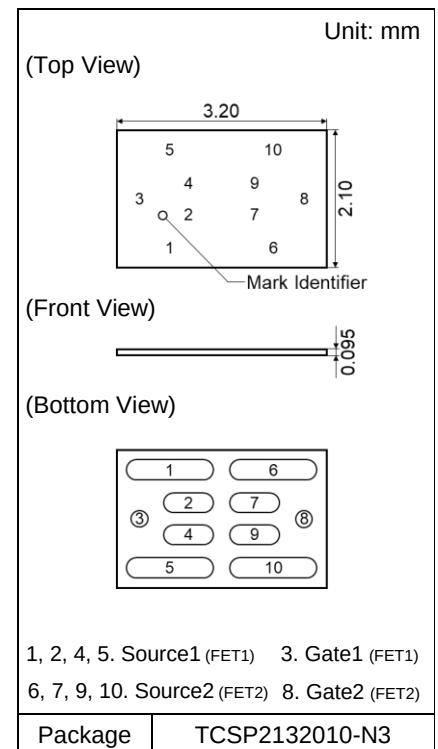
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	22	V
Gate-source Voltage	VGS	± 12	V
Source Current	DC *1	IS1	A
	DC *2	IS2	
	DC *3	IS3	
	Pulsed *4	ISp	
Total Power Dissipation	DC *1	PD1	W
	DC *2	PD2	
	DC *3	PD3	
Operating Junction and Storage Temperature Range	Tj, Tstg	- 55 to + 150	$^\circ\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	212	$^\circ\text{C} / \text{W}$
	Rth2 *2	66	
	Rth3 *3	36	

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (42 mm² area, 36 μm thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (605 mm² area, 36 μm thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$.



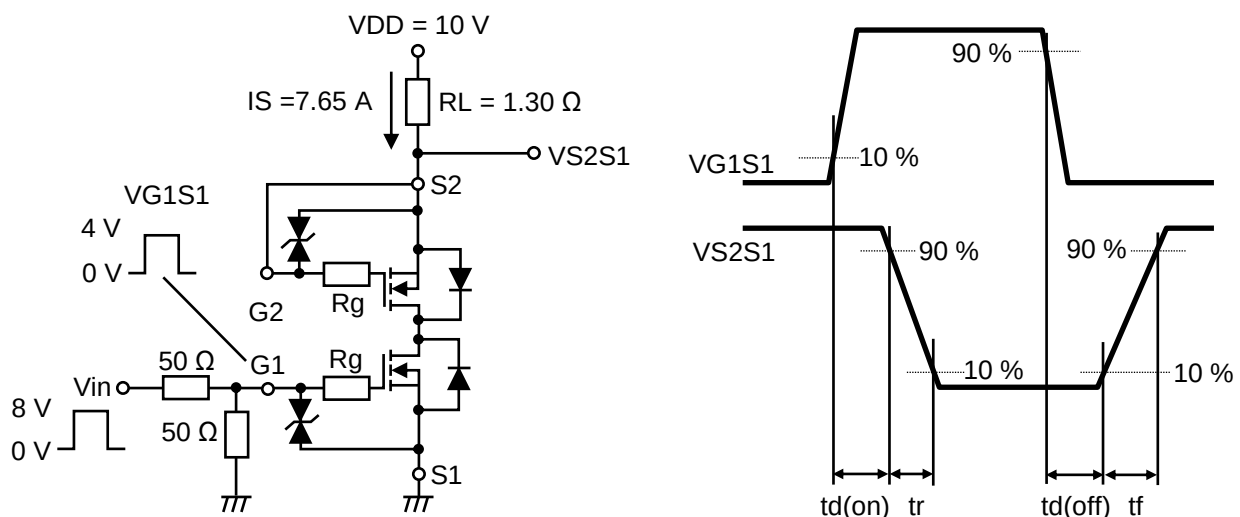
7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	$I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	22			V
Zero Gate Voltage Source Current	ISSS	$V_{SS} = 22\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
Gate-source Leakage Current	IGSS1	$V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$			± 10	μA
	IGSS2	$V_{GS} = \pm 5\text{ V}$, $V_{SS} = 0\text{ V}$			± 1	
Gate-source Threshold Voltage	V_{th}	$I_S = 1.21\text{ mA}$, $V_{SS} = 10\text{ V}$	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	$I_S = 7.65\text{ A}$, $V_{GS} = 4.5\text{ V}$	1.20	1.80	2.35	m Ω
	RSS(on)2	$I_S = 7.65\text{ A}$, $V_{GS} = 3.8\text{ V}$	1.25	1.90	2.50	
	RSS(on)3	$I_S = 7.65\text{ A}$, $V_{GS} = 3.1\text{ V}$	1.30	2.05	3.30	
	RSS(on)4	$I_S = 7.65\text{ A}$, $V_{GS} = 2.5\text{ V}$	1.40	2.40	5.25	
Body Diode Forward Voltage	$V_{F(s-s)}$	$I_F = 7.65\text{ A}$, $V_{GS} = 0\text{ V}$		0.7	1.0	V
Input Capacitance ^{*1}	C_{iss}	$V_{SS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ kHz}$		7500		pF
Output Capacitance ^{*1}	C_{oss}			570		
Reverse Transfer Capacitance ^{*1}	C_{rss}			520		
Turn-on Delay Time ^{*1, *2}	$t_{d(on)}$	$V_{DD} = 10\text{ V}$, $V_{GS} = 0\text{ to }4\text{ V}$ $I_S = 7.65\text{ A}$		40		ns
Rise Time ^{*1, *2}	t_r			200		
Turn-off Delay Time ^{*1, *2}	$t_{d(off)}$	$V_{DD} = 10\text{ V}$, $V_{GS} = 4\text{ to }0\text{ V}$ $I_S = 7.65\text{ A}$		740		ns
Fall Time ^{*1, *2}	t_f			320		
Total Gate Charge ^{*1}	Q_g	$V_{DD} = 10\text{ V}$ $V_{GS} = 0\text{ to }4\text{ V}$ $I_S = 15.3\text{ A}$		67		nC
Gate-source Charge ^{*1}	Q_{gs}			13		
Gate-drain Charge ^{*1}	Q_{gd}			14		
Gate Resistance ^{*1}	R_g	$f = 1\text{ MHz}$	4	9	17	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

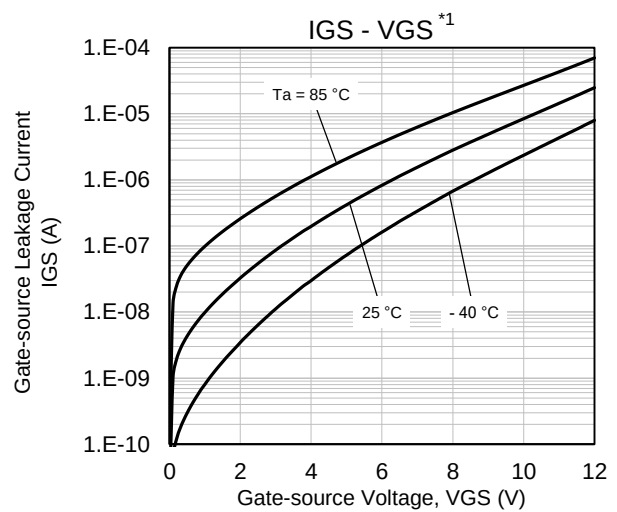
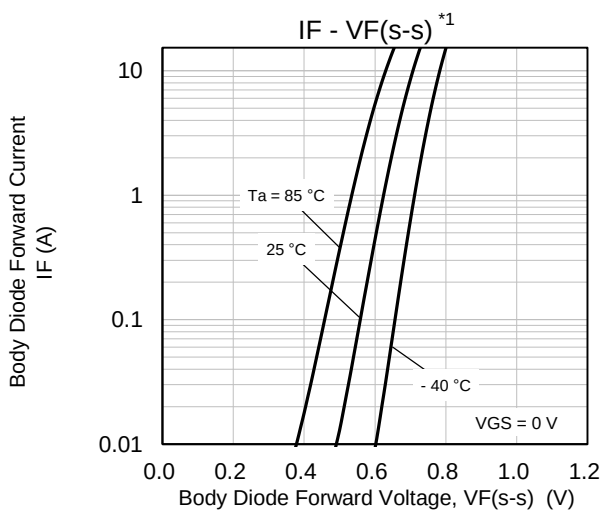
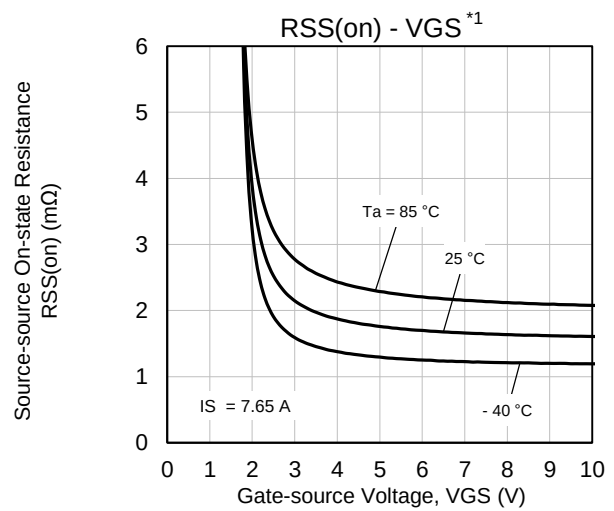
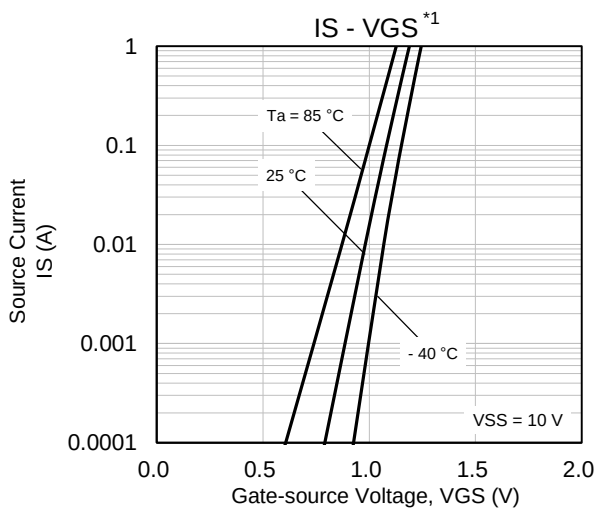
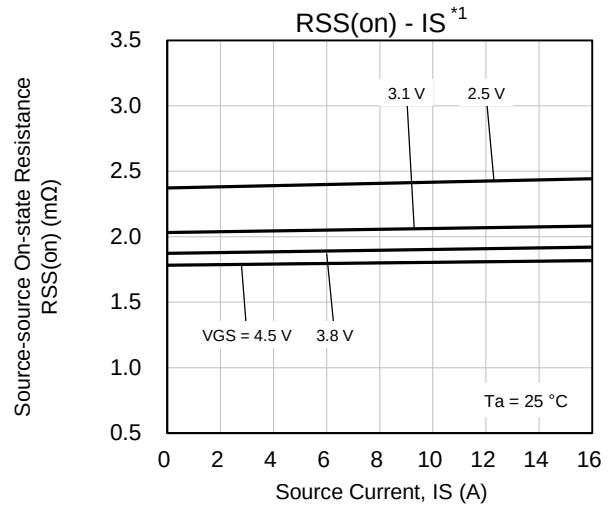
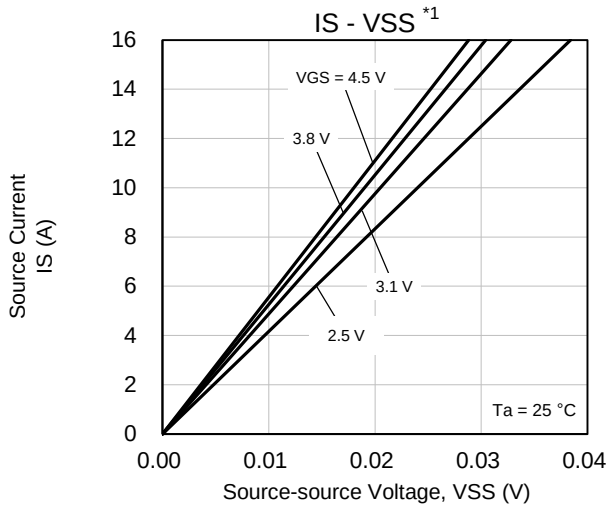
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



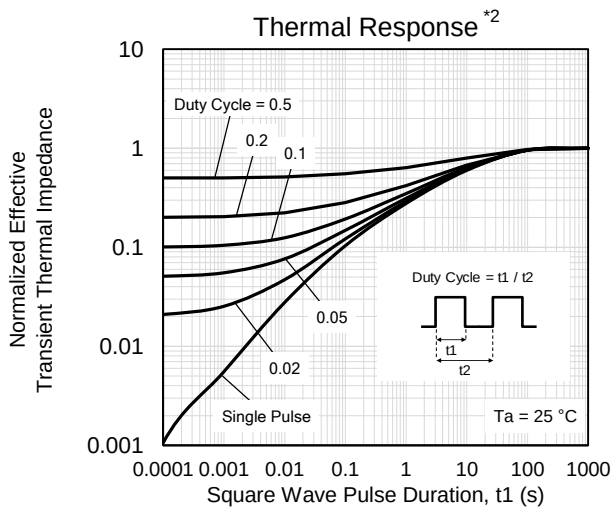
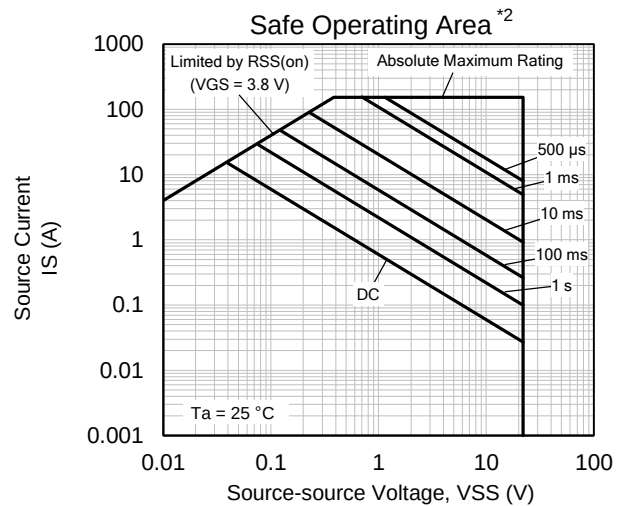
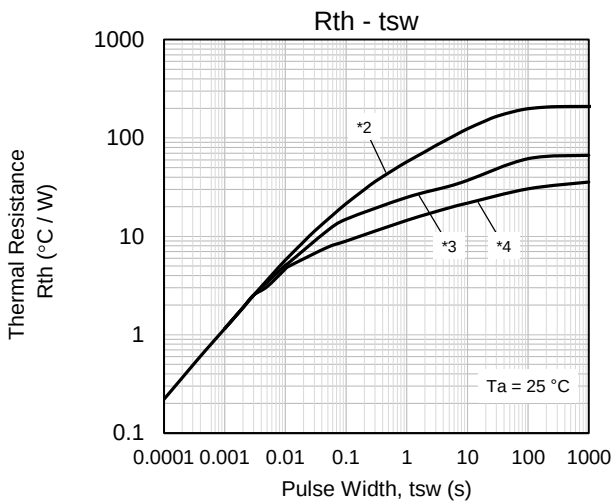
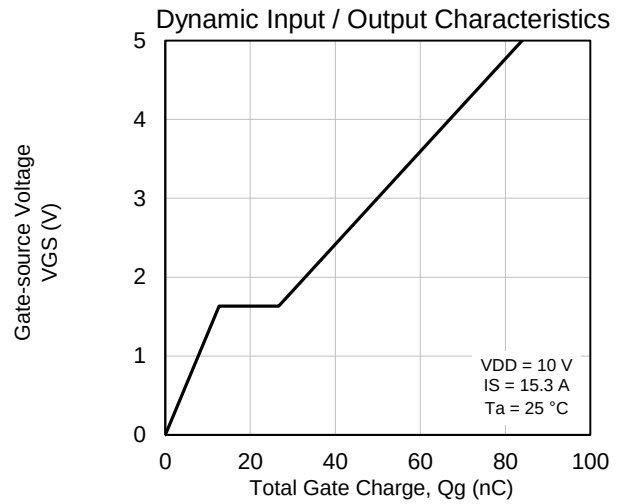
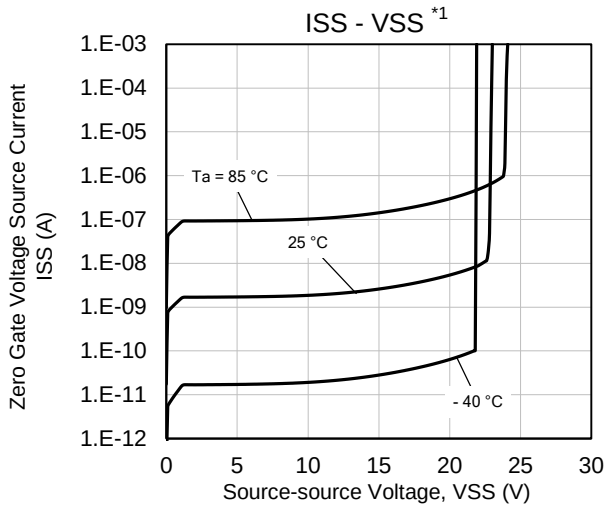
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	$C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$	H2	$> 2\text{ k to } \leq 4\text{ k}$	V

9. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



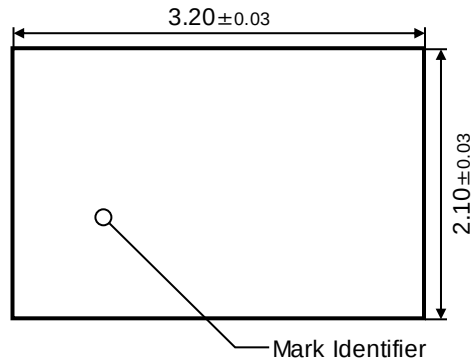
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (42 mm² area, 36 μm thickness).
- *3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (605 mm² area, 36 μm thickness).
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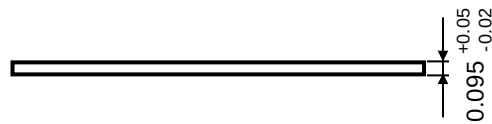
10. OUTLINE

(Top View)

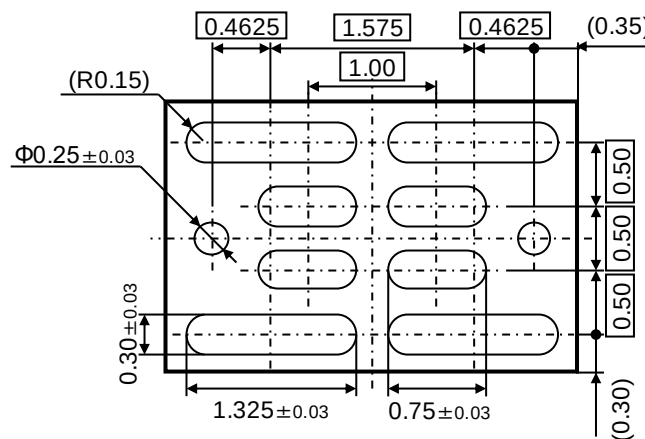
Unit: mm



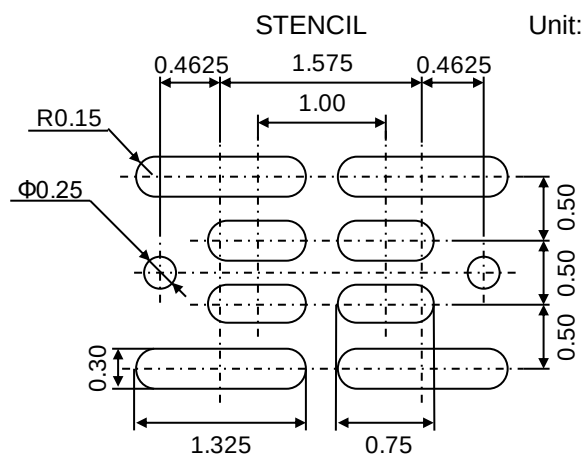
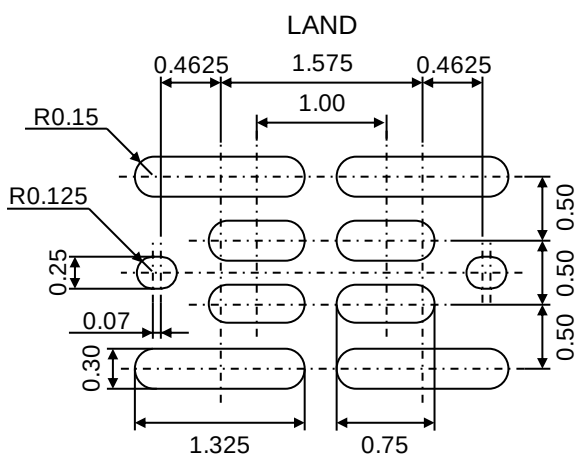
(Front View)



(Bottom View)



11. LAND & STENCIL PATTERN (Reference)



Unit: mm

Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2022.5.16	1.00	1. Initially issued.
2022.9.15	2.00	1. Revised ESD class.
2022.12.23	3.00	1. Revised ESD class.
		2. Revised the value of Rg.
		3. Revised the value of Ciss, Coss, Crss to TBD.
		4. Revised the value of td(on), tr, td(off), tf to TBD.
		5. Added important notice in Land Pattern.
2023.3.6	4.00	1. Updated the value of Ciss, Coss, Crss
		2. Updated the value of td(on), tr, td(off)

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