NUC980 Series Hardware Design Guide

Application Note for 32-bit NuMicro™ Family

Document Information

Abstract	This document introduces how to use the NUC980 series and describes the minimum hardware resources required to develop a basic system.
Apply to	NUC980 Series

For additional information or questions, please contact: Nuvoton Technology Corporation.

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Table of Contents

1 Power Supplies

This section describes design considerations related to the NUC980 series power supply scheme and power operating modes.

1.1 Power Supply Scheme

The NUC980 series should be supplied by a stabilized power; VDD33, VDD12, MVDD, AVDD, RTCVDD, USB0_VDD, USB1_VDD, USBPLL0, USBPLL1 and PLLVDD

Some points need to take care when using these power rails:

- VIO_VDD pin must be powered by 3.3V±10% and with external decoupling capacitors. (place one 0.1uF capacitor for each VDD33 pin is recommended)
- VCORE_VDD pin must be powered by 1.2V±10% and with external decoupling capacitors. (place one 0.1uF with MLCC and one buck 10uF with Tantalum capacitor for each VDD12 pin is recommended)
- MVDD pin must be powered by 1.8V±0.1V and with external decoupling capacitors. (place one 0.1uF with MLCC and one buck 10uF with Tantalum capacitor for each MVDD pin is recommended)
- AVDD pin must be powered by 3.3V±10% and with external decoupling capacitors. (place one 0.1uF capacitor and a buck 10uF capacitor for each AVDD pin is recommended)
- RTCVDD is an independent power domain, it can be powered by 3.6V~2.0V and place with a 0.1uF decoupling capacitor.
- PLLVDD is a phase lock loop power pin which should be supplied by 1.2V±10% and with external decoupling capacitors. (place one 0.1uF capacitor and a buck 10uF capacitor is recommended)
- USB0VDD is USB port 0 PHY power pin which should be supplied by 3.3V±10% and with external decoupling capacitors. (place one 0.1uF capacitor and one buck 10uF capacitor is recommended)
- USB0PLLVDD is USB port 0 core power pin which should be supplied by 1.2V±10% and with external decoupling capacitor. (place one 0.1uF capacitor and one buck 10uF capacitor is recommended)
- USB1VDD is USB port 1 PHY power pin which should be supplied by 3.3V±10% and with external decoupling capacitors. (place one 0.1uF capacitor and one buck 10uF capacitor is recommended)
- USB1PLLVDD is USB port 1 core power pin which should be supplied by 1.2V±10% and with external decoupling capacitor. (place one 0.1uF capacitor and one buck 10uF capacitor is recommended)

1.1.1 NUC980 Power Scheme

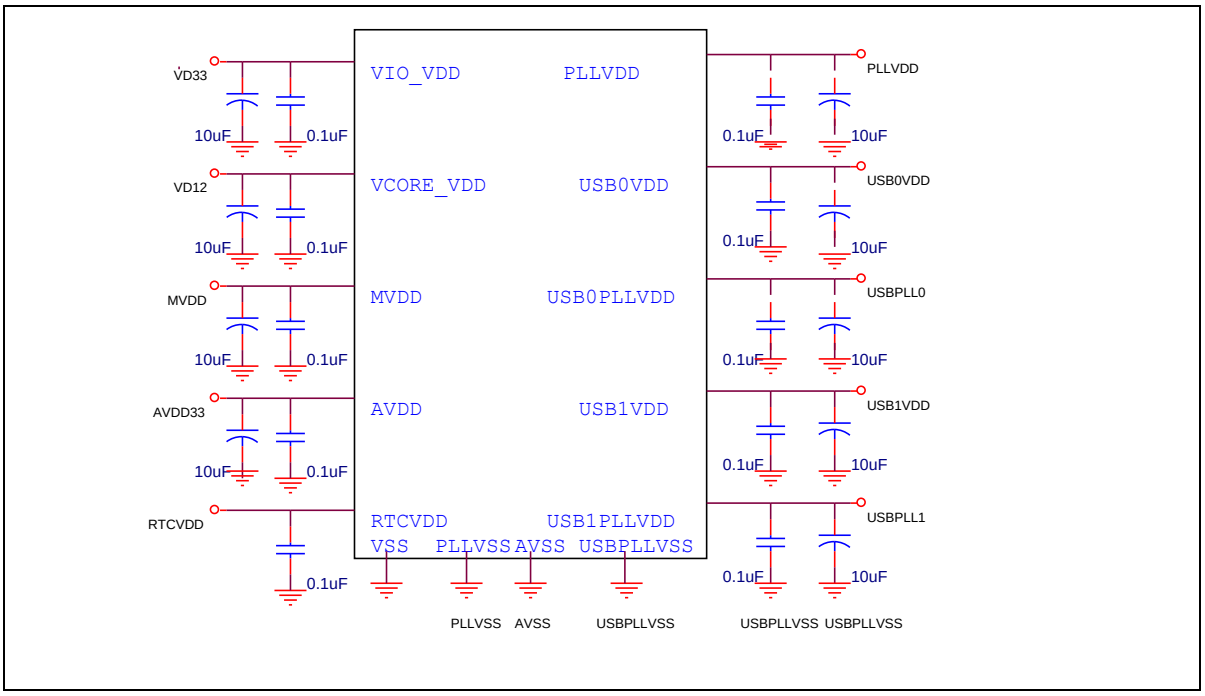

Figure 1-1 Power Supply Scheme

1.2 Power Operating Modes

The NUC980 provides power management scenarios, including Power-down, Idle and Normal Operating modes, to manage the power consumption. The peripheral clocks can be Enabled/Disabled individually by controlling the corresponding bit in CLKSEL control register. User can turn-off the unused modules' clock for power saving.

- Normal mode: In this mode, CPU run normally and clocks of all functionalities are on. The clock frequency of CPU, DRAM, AHB peripherals and APB peripherals are 300 MHz, 150 MHz, 150 MHz and 75 MHz, respectively.

- Idle mode: When CPU is not busy, user can put ARM926EJ-S™ processor into a low-power state by the wait for interrupt instruction. In this mode, the clocks of all functionalities are on. The clock frequency of DRAM, AHB peripherals and APB peripherals are 150 MHz, 150 MHz and 75 MHz.

- Power-down mode: In this mode, all clocks (clocks for all functionalities, CPU and the HXT (12 MHz) stop, except LXT (32.768 kHz), with SRAM retention.
  The mechanisms shown below could wake chip up from Power-down mode:

  1. EINT0, EINT1, EINT2 or EINT3 (External Interrupt) pin toggled.
  2. GPIO pin toggled.
  3. Timer 0/1/2/3/4/5 timeout or capture interrupt is active.
  4. WDT time-out interrupt is active.

5. RTC alarm or relative alarm interrupt is active.
6. UART 0/1/2/3/4/5/6/7/8/9
    - UARTx_nCTS pin toggleed (x is 0, 1, 2, 3, 4, 5, 6, 7, 8 or 9).
    - UARTx_RXD pin goes low level (x is 0, 1, 2, 3, 4, 5, 6, 7, 8 or 9).
    - Received data FIFO reached threshold.
    - Received data FIFO threshold time-out.
    - RS-485 address match (AAD Mode).
7. I^2C slave mode address match.
8. EMAC 0/1 received a Magic Packet.
9. HSUSBD detected a VBUS change event or USB bus RESET/RESUME event.
10. USB 1.1 Full Speed host controller detected a connect/dis-connect/remote-wakeup event.
11. CANx_RXD pin goes low level (x is 0, 1, 2 or 3).
12. SDH detected card pulg/un-plug event or SDIO card interrupt.

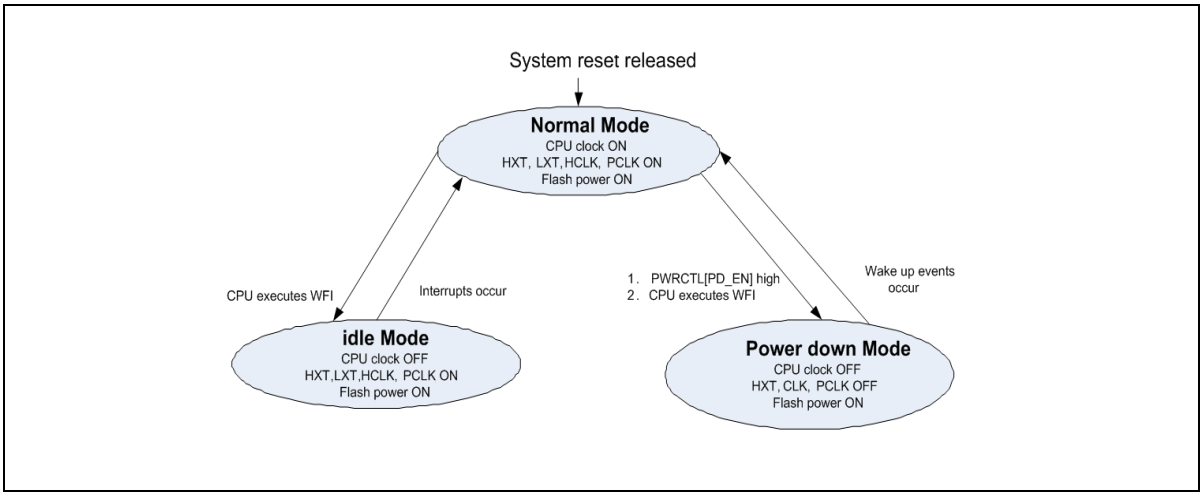

Figure 1-2 Power Operating Modes

1.3 DC Electrical Characteristics

Table 1-3 DC electrical characteristics

Parameter	Sym.	Specification				Test Conditions
		MIN.	TYP.	Max.	Unit	
Core Operation voltage	V_{DD12}	1.14	1.2	1.32	V	
I/O Operation Voltage	V_{DD33}	2.97	3.3	3.63	V	
Memory I/O Operation Voltage for DDR or DDR2	$MV_{DD\ (1)}$	1.70	1.8	1.90	V	
Memory I/O Operation Voltage for SDR Type SDRAM	$MV_{DD\ (2)}$	2.97	3.3	3.63	V	
Battery Operation Voltage	V_{BAT33}	2.0	3.3	3.63	V	
USB Operation Voltage (1)	V_{USB0_VDD12} V_{USB1_VDD12}	1.14	1.2	1.32	V	
USB Operation Voltage (2)	V_{USB0_VDD33} V_{USB1_VDD33}	2.97	3.3	3.63	V	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD33}	2.97	3.3	3.63	V	
Analog Reference Voltage	AVref	0		AV_{DD33}	V	
Current Consumption of Normal Operating Mode 1	I_{VDD12}		150		mA	V_{DD12} = 1.2V MV_{DD} = 1.8V V_{DD33} = 3.3V TA = 25°C, F_{OSC} = 12 MHz Frequency of CPUCLK/DDR_CLK is 300/150 MHz. All IPs on, all GPIO are input with pull-up.
	I_{MVDD_1}		50		mA	
	$I_{USB0\_VDD12\_1}$		7.5		mA	
	$I_{USB1\_VDD12\_1}$		7.5		mA	
	$I_{USB0\_VDD33\_1}$		35		mA	
	$I_{USB1\_VDD33\_1}$		35		mA	
	I_{VBAT33_1}		100		uA	
Current Consumption of Power Down Mode	I_{STDBY_VDD12}		3		mA	V_{DD12} = 1.2V
	I_{STDBY_MVDD}		6		mA	MV_{DD} = 1.8V
	I_{STDBY_VDD33}		5		µA	V_{DD33} = 3.3V
	$I_{STDBY\_USB0\_VDD33}$		0		µA	V_{USB0_VDD33} = 3.3V
	$I_{STDBY\_USB1\_VDD33}$		0		µA	V_{USB1_VDD33} = 3.3V
	$I_{STDBY\_USB0\_VDD12}$		2.5		µA	V_{USB0_VDD12} = 1.2V
	$I_{STDBY\_USB1\_VDD12}$		2.5		µA	V_{USB1_VDD12} = 1.2V
	I_{STDBY_AVDD33}		25		µA	AV_{DD33} = 3.3V
	I_{STDBY_VBAT33}		100		µA	V_{BAT33} = 3.3V

Parameter	Sym.	Specification				Test Conditions
		MIN.	TYP.	Max.	Unit	
System Power Off & RTC V_{BAT33} Power only	I_{VBAT33}		10		uA	

1.4 RTCVDD

NUC980 series is built-in a Real Time Clock (RTC) which is operated by the independent power supply while the system power is off. The RTC uses a 32.768 KHz external crystal.

This section will describe that design considerations related to the RTCVDD.

1.4.1 RTC Power Backup & Power Saving

For some applications requiring operation with either an external power supply or a battery backup, it is recommend to implement with a simple diode OR circuitry as the below figure shown. The diode D1 prevents current from flowing into the CR2032 (3V) battery from LDO when the external power is supplied.

Low forward voltage Schottky diodes are used to minimize the voltage dropout from the diode and ensure that the LDO output will be a little higher than CR2032 (3V). This solution can save CR2302 BAT power life time and provided proper powered to RTCVDD.

When external power is removed and the voltage is dropping lower than VBAT, the CR2032 (3V) battery will start supplying power to NUC980.

To avoid RTCVDD power dropping causes RTC data loss by different power supply switching through diodes, at least place a 100nF capacitance to VBAT with C1.

The following shows the RTC backup power block diagram for design reference.

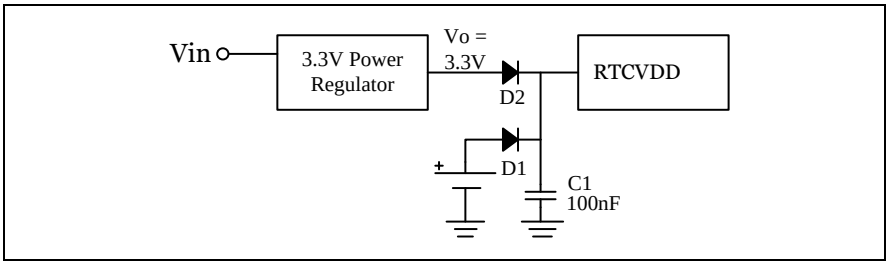

Figure 1.4 RTC Power Backup Block

2 RESET

Hardware Reset conditions can be issued by one of the below listed events. For these reset event flags can be read by RSTSTS register.

- Power-on Reset (POR).
- Low level on the nRESET Pin (nRST).
- Watch-dog time-out reset (WDT).
- Low voltage reset (LVR).

2.1 POR

NUC980 provides POR12 for Core power and POR33 for I/O power to guarantee low level logic output state during the first power up phase.

The Power on Reset (POR) function without external resistor or capacitor could reset the logic elements to their known state if power on slew rate was ≧ 1V/1us. The reset signal may not be available if the power rising rate was too fast.

For detail behaviors and electrical characteristics, it could be refer to the following waveforms and tables.

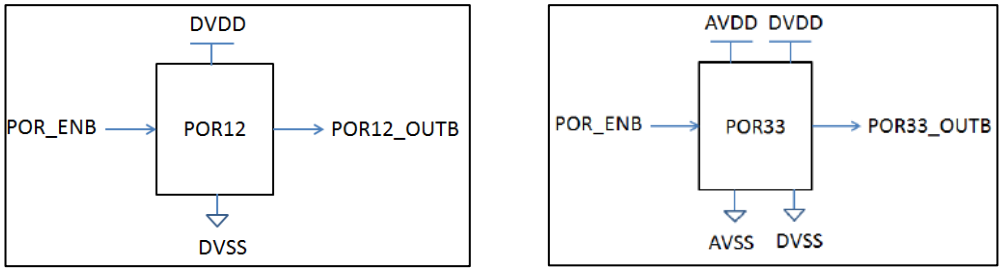

Figure 2.1-1 POR12/ POR33 Block

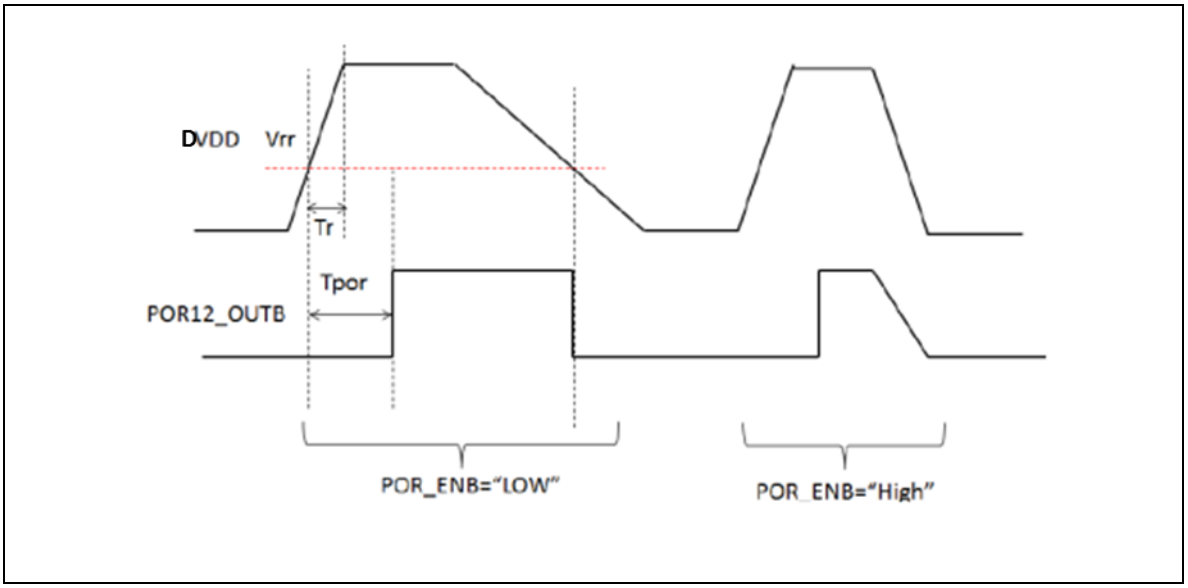

Figure 2.1-2 Power-On Reset at POR12

Table 2.1-1 POR12 Electrical Characteristics

SYMBOL	Description	Min.	Typ.	Max.	Unit	Condition
DVDD	Power Supply		1.2		V	
T_r	Power rising rate	1V/1us				
V_{rr}	Active level	0.63	0.76	0.86	V	● Power slew rate is 1.2V/20mS@25℃ ● POR_ENB=0
T_{POR}	POR output low duration		4.25		uS	● Power DVDD(rise) at Vrr to POR(rise) at 1/2 DVDD (DVDD slew rate=1V/1uS) ● AVDD up to 3.3V@25℃

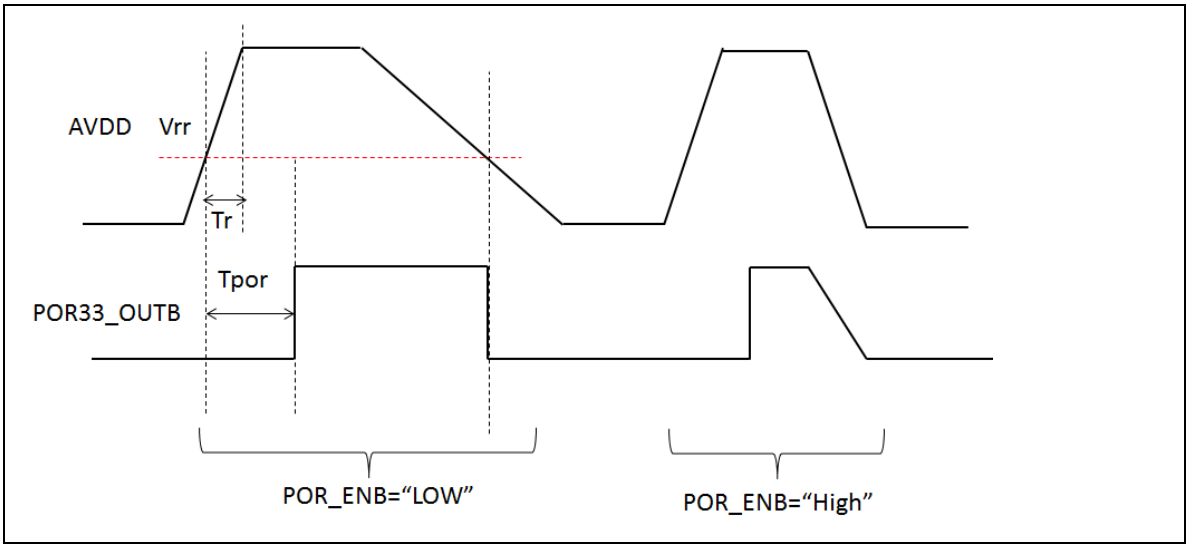

Figure 2.1-3 Power-On Reset at POR33

Table 2.1-2 POR33 Electrical Characteristics

SYMBOL	Description	Min.	Typ.	Max.	Unit	Condition
DVDD	Power Supply		3.3		V	
T_r	Power rising rate	1V/1us				
V_{rr}	Active level	1.65	1.83	2.0	V	● Power slew rate is 3.3V/20mS@25℃ ● POR_ENB=0
T_{POR}	POR output low duration		5.2		uS	● Power AVDD(rise) at Vrr to POR(rise) at 1/2 AVDD (AVDD slew rate=1V/1uS) ● AVDD up to 3.3V@25 ℃

2.2 nRST

Except for typical R & C elements tied to nRST pin is necessary that we also suggest to adding an auxiliary circuit as the following figure to ensure that system robustness.

Note. About related components parameters use please refer to the below circuitry shows on.

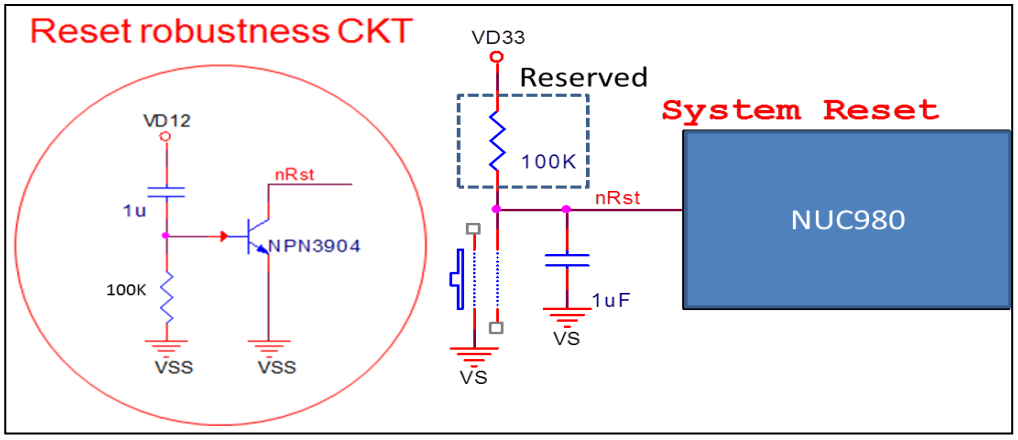

Figure 2.2-1 nRST External CKT

Table 2.2-1 nRESET Characteristics

Symbol	Parameter	Min.	Typ.	Max.	unit	**Test Conditions**
V_{ILR}	Negative going threshold (Schmitt input), nRESET	-	-	0.3*V_{DD}	V	V_{DD33} = 3.3V
V_{IHR}	Positive going threshold (Schmitt Input), nRESET	0.7*V_{DD}	-	-	V	V_{DD33} = 3.3V
R_{RST}	Internal nRESET pin pull up resistor	-	-	84	KΩ	1. V_{DD33}=3.63V, apply /RESET pin Vin= 3.63V and measure the input current 2. Reverse the current to Resistor value, R=V/I

2.3 WDT

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (24 ~ 220) and the time-out interval is 0.48828125ms ~ 32s if WDT_CLK = 32.768 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting WDTON (Power-on setting, SYS_PWRON [3]).
- Supports WDT time-out wake-up function only if WDT clock source is selected as LXT (32 KHz low-speed oscillator).

2.4 LVR

The Low Voltage Reset (LVR) and the Low Voltage Detector (LVD) both will generate logic high or logic low output for digital core once the monitored power, VDD, surpasses or falls below their detection level. The block diagram as Figure,

Table 2.4-1 Internal LVR/LVD Characteristics

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{ADD33}	Operation Voltage	2.97	3.3	3.63	V	-
T_A	Temperature	-40	-	85	°C	-
V_{TH_LVD}	LVD Threshold Voltage	2.295	2.55	2.805	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		2.475	2.75	3.025	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{TH_LVR}	LVR Threshold Voltage	2.115	2.35	2.585	V	-

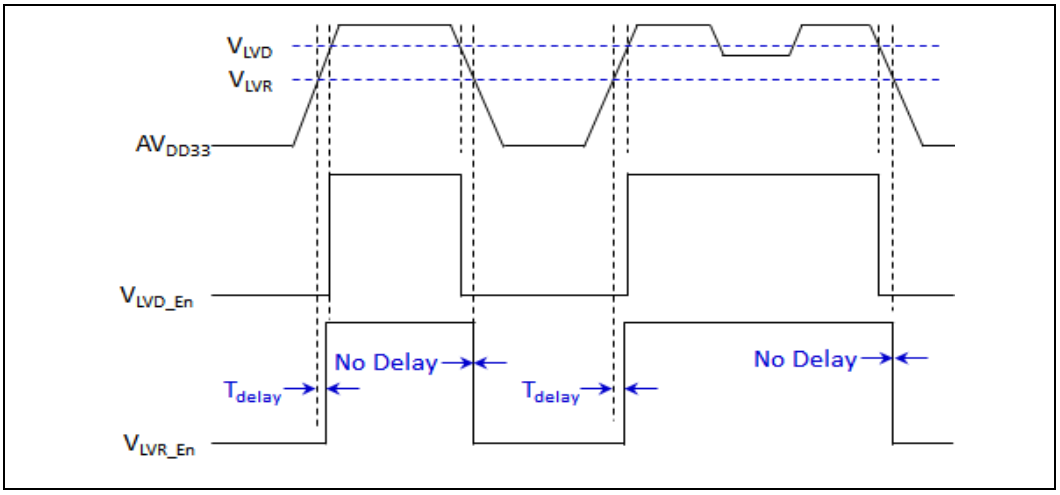

Figure 2.4-1 LVR and LVD Timing Waveform

Note:

1. When testing the features of LVD/LVR detect levels, the power-up or power-down speed of VDD should be slower than 100mS/2V.

3 Power sequence

3.1 Power-on Sequence

3.1.1 Condition-1

If $T_{IO} \geq T_{MVDD} \geq T_{CORE}$, the time of delay gap between < 0.5mS is prefer.

Note.

1. The time of delay gap is meaning that timing between T_{IO} with T_{core}.
2. When the time of delay gap < 0.5mS could prevent that transient phenomenon while power-on.

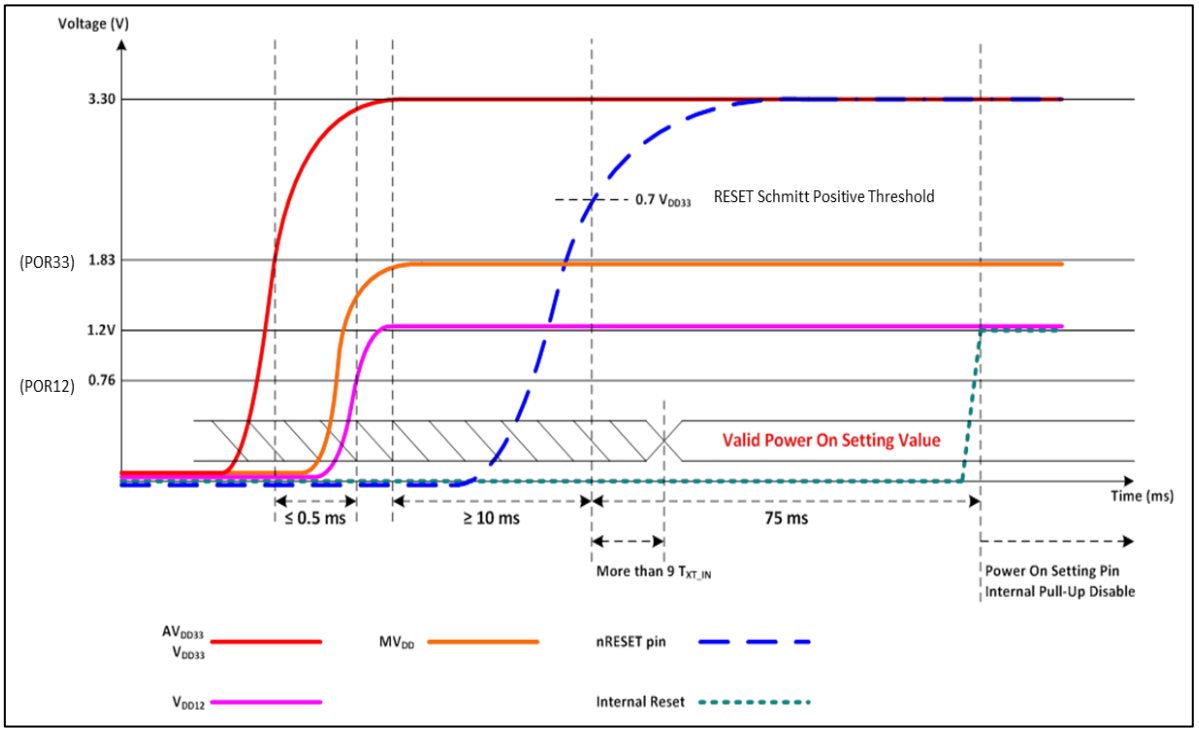

Figure 3.1-1 RESET vs. Power-on Sequence (I)

3.1.2 Condition-2

If $T_{CORE} \geq T_{MVDD} \geq T_{IO}$, it is acceptable as the below waveform, the time of delay gap between < 1mS is prefer.

Note.

1. The time of delay gap is meaning that timing between T_{core} with T_{IO}.
2. The time of delay gap < 1mS is prefer although NUC980 have that protection for latchup prevention.

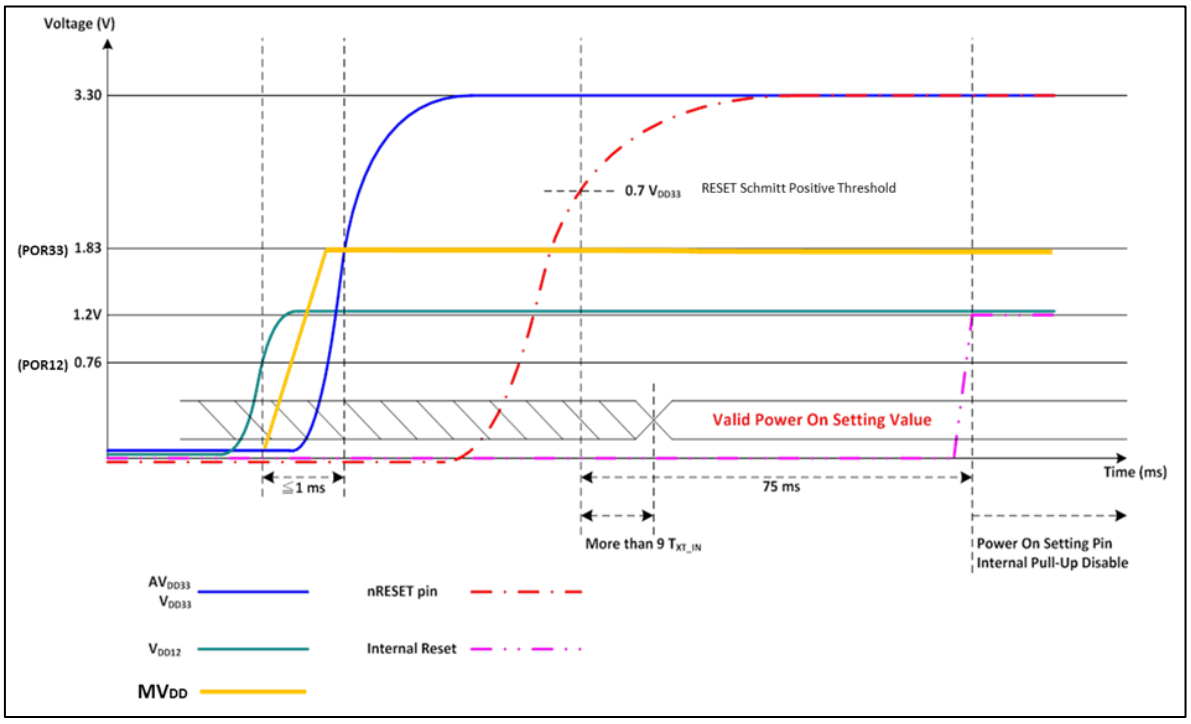

Figure 3.1-2 RESET vs. Power-on Sequence (II)

3.2 Power-down Sequence

The sequence doesn’t care.

Note.

1. T_{CORE} represents VDD12 powered time for Core power
2. T_{MVDD} represents MVDD powered time for MVDD power
3. T_{IO} represents VDD33 powered time for I/O power

4 Power on setting

The power-on setting is used to configure the chip to enter the specified state when the chip is powered up or reset.

Since each pin of power on setting has an internal pulled-up resistor when in reset period. If the application needs to set the configuration to “0”, the proper pull-down must be added resisters for corresponding configuration pins as the figure shown.

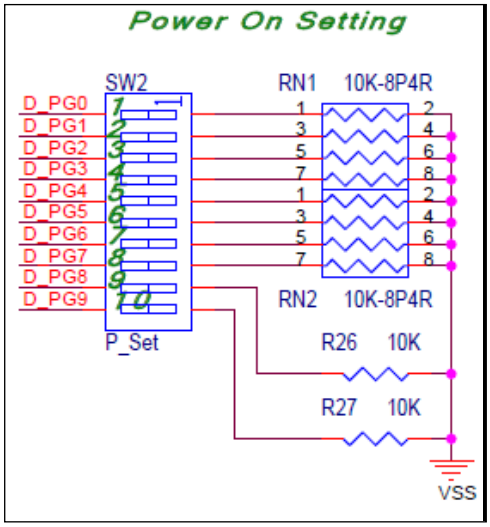

Figure 4.1-1 Power-on setting switch

Note:

1 = Open,

0 = Pulled down,

PG [9:0] = SYS_PWRON[9:0]

Table 4-1 System Power-On Setting, SYS_PWRON[1:0] for Booting Source Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PG[1:0]	Booting Sources Selection • 00 = Boot from USB • 01 = Boor from SD/eMMC • 10 = Boot from NAND Flash • 11 = Boot from SPI Flash (default)	SYS_PWRON[1:0]

Table 4-2 System Power-On Setting, SYS_PWRON[2] for SPI Booting Speed Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PG.2	QSPI0_CLK Frequency Selection • 0 = QSPI0_CLK = 30MHz • 1 = QSPI0_CLK = 50MHz (default)	SYS_PWRON[2]

Table 4-3 System Power-On Setting, SYS_PWRON[3] for WDT RESET Enable/Disable

Power-On Setting Pin	Description	Power-On Setting Register Bit
PG.3	Watchdog Timer (WDT) Enabled/Disabled Selection • 0 = WDT Disabled. • 1 = WDT Enabled.(default)	SYS_PWRON[3]

Table 4-4 System Power-On Setting, SYS_PWRON[5:4] for Debugging

Power-On Setting Pin	Description	Power-On Setting Register Bit
PG.4	JTAG Interface Selection • 0 = PA[6:2] used as JTAG interface. • 1 = PG[15:11] used as JTAG interface. (default)	SYS_PWRON[4]
PG.5	UART 0 Debug Message Output ON/OFF Selection • 0 = UART0 (PF[12:11]) debug message output ON. • 1 = UART0 (PF[12:11]) debug message output OFF. (default)	SYS_PWRON[5]

Table 4-5 System Power-On Setting, SYS_PWRON[9:6] for NAND Type Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PG[7:6]	NAND Flash Page Size selection • 00 = NAND Flash page size is 2KB. • 01 = NAND Flash page size is 4KB. • 10 = NAND Flash page size is 8KB. • 11 = Ignore Power-On Setting. (default)	SYS_PWRON[7:6]
PG[9:8]	Miscellaneous Configuration ➢ When Boot from NAND Flash, the PG[9:8] defines the ECC type as below • 00 = ECC is BCH T8 • 01 = ECC is BCH T12 • 10 = ECC is BCH T24 • 11 = Ignore power-on setting (default)	SYS_PWRON[9:8]

Table 4-6 System Power-On Setting for MISC. type selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PG[9:8]	Miscellaneous Configuration ➢ When Boot from SD/eMMC, the PG[9:8] defines the SD0/eMMC0 or SD1/eMMC1 used as the booting source. • 11 = SD0/eMMC0 (GPC group) used as the booting source. • Others = SD1/eMMC1 (GPF group) used as the booting source. ➢ When Boot from SPI Flash, the PG[9:8] defines the SPI flash type and data width. • 00 = SPI-NAND flash with 1-bit mode. • 01 = SPI-NAND flash with 4-bit mode. • 10 = SPI-NOR flash with 4-bit mode. • 11 = SPI-NOR flash with 1-bit mode. (default)	SYS_PWRON[9:8]

Table 4-7 System Power-On Setting for USB port0 Host/Device Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
USB0_ID	USB Port 0 Role Selection • 0 = USB Port 0 act as a USB host • 1 = USB Port 0 act as a USB device (default)	SYS_PWRON[16]

Note. USB0_ID pin has an internal pull-up with 50K Ω around.

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5 Clock

The clock controller generates all clocks for CPU, system bus, AHB masters and all APB IP functionalities. NUC980 includes two PLL modules. Each functionality clock source comes from the PLL or from the external crystal input directly.

For each clock there is a bit on the CLKEN register to control the clock ON or OFF individually, and the divider setting is in the CLK_DIVCTL register. The register can also be used to control the clock enable or disable for power control.

This section describes that design considerations with CLK oscillation installation.

5.1 External Crystal Sources

There are two external clock sources for the NUC980 series:

1. HXT, external 12 MHz high speed crystal input for PLL precise timing operation.
2. LXT, external 32.768 kHz low speed crystal input for RTC function and low speed clock source.

The oscillators of 12MHZ CLK and RTC_32K are connected with a quartz X'tal and two capacitors externally.

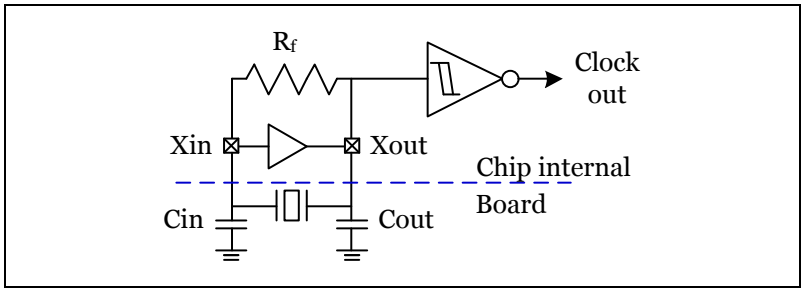


Figure 5.1-1 Crystal Oscillator Circuit

- Cin, Cout: External capacitors
- Rf: feedback resistor
- X'tal: External X'tal

The external crystal oscillator and two capacitors are connected to the pad "Xin" and pad "Xout". The capacitance value of the two capacitors may be adjustment by different crystal oscillator characteristic.

5.2 HXT, High Speed XTAL 12MHz

C1 and C2 should use high-quality ceramic capacitors, usually C1 with C2 have same value by symmetry. Here, C1/C2 using 15 pF is recommended for resonating with low ESR (≦50 Ω) 12MHz crystal and the crystal's CL is 12pF around.

Typically, PCB layout and NUC980 package capacitances should be calculation, the capacitance can estimate be 2pF around if PCB was 4-layers with FR4 material. Layout should make sure that crystal, C1/C2 and related components place together to close NUC980 XTAL_IN pin and XTAL_OUT pin ASAP to get that optimum performance and stability.

About C1/C2 value calculation for detail please refer the application note of "NUC980 XTAL CL design note".

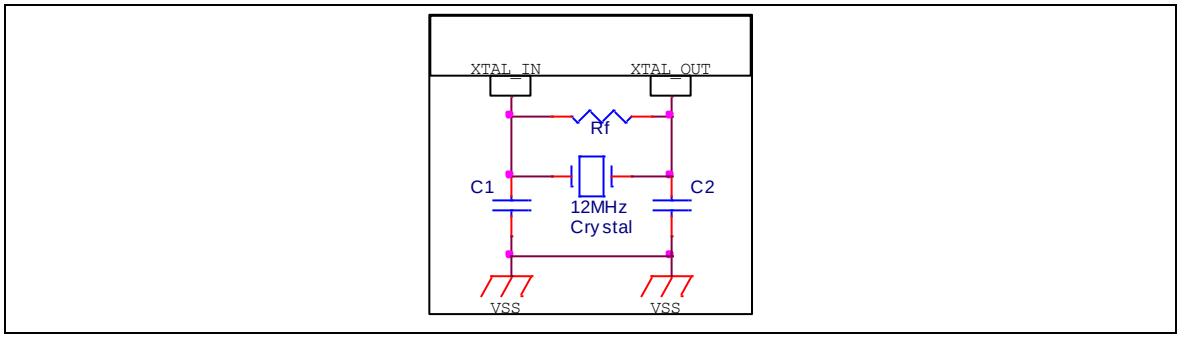


Figure 5.2-1 12MHz Crystal Oscillator Circuit

Table 5.2-1 12MHz C1/C2 reference value

Crystal	ESR (ohm)	C1, C2 (pF)	Condition
12 MHz	≦50	15	Assume that: 1. XTAL CL=12pF 2. PCB layout CL=2pF

5.3 LXT, Low Speed XTAL 32.768 KHz

About RTC 32.768KHz oscillation circuit that C1 and C2 are recommended to use high-quality ceramic capacitors. Usually C1 with C2 have same value by symmetry. Using 15 pF is recommended for resonating with 32.768KHz crystal.

For getting that accuracy 32.768KHz, typical engineer can operate the timer counter machine to calibrate C1/C2 value or alternative use software method that adjust NUC980 RTC frequency compensation register for approach.

For PCB layout that XTAL, C1/C2 and related components must place them together to close NUC980 X32_IN pin and X32_out pin ASAP to get that optimum accuracy and stability.

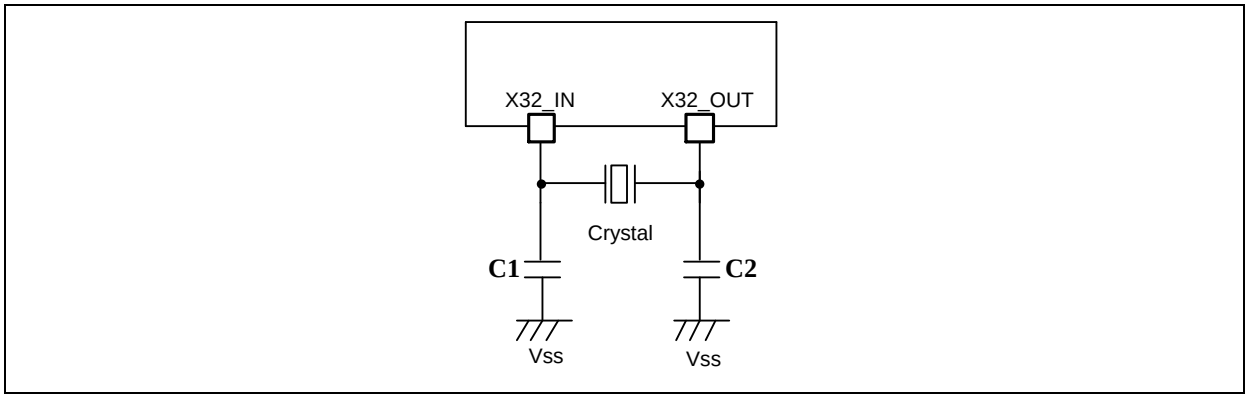


Figure 5.3-1 32.768KHz Crystal Oscillator Circuit

Table 5.3-1 32.768KHz C1 & C2 Recommend Value

Board Parameter	Symbol	Value
RTC_IN, RTC_OUT Capacitance	C1, C2	15pf

6 External Bus Interface (EBI)

The EBI supports 8-/16-bit data width have three chip selects that can connect three external devices with different timing setting requirements.

EBI supports dedicated external chip select pin with polarity control for each bank, also supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out.

EBI bus can supports LCD interface i80 mode with PDMA, supports variable external bus base clock (MCLK) which based on HCLK.

6.1 EBI Block Diagram

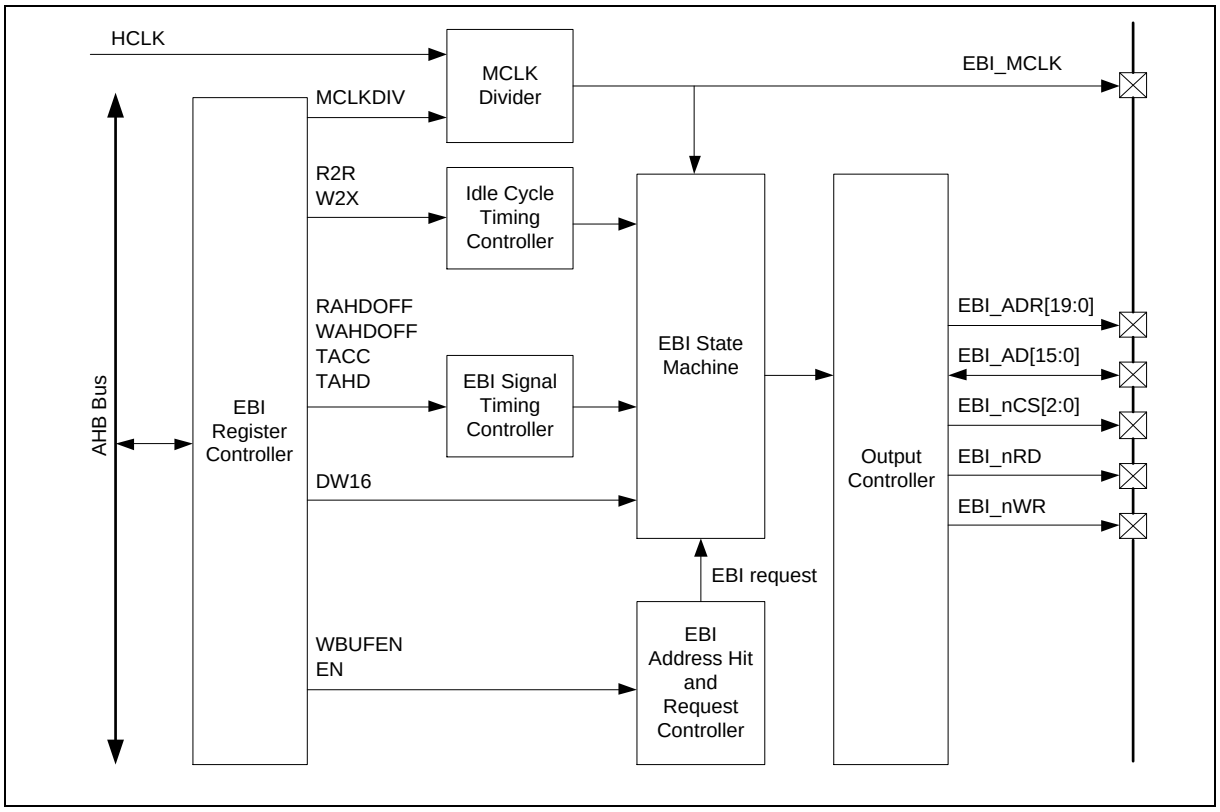


Figure 6.1-1 EBI Block Diagram

6.2 EBI Pin Configuration

Table 6-2 EBI pin-list

EBI	EBI_ADDR0	PG.0	MFP1	O	EBI address bus bit 0.
	EBI_ADDR1	PG.1	MFP1	O	EBI address bus bit 1.
	EBI_ADDR2	PG.2	MFP1	O	EBI address bus bit 2.
		PB.2	MFP1	O	
	EBI_ADDR3	PG.3	MFP1	O	EBI address bus bit 3.
	EBI_ADDR4	PG.6	MFP1	O	EBI address bus bit 4.
	EBI_ADDR5	PG.7	MFP1	O	EBI address bus bit 5.
	EBI_ADDR6	PG.8	MFP1	O	EBI address bus bit 6.
	EBI_ADDR7	PG.9	MFP1	O	EBI address bus bit 7.
	EBI_ADDR8	PA.12	MFP1	O	EBI address bus bit 8.
	EBI_ADDR9	PA.11	MFP1	O	EBI address bus bit 9.
	EBI_ADDR10	PA.10	MFP1	O	EBI address bus bit 10.
	EBI_ADDR11	PB.8	MFP1	O	EBI address bus bit 11.
	EBI_ADDR12	PG.5	MFP1	O	EBI address bus bit 12.
		PB.0	MFP1	O	
	EBI_ADDR13	PA.13	MFP1	O	EBI address bus bit 13.
		PB.6	MFP1	O	
	EBI_ADDR14	PA.14	MFP1	O	EBI address bus bit 14.
		PB.4	MFP1	O	
	EBI_ADDR15	PB.7	MFP1	O	EBI address bus bit 15.
	EBI_ADDR16	PB.5	MFP1	O	EBI address bus bit 16.
	EBI_ADDR17	PB.1	MFP1	O	EBI address bus bit 17.
	EBI_ADDR18	PG.4	MFP1	O	EBI address bus bit 18.
		PB.3	MFP1	O	
	EBI_ADDR19	PA.15	MFP1	O	EBI address bus bit 19.
	EBI_DATA0	PG.10	MFP1	I/O	EBI data bus bit 0.
		PC.0	MFP1	I/O	
		PB.13	MFP8	I/O	
	EBI_DATA1	PC.1	MFP1	I/O	EBI data bus bit 1.
		PD.12	MFP8	I/O	

	EBI_DATA2	PC.2	MFP1	I/O	EBI data bus bit 2.
		PD.13	MFP8	I/O	
	EBI_DATA3	PC.3	MFP1	I/O	EBI data bus bit 3.
		PD.14	MFP8	I/O	
	EBI_DATA4	PC.4	MFP1	I/O	EBI data bus bit 4.
		PD.15	MFP8	I/O	
	EBI_DATA5	PC.5	MFP1	I/O	EBI data bus bit 5.
		PF.0	MFP8	I/O	
	EBI_DATA6	PC.6	MFP1	I/O	EBI data bus bit 6.
		PF.1	MFP8	I/O	
	EBI_DATA7	PC.7	MFP1	I/O	EBI data bus bit 7.
		PF.2	MFP8	I/O	
	EBI_DATA8	PC.8	MFP1	I/O	EBI data bus bit 8.
		PF.3	MFP8	I/O	
	EBI_DATA9	PC.9	MFP1	I/O	EBI data bus bit 9.
		PF.4	MFP8	I/O	
	EBI_DATA10	PC.10	MFP1	I/O	EBI data bus bit 10.
		PF.5	MFP8	I/O	
	EBI_DATA11	PC.11	MFP1	I/O	EBI data bus bit 11.
		PF.6	MFP8	I/O	
	EBI_DATA12	PC.12	MFP1	I/O	EBI data bus bit 12.
		PF.7	MFP8	I/O	
	EBI_DATA13	PC.13	MFP1	I/O	EBI data bus bit 13.
		PF.8	MFP8	I/O	
	EBI_DATA14	PC.14	MFP1	I/O	EBI data bus bit 14.
		PF.9	MFP8	I/O	
	EBI_DATA15	PC.15	MFP1	I/O	EBI data bus bit 15.
		PF.10	MFP8	I/O	
	EBI_MCLK	PA.1	MFP2	O	EBI external clock output pin.
	EBI_nCS0	PA.9	MFP1	O	EBI chip select 0 output pin.
	EBI_nCS1	PA.6	MFP1	O	EBI chip select 1 output pin.
	EBI_nCS2	PA.1	MFP1	O	EBI chip select 2 output pin.
	EBI_nRE	PA.8	MFP1	O	EBI read enable output pin.

	EBI_nWE	PA.7	MFP1	O	EBI write enable output pin.

6.3 EBI Connectivity

Follow the pin configuration table to connect the EBI bus to connector (as the below example circuitry) for external devices connectivity, such as SRAM, LCD…etc.

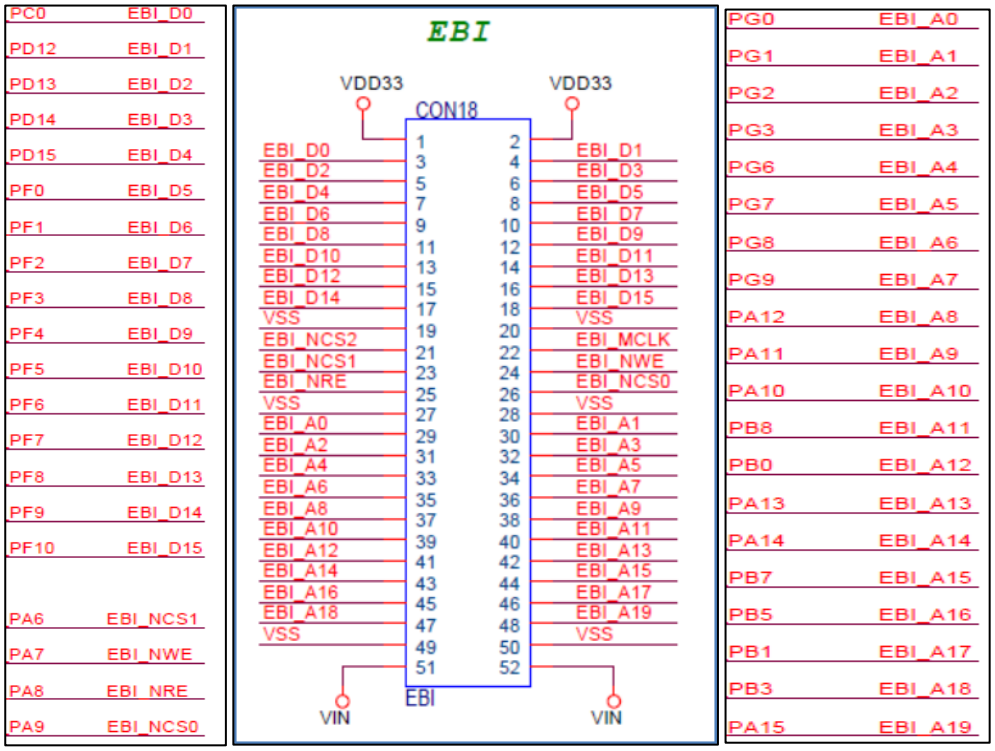


Figure 6.3.Example Circuitry for EBI devices connection

7 SAR_ADC

NUC980 series contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with 9 input channels. The ADC output coding is offset in binary, 1LSB=VREF/4096, the transfer characteristic is shown in Figure.

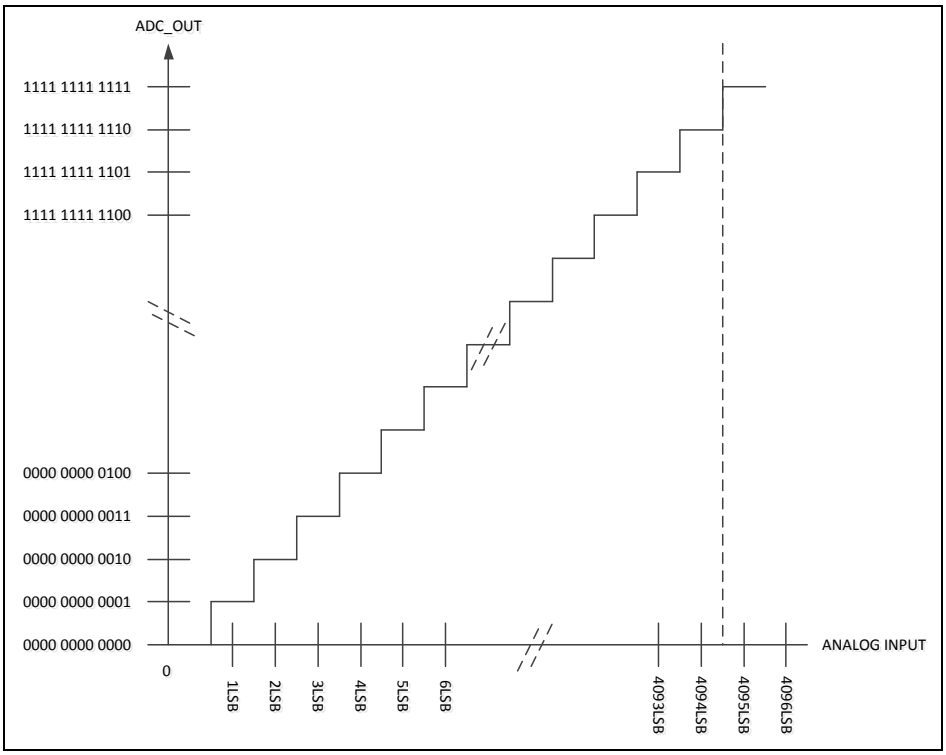


Figure 7.1-1 ADC Transfer Function

7.1 ADC Features

- Resolution: 12-bit resolution.
- DNL: +/-1.5 LSB, INL: +/-3 LSB.
- Data Rates: 200K SPS.
- Analog Input Range: VREF to AGND, could be rail-to-rail.
- Analog Supply: 2.7-3.6V.
- 8 Single-Ended analog inputs.
- Auto Power Down.

Table 7.1-1 SAR_ADC interfaces pin-list

Group	Pin Name	GPIO	MFP
ADC	ADC_CH0	PB.0	MFP8
	ADC_CH1	PB.1	MFP8
	ADC_CH2	PB.2	MFP8
	ADC_CH3	PB.3	MFP8
	ADC_CH4	PB.4	MFP8
	ADC_CH5	PB.5	MFP8
	ADC_CH6	PB.6	MFP8
	ADC_CH7	PB.7	MFP8
	AVREF	ADC_VREF	N/A

7.2 ADC Selection of Input Signals

IN_SEL[3:0]	Select ADC Analog Input Signal	Description
0000	ADC_CH0	ADC high speed input When HSPEED is set to high, it supports 600KS/S; When HSPEED is set to low, it supports 200KS/S. (suggestion)
0001	ADC_CH1	ADC high speed input When HSPEED is set to high, it supports 600KS/S; When HSPEED is set to low, it supports 200KS/S. (suggestion)
0010	ADC_CH2	ADC low speed input, only support 200KS/S
0011	ADC_CH3	ADC low speed input, only support 200KS/S
0100	ADC_CH4	ADC low speed input, only support 200KS/S
0101	ADC_CH5	ADC low speed input, only support 200KS/S
0110	ADC_CH6	ADC low speed input, only support 200KS/S
0111	ADC_CH7	ADC low speed input, only support

		200KS/S
1000	VREF	ADC low speed input, only support 200KS/S

7.3 Selection of Reference Voltage

REF_SEL[1:0]	ADC Analog Reference Pair Selection Signals
00	AVSS33 to 2.5V buffer output, or VREF input
11	AVSS33 to AVDD33
01 or 10	Reserved

Note.

Reference voltage is flexible, and could be selected according to the application.

For example, CH0 inputs a sine wave for rail to rail, REF_SEL should be set to 00 or 11.

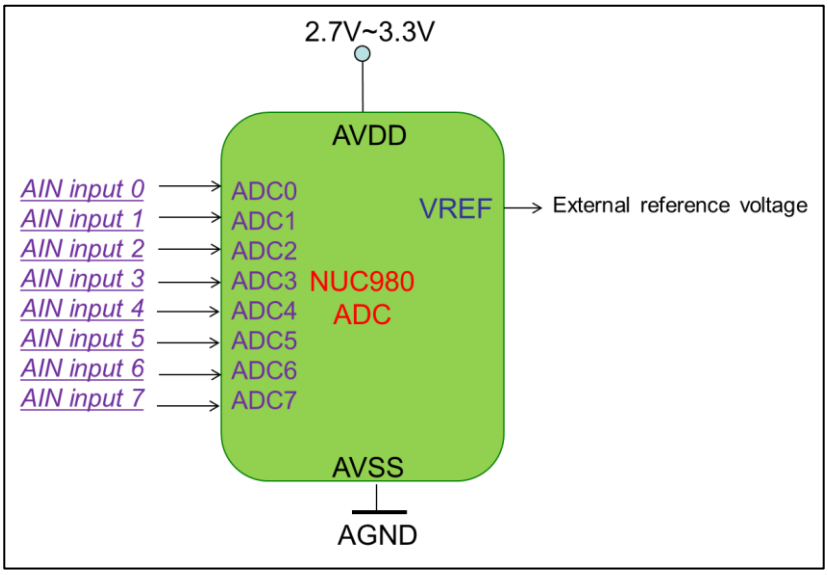
7.4 ADC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
-	Resolution	-	12	-	Bit	
DNL	Differential Nonlinearity Error	-	±1	-	LSB	V_{REF} is external AVREF pin
INL	Integral Nonlinearity Error	-	-1.2	-	LSB	V_{REF} is external AVREF pin
E_O	Offset Error	-	+3.7	-	LSB	V_{REF} is external AVREF pin
E_G	Gain Error (Transfer Gain)	-	-6.6	-	LSB	V_{REF} is external AVREF pin
E_A	Absolute Error	-	4.2	-	LSB	V_{REF} is external AVREF pin
-	Monotonic	Guaranteed				
F_{ADC}	ADC Clock Frequency	-	-	16	MHz	
F_S	Sample Rate	-	200K		SPS	
AV_{DD33}	Supply Voltage	2.7	3.3	3.6	V	
I_{DDA1}	Supply Current (Avg.)	-	1.2		mA	ADC channel 0/1 high speed mode
I_{DDA2}	Supply Current (Avg.)	-	1.0		mA	ADC channel 0/1 low speed mode
I_{DDA3}	Supply Current (Avg.)	-	0.4		mA	Other channels
AV_{REF}	Reference Voltage	2	-	AV_{DD33}	V	
V_{IN}	Analog Input Voltage	0	-	AV_{REF}	V	
R_{IN}	Analog Input Impedance	-	-	2	MΩ	
C_{IN}	Capacitance	-	25.6		pF	
2.5V BG	2.5V Band-gap voltage output accuracy		±6	±10	%	There isn't trimming for VREF output 100ppm/℃

7.5 Typical Connection and Application Note

As the figure shown that ADC detection supports external channel-0 to channel-7,

- For avoiding NUC980 be damage and big leakage occurred when ADC_AVDD didn't powered yet, that voltage detection source VIN input to ADC channel directly is illegal and inhibition.
- The ADC input channels have mega-Ω impedance level, for getting accuracy the divider R value should recommend to use hundred-kΩ level resistor (i.e. R1+R2 ＜ 1M Ω).



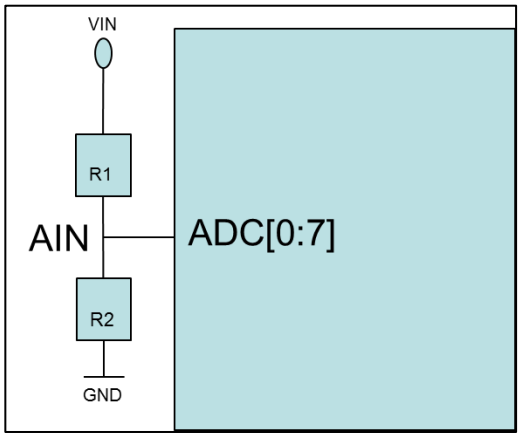


Figure 7.5-1 ADC AIN connection

8 USB

NUC980 integrated 6 USB 1.1 Full Speed Host Lite ports and two USB ports which the USB0 supports USB 2.0 High Speed Dual Role (Host/Device), the USB1 is dedicated support USB 2.0 High Speed Host Controller.

About USB Host Lite ports are compliant with USB Revision 2.0 Specification, compatible with OHCI (Open Host Controller Interface) Revision 1.0. It supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices, Built-in DMA supports Control, Bulk, Interrupt, Isochronous and Split transfers. Also supports an integrated Root Hub. Because USB Host Lite ports are used 8mA I/O driver buffer to instead of standard USB1.1 transceiver that transmission distance is limited to less than 1 meter.

Table 8-1 USB HOST lite portsx6 pin-list

USBHL0	USBHL0_DM	PB.6	MFP4	A	USB host lite port-0 differential signal D-.
		PB.7	MFP4	A	
		PB.9	MFP4	A	
		PD.14	MFP5	A	
	USBHL0_DP	PB.4	MFP4	A	USB host lite port-0 differential signal D+.
		PB.5	MFP4	A	
		PB.10	MFP4	A	
		PD.15	MFP5	A	
USBHL1	USBHL1_DM	PF.0	MFP6	A	USB host lite port-1 differential signal D-.
		PE.0	MFP6	A	
	USBHL1_DP	PF.1	MFP6	A	USB host lite port-1 differential signal D+.
		PE.1	MFP6	A	
USBHL2	USBHL2_DM	PF.2	MFP6	A	USB host lite port-2 differential signal D-.
		PE.2	MFP6	A	
	USBHL2_DP	PF.3	MFP6	A	USB host lite port-2 differential signal D+.
		PE.3	MFP6	A	
USBHL3	USBHL3_DM	PF.4	MFP6	A	USB host lite port-3 differential signal D-.
		PE.4	MFP6	A	
	USBHL3_DP	PF.5	MFP6	A	USB host lite port-3 differential signal D+.
		PE.5	MFP6	A	
USBHL4	USBHL4_DM	PA.15	MFP4	A	USB host lite port-4 differential signal D-.
		PF.6	MFP6	A	
		PE.6	MFP6	A	
	USBHL4_DP	PG.10	MFP4	A	USB host lite port-4 differential signal D+.
		PB.13	MFP6	A	
		PF.7	MFP6	A	

		PE.7	MFP6	A	
USBHL5	USBHL5_DM	PA.13	MFP4	A	USB host lite port-5 differential signal D-.
		PB.11	MFP4	A	
		PF.8	MFP6	A	
		PE.8	MFP6	A	
	USBHL5_DP	PA.14	MFP4	A	USB host lite port-5 differential signal D+.
		PB.12	MFP4	A	
		PF.9	MFP6	A	
		PE.9	MFP6	A	

The following guidelines will provide PCB design considerations for system designer reference.

8.1 USB Termination

For getting a good USB signals quality and USB Eye-Diagram to meet USB compliant test electrical characteristic that USB bus must be request that 90-Ω impedance for PCB layout.

Normally, the USB terminator resistors and terminator capacitors should be reserved and placed them to USB termination, i.e. USB connector side purposed for USB Eye-Diagram and USB signals quality matching impedance 90-Ω correction.

As the below figures shown that USB termination connection for system design reference

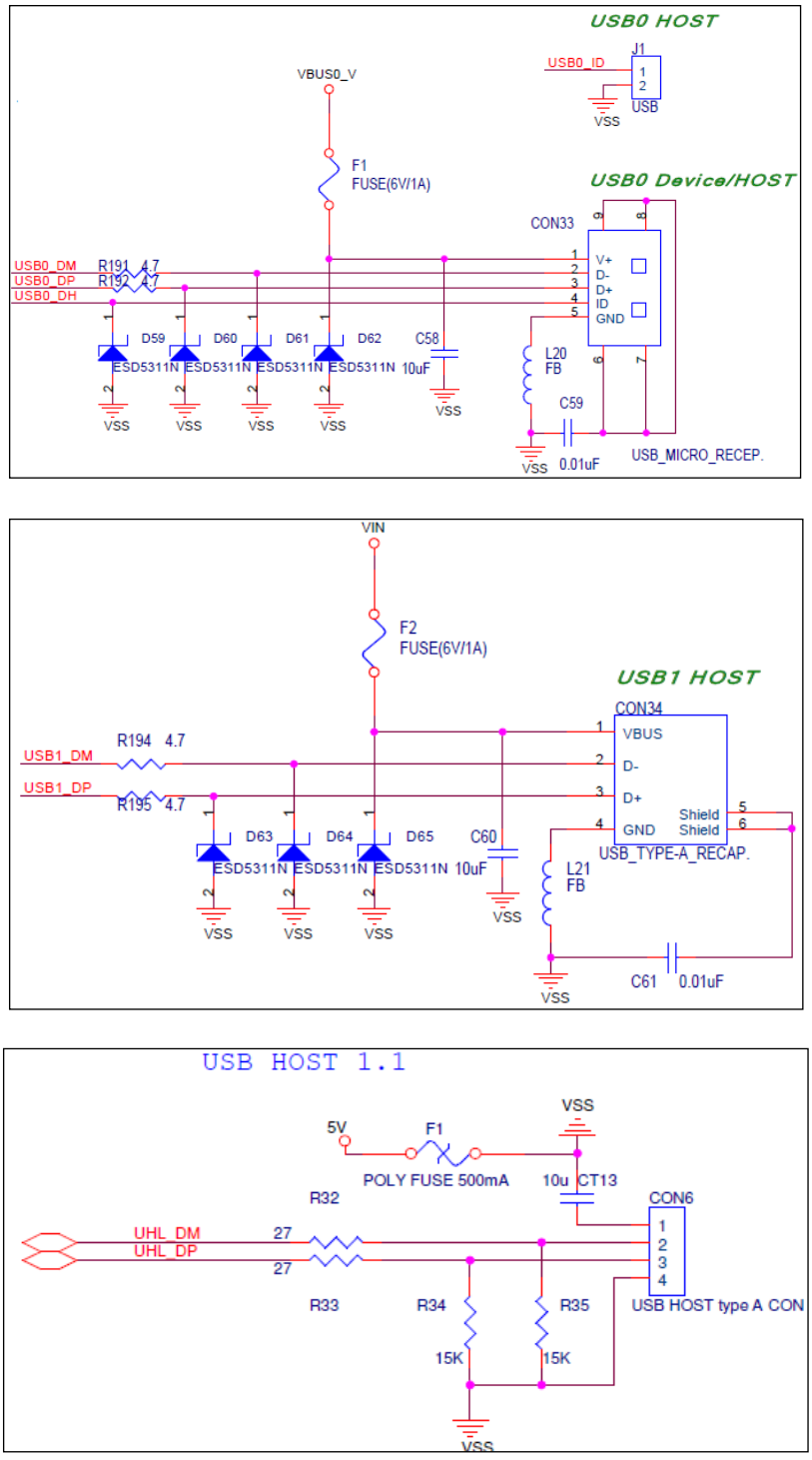


Figure 8.1 Example for USB termination connection

8.2 USB REXT and USB Power

The USB REXT signal needs an external resistor with precision 12.1K ohm for preventing any noise interference to the reference bias, the REXT which should be placed close to the pins of NUC980 USB_REXT and USB_VSS as figure shown.

Of course PCB design also needs to take care of USB power and ground as the figure shown the USBVDD33, USBVDD12 and USBVSS, they are isolated with ferrite bead and 0 ohm resistor for reducing possible power noise from system.

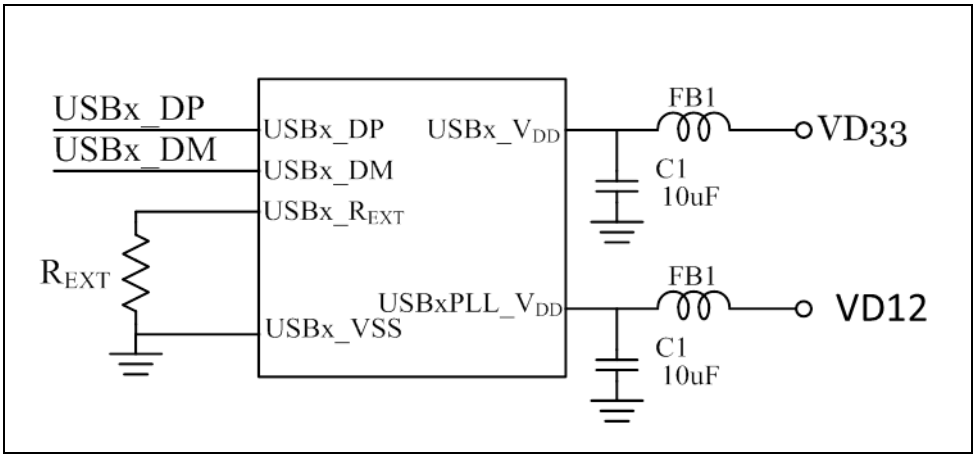


Figure 8.2 Example of USBVDD & REXT Connection

8.3 PCB Layout Considerations

Traces the DP/DM to the connector, the signal swing during high-speed operation on the DP/DM line is relatively a small waveform about 400mV. So, if there is any differential noise picked up will affect transceiver signal on the pair traces. When the DP/DM traces are not shield, the traces behave like an antenna to pick up noise by the surrounding components.

To lower the interference effect, use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems.

The high speed USB validation efforts focused on a four-layer PCB where the first layer is a signal layer, the second layer is power, the third layer is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth layer closest to the ground layer, and allowing a higher component density on the first layer.

8.3.1 Layout Guidelines

1. DP/DM traces should be length matched and as close as possible to the connector.
2. Route DP/DM traces should be close together for noise rejection on the differential signals, parallel to each other and the length difference within 200-mil.
3. If the common chock is necessary, it should be as close as to the connector.
4. No extra components at DP/DM pair traces to maintain signal integrity.
5. No de-coupled caps on the DP/DM.
6. The characteristic of matching impedance 90Ω on the DP/DM is necessary.
7. Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.

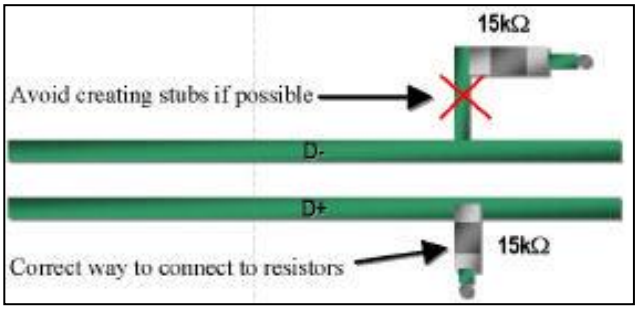


Figure 8.3.1-1 BUS Stubs should avoid

8. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. It is preferable to change layers to avoid crossing a plane split.
9. Use the following guidelines for the VCC OR GND plane.
    a. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to High Speed USB signals, high-speed clock and signal traces as well as slower signal traces, which might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is

common mode)

b. Avoid routing of USB signals within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

10. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
11. Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
12. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack up the height above the plane are 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

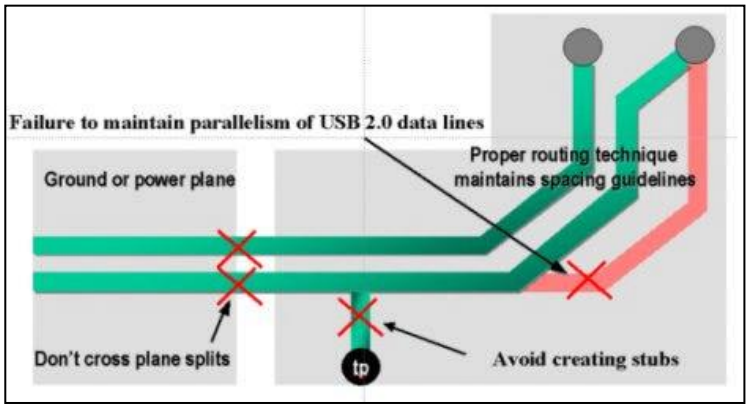


Figure 8.3.1-2 Maintain Parallelism USB BUS

8.3.2 Through Hole Consideration for D+ and D-

For the two-layer or multi-layer of PCB, when the signals of D+ and D- need to be through another layer, in which the resistively of through hole should be concerned. To lower the resistively issue for the sensitivity case, the two-via or multi-via should be adapted, as shown in the following figure.

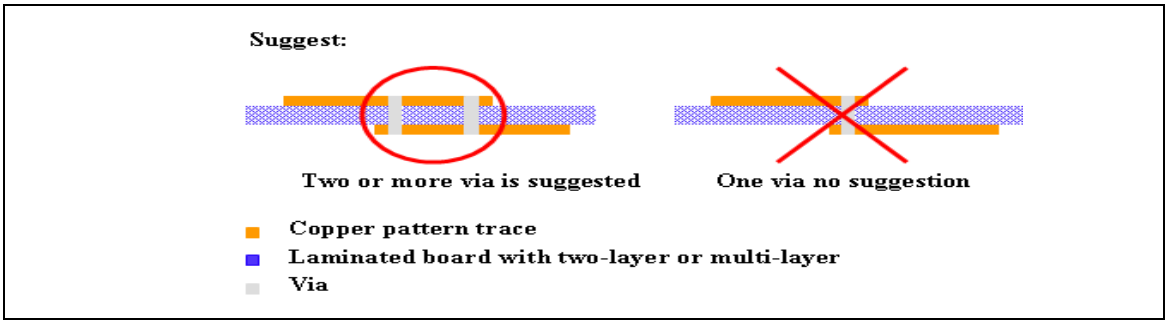


Figure 8.3.2 Through Hole for D+ and D-

8.3.3 USB Full Speed Signal Trace for D+ and D-

To avoid trace effect the USB bus trace length should be almost the same of D+ and D-. Then, the characteristic impedance should be a symmetrical path for the differential end of the USB port. The characteristic impedance should be 50 Ω for full speed USB1.1. For reducing the trace length, the USB terminal should be as close as the USB port of NUC980.

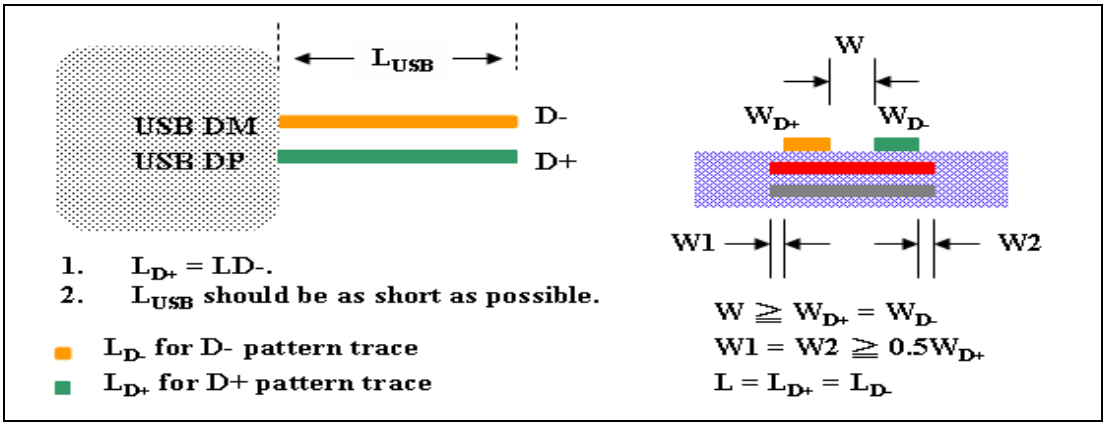


Figure 8.3.3 Signal Trace for D+ and D-

8.3.4 USB High Speed Trace Spacing

The following figure provides an illustration of the recommended trace spacing for multi-layer and 2-layer PCB.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90ohms differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviation is kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack up being used. For the board stack up parameters referred to in Layer Stacking, 7.5-mil traces with 7.5-mil spacing results in approximately 90 ohms differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
5. If PCB is 2-layer design, for signals quality request that USB signal pairs should have GND plane closely to traces side for shielding as the illustration of figure.

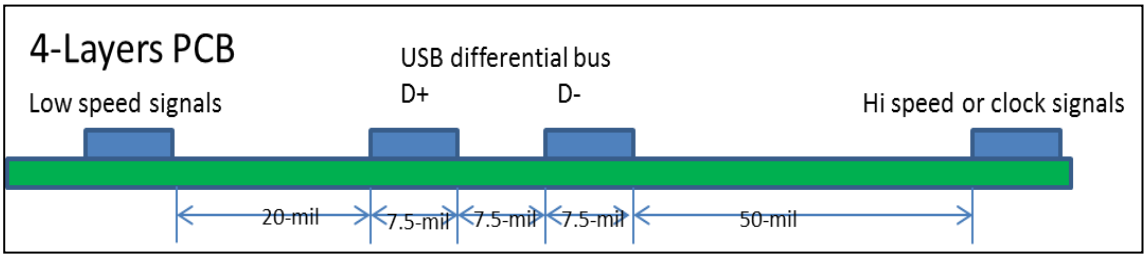


Figure 8.3.4-1 Multi-Layer PCB USB Bus Trace Space Recommendation

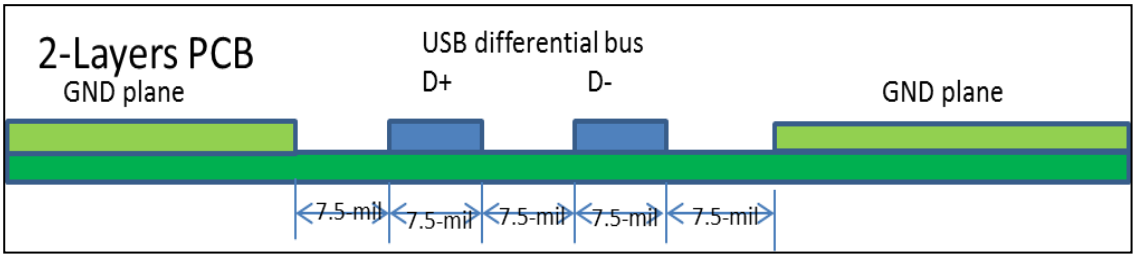


Figure 8.3.4-2 2-Layer PCB USB Bus Trace Space Recommendation

8.3.5 High Speed USB Trace Length

Main board's USB signal pairs total trace length should be less than or equal 18 inches.

8.3.6 PCB Stacking for USB

The following is an example of PCB layout stack-up for USB
4-Layer Stack-Up,

- Layer-1 Signal (top)
- Layer-2 VCC
- Layer-3 GND
- Layer-4 Signal (bottom)

In this case, high speed USB validation PCB used 7.5-mil traces with 7.5-mil spacing between differential pairs to obtain 90 Ohm differential impedance. The PCB specific board stack up used is as follows:

- 1 oz. copper
- Prepreg @4.5 mils
- Core @53 mils
- PCB thickness @ 63 mils (1.6mm)
- FR4 material

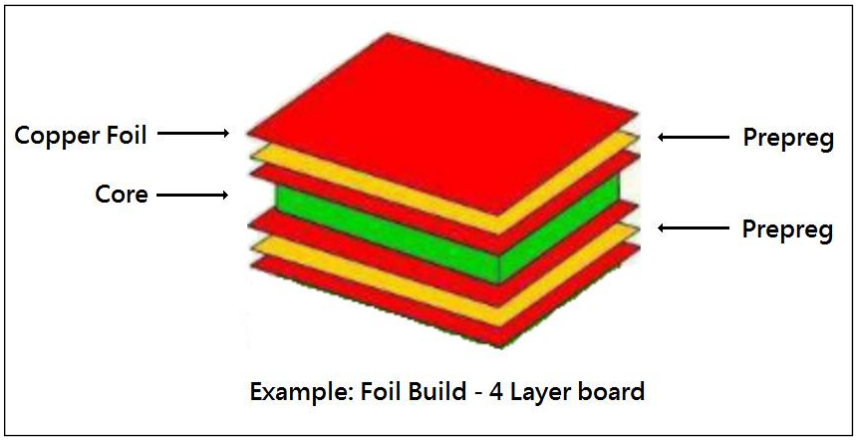


Figure 8.3.6 4-Layer PCB structures

8.3.7 USB EMI/ESD Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

8.3.8 EMI - Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design may include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Below figure shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

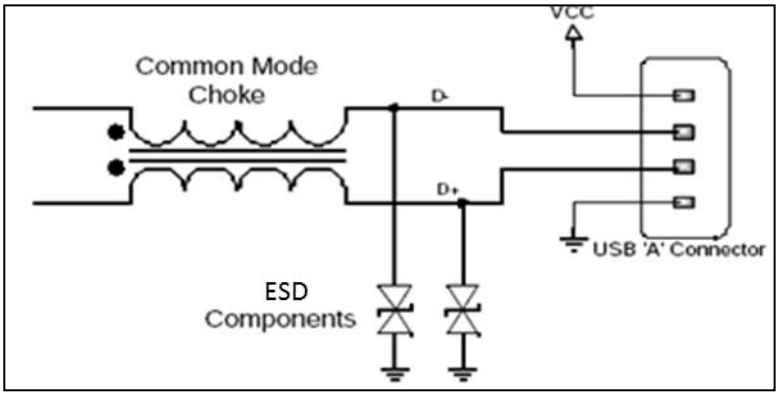


Figure 8.3.8-1 Common mode choke

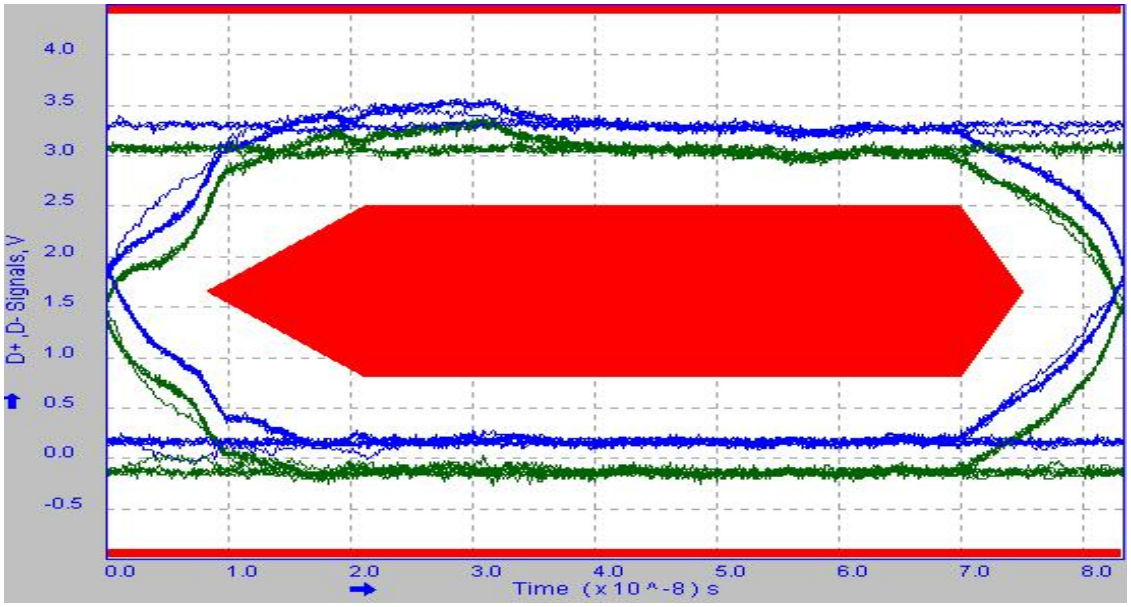


Figure 8.3.8-2 USB Full Speed

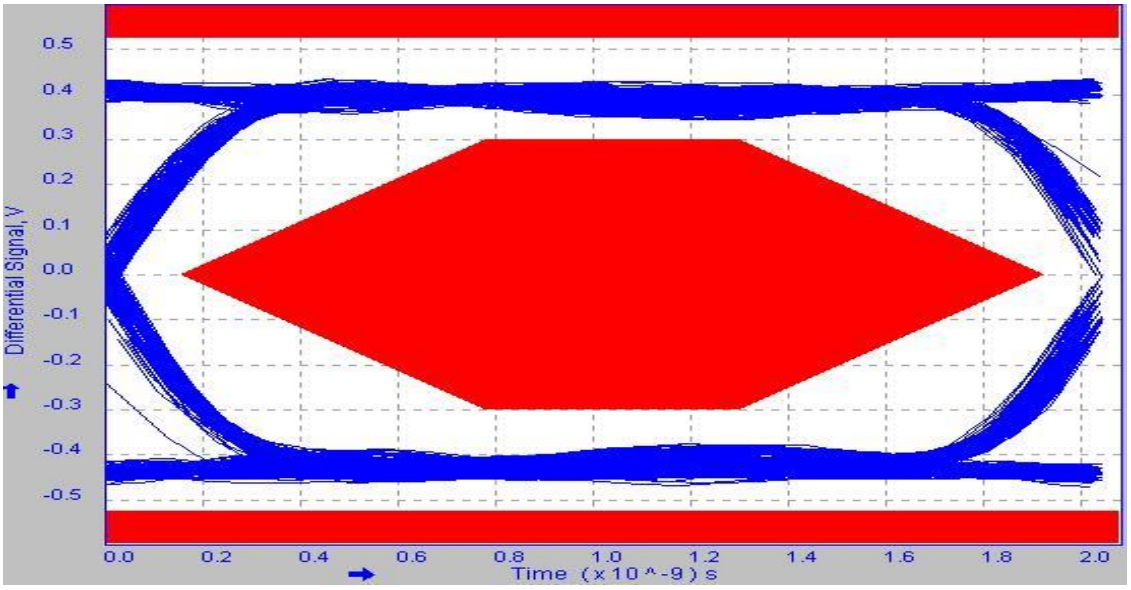


Figure 8.3.8-3 USB port0 High Speed Device

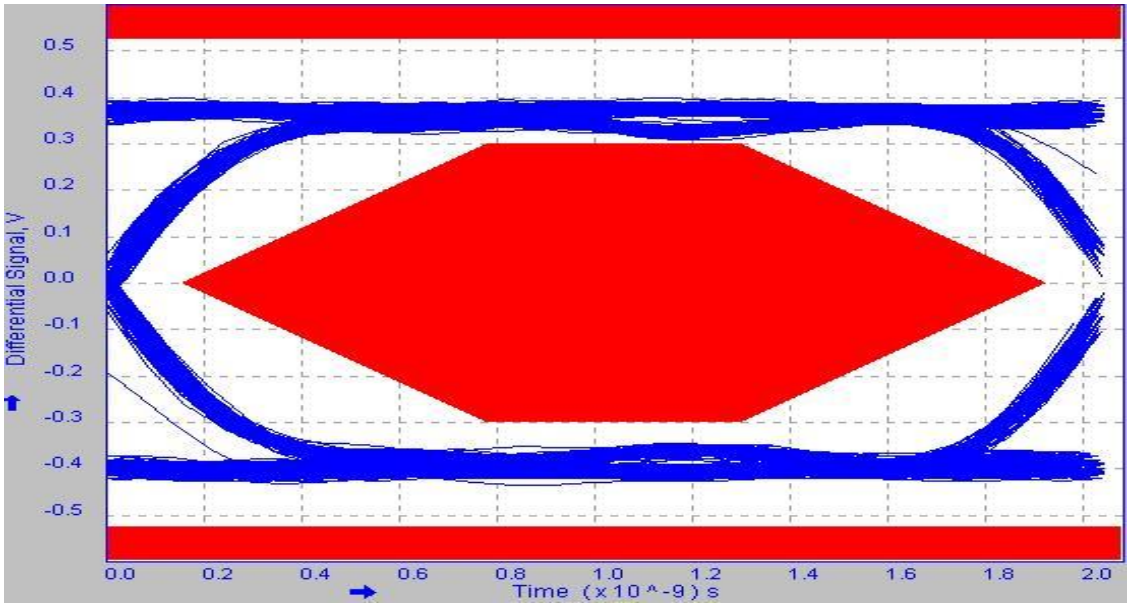


Figure 8.3.8-4 USB port0 High Speed HOST

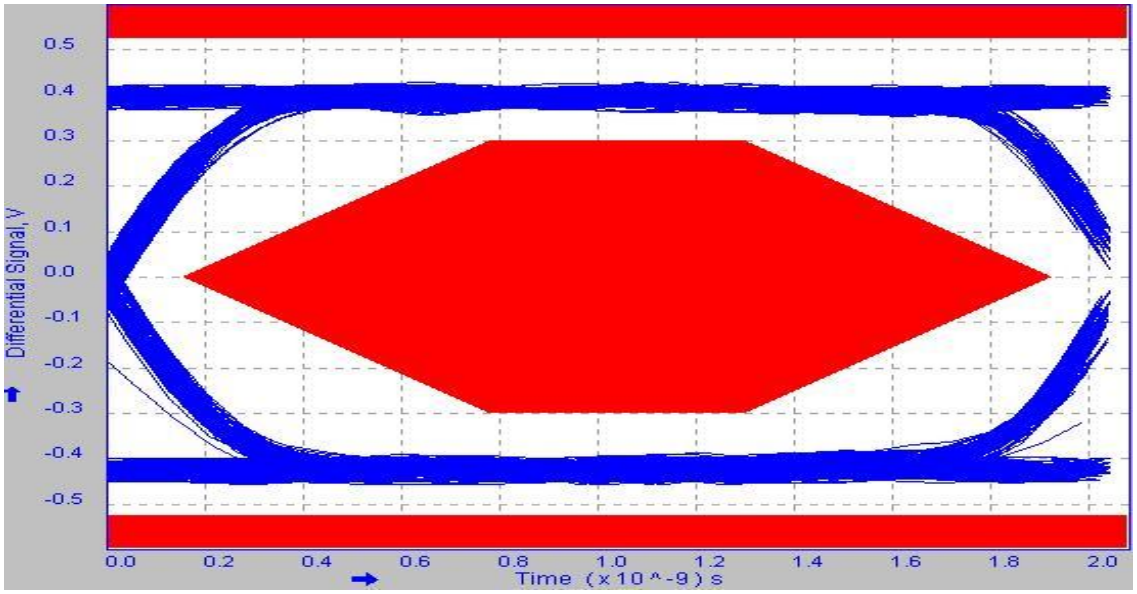


Figure 8.3.8-5 USB port1 High Speed HOST

The eye diagram above shows USB signal quality, as the common mode impedance increases, this distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality.

Finding a common mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces that the designer is trying to suppress.

2. Once the designer has a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so be careful about increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low speed, Full speed and High speed USB operation.

8.3.9 USB ESD solution

Low-speed and full-speed USB provide ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique doesn't work for high speed USB due to the much higher signal rate of HS data. Thus, for high speed USB solution designer should select proper low-capacitance ESD protection devices to resolve.

As with the common mode choke solution, we recommend including the footprints for this device, or some other proven solution, as a stuffing option in case it is needed to pass ESD testing.

ESD protection and common mode chokes are only needed if the design does not pass EMI or ESD testing. Footprints for common mode chokes and/or ESD suppression components should be included in the event that a problem occurs (General routing and placement guidelines should be followed).

9 Ethernet

NUC980 provides 2 Ethernet MAC Controller (EMAC) for Network application.
Supports both half and full duplex for 10 Mbps or 100 Mbps operation the EMAC supports RMII (Reduced MII) interface to connect with external Ethernet PHY.

Table 9-1 RMII 0/1 interfaces pin-list

RMII0	RMII0_CRSDV	PE.1	MFP1	I	RMII0 Carrier Sense/Receive Data input pin.
	RMII0_MDC	PE.9	MFP1	O	RMII0 PHY Management Clock output pin.
	RMII0_MDIO	PE.8	MFP1	I/O	RMII0 PHY Management Data pin.
	RMII0_REFCLK	PE.4	MFP1	I	RMII0 mode clock input pin.
	RMII0_RXD0	PE.3	MFP1	I	RMII0 Receive Data bus bit 0.
	RMII0_RXD1	PE.2	MFP1	I	RMII0 Receive Data bus bit 1.
	RMII0_RXERR	PE.0	MFP1	I	RMII0 Receive Data Error input pin.
	RMII0_TXD0	PE.7	MFP1	O	RMII0 Transmit Data bus bit 0.
	RMII0_TXD1	PE.6	MFP1	O	RMII0 Transmit Data bus bit 1.
	RMII0_TXEN	PE.5	MFP1	O	RMII0 Transmit Enable output pin.
RMII1	RMII1_CRSDV	PF.1	MFP1	I	RMII1 Carrier Sense/Receive Data input pin.
	RMII1_MDC	PF.9	MFP1	O	RMII1 PHY Management Clock output pin.
	RMII1_MDIO	PF.8	MFP1	I/O	RMII1 PHY Management Data pin.
	RMII1_REFCLK	PF.4	MFP1	I	RMII1 mode clock input pin.
	RMII1_RXD0	PF.3	MFP1	I	RMII1 Receive Data bus bit 0.
	RMII1_RXD1	PF.2	MFP1	I	RMII1 Receive Data bus bit 1.
	RMII1_RXERR	PF.0	MFP1	I	RMII1 Receive Data Error input pin.
	RMII1_TXD0	PF.7	MFP1	O	RMII1 Transmit Data bus bit 0.
	RMII1_TXD1	PF.6	MFP1	O	RMII1 Transmit Data bus bit 1.
	RMII1_TXEN	PF.5	MFP1	O	RMII1 Transmit Enable output pin.

The following recommendation will help users to gain maximum performance.

- Make a Stable & Low-Noise environment for Ether Net PHY working
- Make a better circuit for Ethernet PHY by simplifying signal trace
- Reduce EMI & EMC
- Make better ESD protecting

9.1 RMII PHY layout guideline (refer to IC+ IP101G design guide)

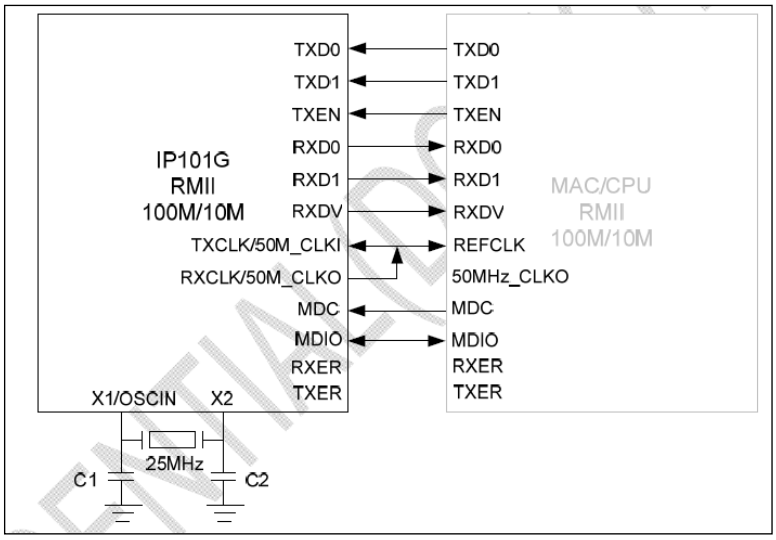


Figure 9.1-1 RMII interface connection

Block A and B may be better placed as close to magnetic as possible. Let the trace between Ethernet PHY and magnetic as short as possible, and **keep the Tx+/-(So as Rx+/-) signal traces to be symmetry**.

The traces should not be too long and **12cm** will be the maximum of path's length. When Tx, Ethernet PHY will sink current from Block A (When Auto-MDIX working, Tx<->Rx direction switch). When Rx, Ethernet PHY will take differential voltage signal from Block B **(**When Auto-MDIX working, Rx<->Tx direction switch).

Besides, the distance between **RJ-45 and magnetic should be as short as possible**. If these 2 requirements couldn't be met at the same time, the distance between Ethernet PHY and transformer might be scarified to keep the distance between RJ-45 and magnetic as short as possible.

A).The termination resistors (**50Ω** in block A & B) may be better placed as **close to magnetic** as possible. For better impedance matching, the termination resistors and caps should pay more attention to take care.

B).**ISET** (Transmit Bias Resistor Connection) pin should be placed as **close to Ethernet PHY** as possible. Furthermore, it should not be affected by other signals such as TX+/-, RX+/- and clock signal traces.

C).**Crystal (25MHz)** shouldn't be placed close to: Input /Output ports, edge of PCB board and magnetic devices. The most important thing is that crystal should not be placed close to high-frequency devices or traces, such as RMII interface signals, Tx+/-, Rx+/- and Power signals.

D).High current on the trace will induce the higher EMI noise, so it will be better to reduce the trace length to the power source when we placing the high current devices. The

magnetic device with **magnetic** field should be separated (**Isolation**) and mounted at **90°** to each other.

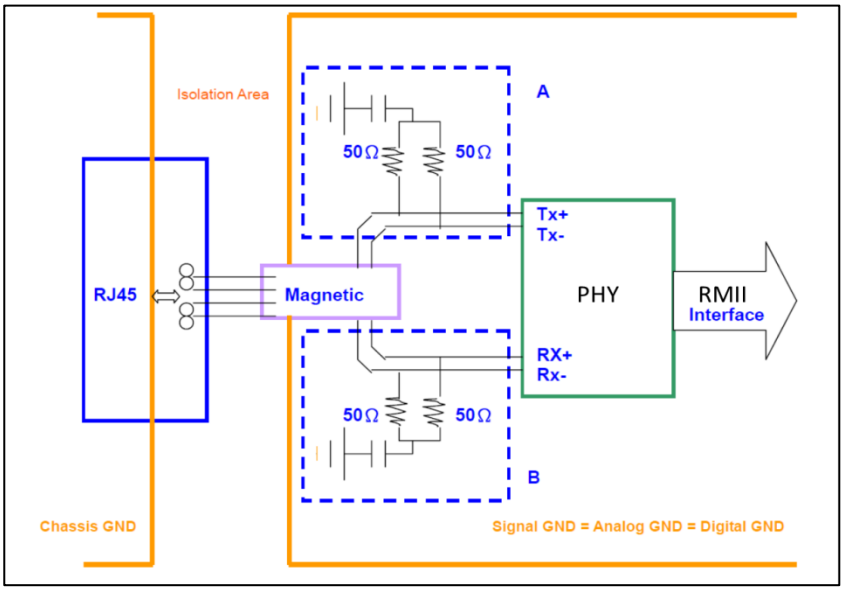


Figure 9.1-2 placement notices for RJ45 to Transformer and RMII

9.2 Power and Ground

A). It is better that do not try to partition GND at all. Never use **right angle** for all **partition** on power plane or GND plane, so as each **signal trace** should be.

B).No power and GND planes can be **underneath** the isolated area for the RJ-45 connector and magnetic. Also RJ-45 connector has its isolated GND (**Chassis GND**) to connect to RJ-45's case.

C).Try to keep the GND plane as large as possible and don't partition the GND plane for good GND return path.

9.3 Trace Routing

To reduce the propagation delay, frequency noise, cross-talk and improve the signals quality that Ethernet PHY received, and reduce the loss from transmit signals that traces routing should follow that below design rules.

9.3.1 Avoid right angle signal trace

Figure 9.3.1 PCB layout trace notice for RMII signals

9.3.2 For Tx+/−, Rx+/− traces

- Avoid signal noise or loss on these traces.
- Tx+ & Tx- should be equal length to each other.
- Rx+ & Rx- should be equal length to each other.
- The line width and distance between Tx+/− and Rx+/− could be refer as the below note,

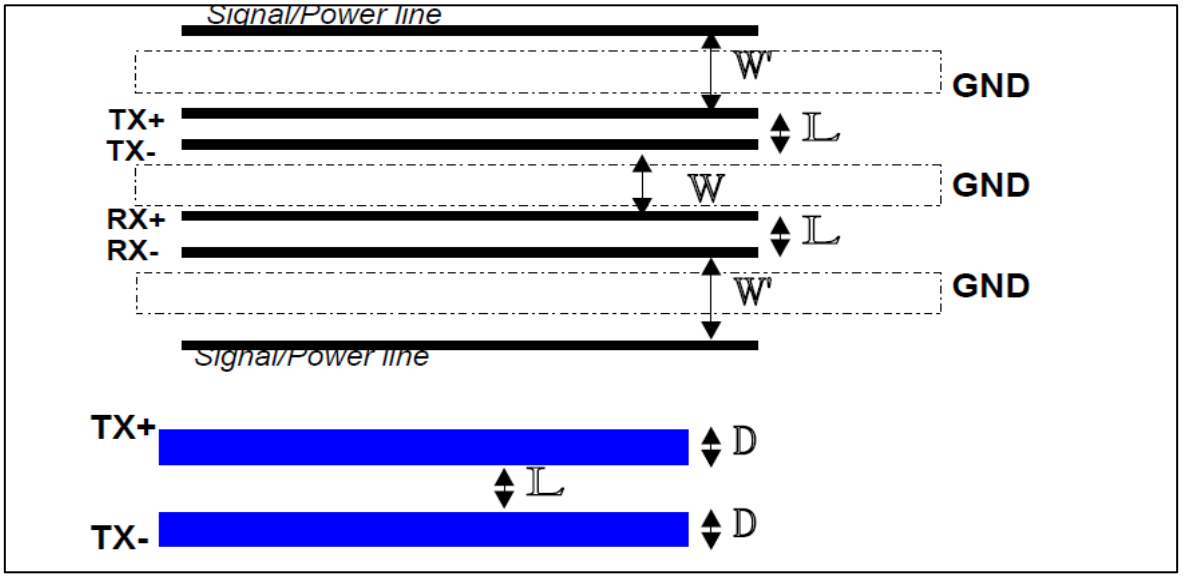


Figure 9.3.2 PCB trace line width notices for RMII to Transformer

Note.

D: Line width is as wide as possible in the range of (6mil ~ 12 mil), ex: **8mil.**
L: Width between differential pair should be small, ex: **4mil.**
W: Isolation width between TX+/- and RX+/- is as wide as possible, ex: **30mil.**
GND used as isolation is recommended.
W': Isolation width between TX/RX and noisy **signal/power** is as wide as possible, ex: **30mil**. GND used as isolation is recommended.

9.3.3 For W & W' need better isolation, ex: shielding with GND

- Try to **avoid via for TX+/-, RX+/- traces**. Via will degrade signal quality.
- Try to avoid digital signals (like Clocks or RMII signal traces) interfere with analog signals (like Tx+/-, Rx+/-, or ISET traces) and power lines.

9.3.4 Never running noisy digital signals in parallel with TX+/- and RX+/-

The traces of power, ground, and those need de-couple cap should be shorter and wider. If via are not eliminated on the trace for de-couple cap, try to enlarge the diameter of these via.

A) For some **critical signals**, clock and the other high speed signal traces should be as short and wide as possible. (Surely that is compared with normal signal traces.) And it is better having the GND plane under them, and it is even better with the GND plane around it.

B) The length of each signal trace shouldn't exceed 1/20 of the highest harmonic wavelength. For example, for the **25MHz clock trace shouldn't exceed 30cm** and for the 50**MHz** signal trace shouldn't exceed 12cm (Tx+/-, Rx+/-).

C) **De-couple cap** should be placed as close to IC as possible, and the traces should be short. Every Ethernet PHY analog/digital power needs de-couple cap and keeps the analog power close to analog GND pin, digital power close to digital GND pin. (See the diagram below)

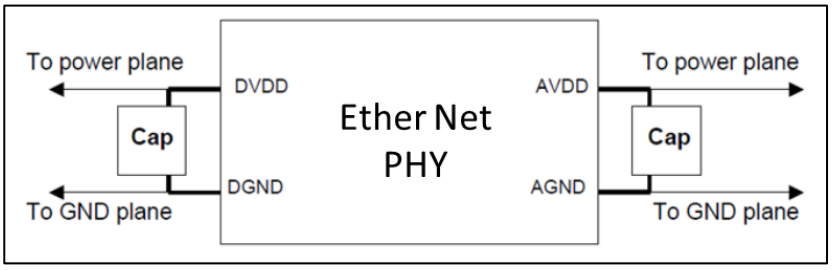


Figure 9.3.4 power plane layout notices for RMII PHY

9.3.5 Keep the distance between Tx+/- & Rx+/- differential pairs for good isolation

When these two pair of traces runs together in parallel, don't place them too close for unwanted interference. Shielding by GND planes can get a better isolation to these two differential pairs.

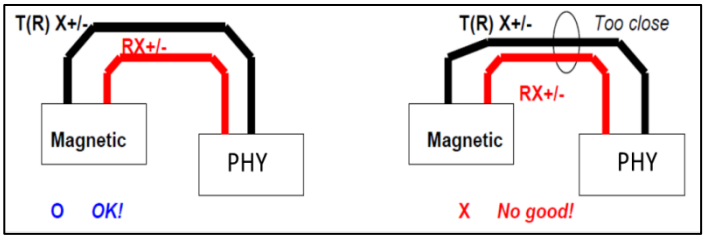


Figure 9.3.5 RMII PHY to transformer connection

A) The signal trace length difference between Tx+ and Tx- (Same as Rx+ and Rx-) should be kept as small as possible, better **within 1 inch.**

B) **Ferrite Beads** should be as close to IC pins and let it on the rating of **100Ω@100MHz.** The ferrite bead between DVDD and AVDD of Ethernet PHY pins should be placed as close to Ethernet PHY as possible, and at the same side as Ethernet PHY, not opposite side.

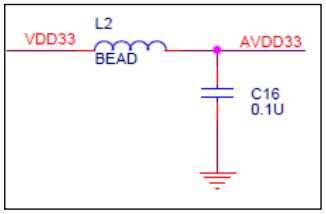


Figure 9.3.5-B RMII PHY AVDD connection

C) The ferrite bead between **REGOUT and REGIN** of Ethernet PHY pins should be placed as close to Ethernet PHY as possible, and at the same side as Ethernet PHY, not opposite side.

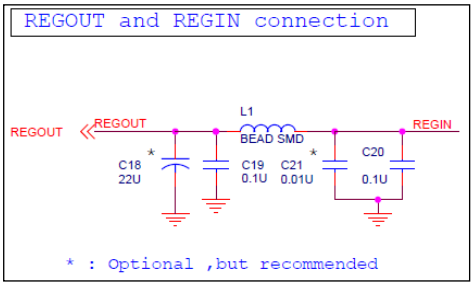


Figure 9.3.5-C RMII PHY REGOUT & REGIN connection

D) Magnetic: Any Magnetic with Tx/Rx turn ration of **1:1/1:1** are suitable for IP101, such as SINKA LS518/LS502, Bothhand TS8121C/TS6121C. Transformer supports Automdix function is recommended for better EMI performance.

9.4 Better Analog Performance

A) When using regulator such as 5V to be 3.3V, the rated current of the regulator should be at least **300mA**.

B) Both Analog GND pins and Digital GND pins must maintain a good GND return path (One GND plane is recommended. Avoid using single ended GND or making the GND plane discrete. Keep the circuit's return path back to the system's real GND as short as possible. This is especially important **for 2 layers PCB layout**.

C) When using 25MHz crystal as Ethernet PHY clock source, the spec of crystal is under **50ppm** better. Two caps attached to X1 and X2 should be close to **20pf.**

D) Avoid placing cap in the clock path when using oscillator as clock source.

E) If **EMI** of the system couldn't pass, add some de-couple caps (such as **0.1uf, 10nf, 1nf, 390pf..,** etc.) between systems Power to GND.

9.5 ESD Protecting

For ESD protection, we suggest to keep a distance at least **80mil** for good isolation, which avoid ESD energy jumping by traces nearby IC. (See the diagram below)

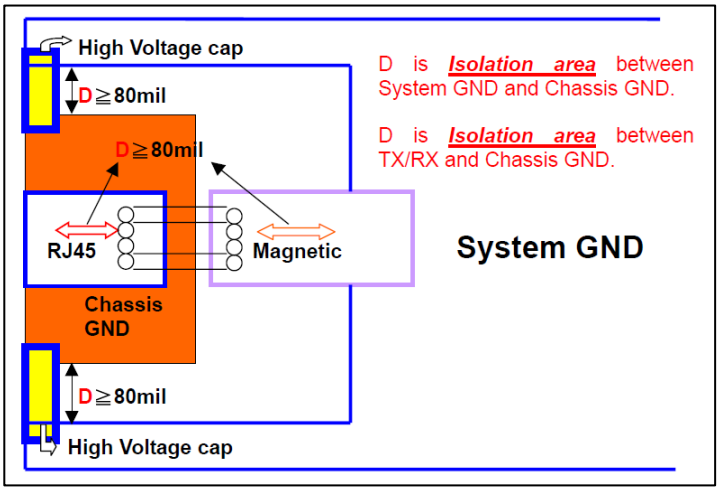


Figure 9.5 RJ45 ESD isolation distance with 80mil at least

10 Capture Sensor Interface

The Image Capture Interface is designed to capture image data from a sensor. After capturing or fetching image data, it will process the image data, and then FIFO output them into frame buffer.

NUC980 have two sets of CMOS capture sensor interfaces with supporting CCIR601 and CCIR656 type sensor and resolution up to 3M pixels. It can support YUV422 and RGB565 color format for data output by CMOS image sensor.

10.1 Pin Configuration

Table 10.1-1 video capture-0 interface pin-list

VCAP0	VCAP0_CLKO	PC.3	MFP2	O	Video image interface-0 sensor clock pin.
	VCAP0_DATA0	PC.8	MFP2	I	Video image interface-0 data pin.
	VCAP0_DATA1	PC.9	MFP2	I	Video image interface-0 data pin.
	VCAP0_DATA2	PC.10	MFP2	I	Video image interface-0 data pin.
	VCAP0_DATA3	PC.11	MFP2	I	Video image interface-0 data pin.
	VCAP0_DATA4	PC.12	MFP2	I	Video image interface-0 data pin.
	VCAP0_DATA5	PC.13	MFP2	I	Video image interface-0 data pin.
	VCAP0_DATA6	PC.14	MFP2	I	Video image interface-0 data pin.
	VCAP0_DATA7	PC.15	MFP2	I	Video image interface-0 data pin.
	VCAP0_FIELD	PC.7	MFP2	I	Video image interface-0 even/odd indicator frame sync. pin.
	VCAP0_HSYNC	PC.5	MFP2	I	Video image interface-0 horizontal sync. pin.
	VCAP0_PCLK	PC.4	MFP2	I	Video image interface-0 pixel clock pin.
	VCAP0_VSYNC	PC.6	MFP2	I	Video image interface-0 vertical sync. pin.

Table 10.1-1 video capture-2 interface pin-list

VCAP1	VCAP1_CLKO	PE.12	MFP7	O	Video image interface-1 sensor clock pin.
	VCAP1_DATA0	PE.2	MFP7	I	Video image interface-1 data pin.
	VCAP1_DATA1	PE.3	MFP7	I	Video image interface-1 data pin.
	VCAP1_DATA2	PE.4	MFP7	I	Video image interface-1 data pin.
	VCAP1_DATA3	PE.5	MFP7	I	Video image interface-1 data pin.
	VCAP1_DATA4	PE.6	MFP7	I	Video image interface-1 data pin.
	VCAP1_DATA5	PE.7	MFP7	I	Video image interface-1 data pin.
	VCAP1_DATA6	PE.8	MFP7	I	Video image interface-1 data pin.
	VCAP1_DATA7	PE.9	MFP7	I	Video image interface-1 data pin.
	VCAP1_FIELD	PE.10	MFP7	I	Video image interface-1 frame sync. pin.
	VCAP1_HSYNC	PE.0	MFP7	I	Video image interface-1 horizontal sync. pin.
	VCAP1_PCLK	PF.10	MFP7	I	Video image interface-1 pixel clock pin.
	VCAP1_VSYNC	PE.1	MFP7	I	Video image interface-1 vertical sync. pin.

10.2 Reference Connection

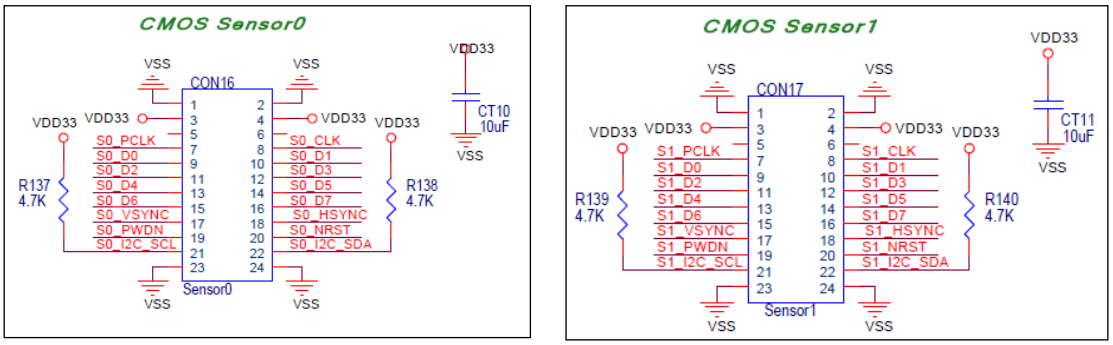


Figure 10.2-1 CMOS sensor interface connection

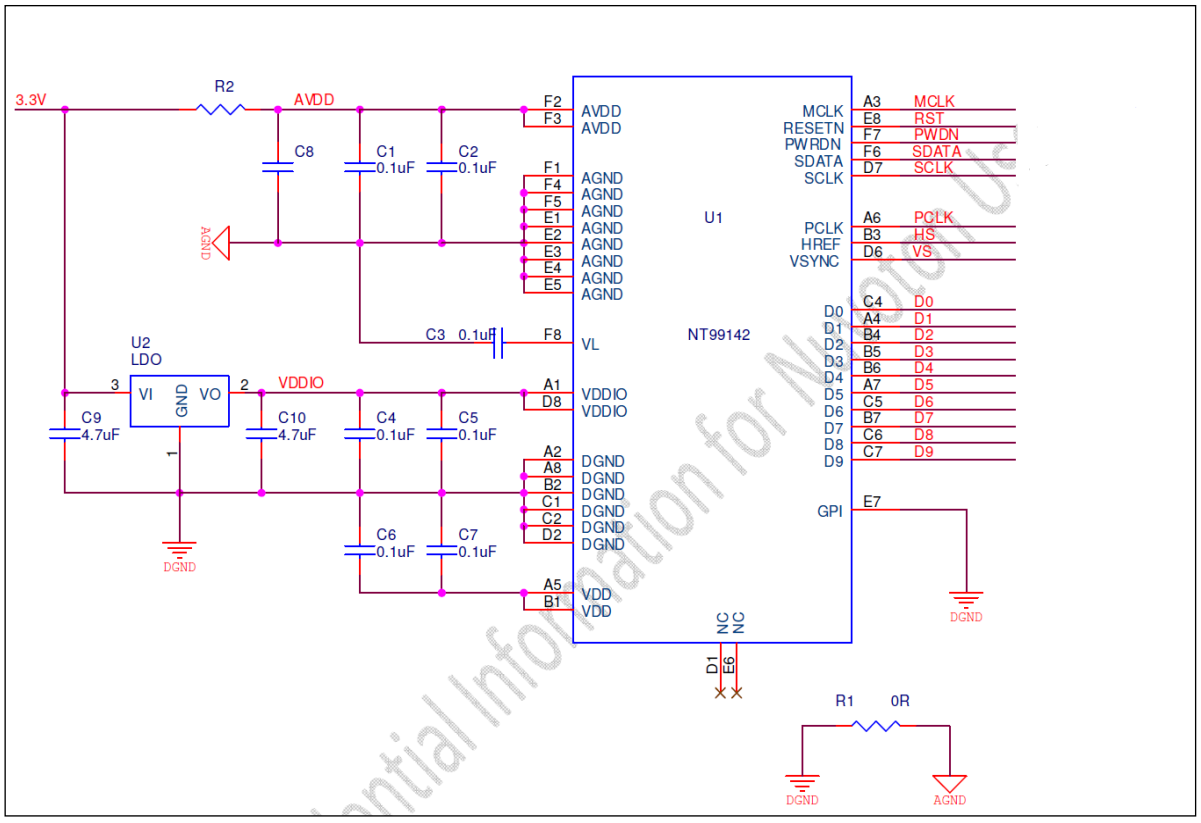
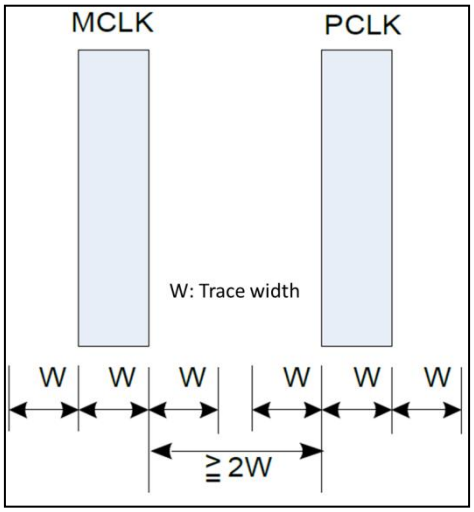


Figure 10.2-2 reference connection with NT99142 CMOS sensor

10.3 PCB Design Considerations

- Routing sequences: PCLK ➔ MCLK ➔ Data ➔ HREF ➔ VSYNC ➔ Others
- Connect GND/AGND and route ground plane as large as possible.
- Minimum gap between PCLK and MCLK trace is double of trace width (W*2).



- Route ground trace adjacent to PCLK/MCLK traces to reduce crosstalk between other traces, or route power or low frequency signal adjacent to PCLK/MCLK traces.
- Priority: GND->Power->Low frequency signals

  Note: low frequency signal: I2C/PWDN/ RESETN/VSYNC etc.
- In 2-layer design, avoid route any signal trace parallel to PCLK/MCLK nearby.
- Place Decoupling Caps as close to CMOS sensor power pins as possible, connect Cap first and then connect power pins, Decoupling Caps is recommend to get better image quality. In placement or routing issue, you may use less Cap by Cap sharing (with adjacent power pin),the Cap sharing need use larger Cap.
- When use external LDO VDD, decoupling Cap for VDD is required.
- Do not route MCLK & PCLK under Sensor, route trace outside Sensor is recommend.
- Do not route VSYNC/HREF/MCLK/PCLK traces adjacently, if possible, shield by GND trace would be better.
- In all signal trace, use Via less than 3 to get good signal quality.
- Route CMOS sensor AVDD trace directly to AVDD plane to get good image quality.

11 Quad Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller support Dual and Quad I/O Transfer mode and the controller supports PDMA function to access the data buffer.

QSPI0 supports SPI flash booting, it can support SPI-NOR and SPI-NAND types flash.

11.1 Pin Configuration

Table 11.1 QSPI0 interface pin-list

Group	Pin Name	GPIO	MFP
QSPI0	QSPI0_CLK	PD.3	MFP1
	QSPI0_MISO0	PD.5	MFP1
	QSPI0_MISO1	PD.7	MFP1
	QSPI0_MOSI0	PD.4	MFP1
	QSPI0_MOSI1	PD.6	MFP1
	QSPI0_SS0	PD.2	MFP1
	QSPI0_SS1	PA.0, PD.0	MFP1

11.2 QSPI Reference Connection

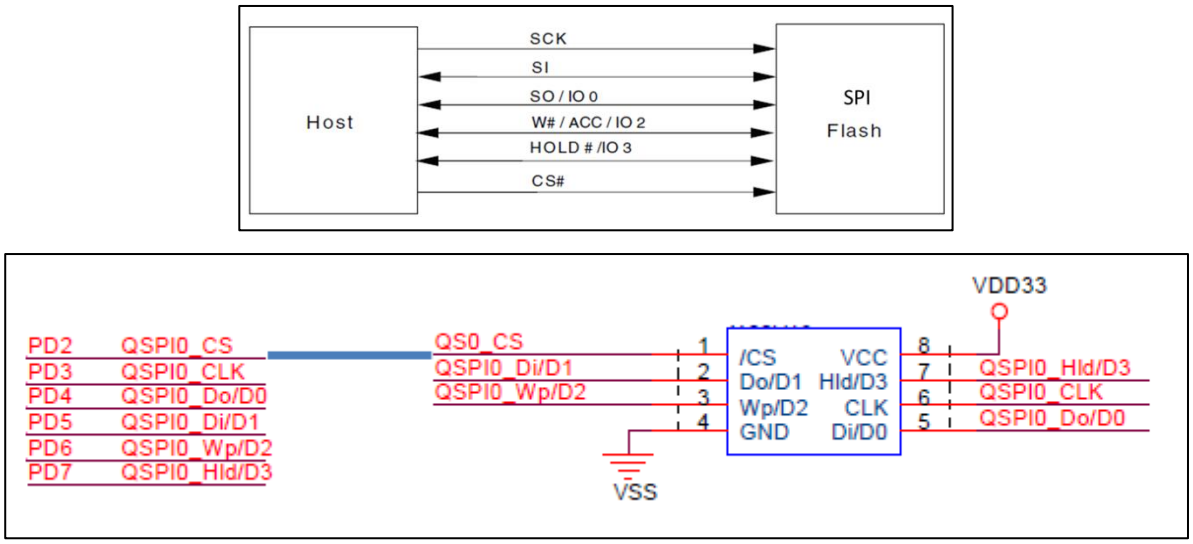


Figure 11.2 reference circuit for QSPI0 booting with SPI flash

11.3 PCB Layout Considerations for QSPI Flash

QSPI0 supports (up to 100MHz) high speed SPI flash memory device for booting.

For PCB design, standard high speed layout practices should be followed. This session provides the recommendations for PCB layout.

11.3.1 Power Supply Decoupling

The SPI Flash has one power supply pin (VCC) and one ground pin (GND). One ceramic capacitor with 0.1μF at least is recommended for power supply decoupling. This capacitor should be placed as close as possible to the power supply pin of the package.

11.3.2 Clock Signal Routing

In high speed synchronous data transfer, good signal integrity in a PCB design is of importance, especially for the clock signal. When routing the clock signal, special cares should be taken. The following practices are recommended.

- Run the clock signal at least 3x of the trace width away from all other signal traces. This helps to keep clock signal clean from noise. See the 13-3-2-1 Figure.
- Use as less via(s) as possible for the whole path of clock signal. Via will cause impedance change and signal reflection.
- Run the clock trace as straight as possible and avoid using serpentine routing. See the 13-3-2-2 Figure.
- Keep a continuous ground in the next layer as reference plane.
- Route the clock trace with controlled impedance.

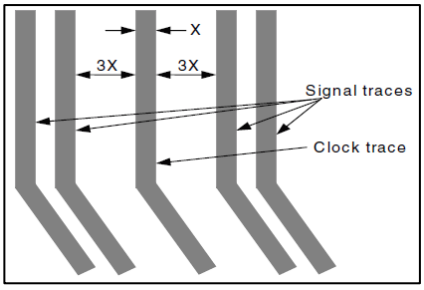


Figure 11.3.2-1 Separate SPI Clock From Other Signals

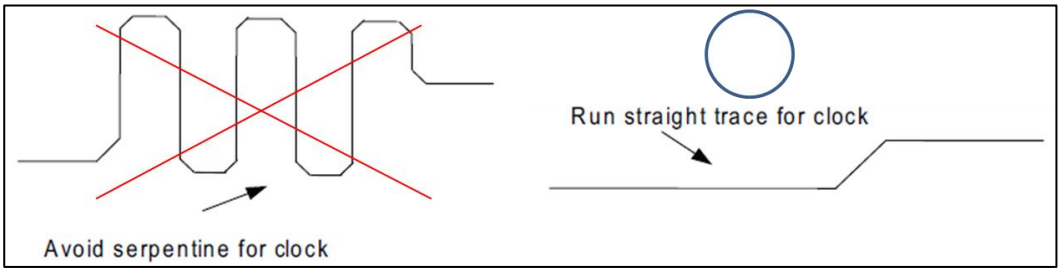


Figure 11.3.3-2 Run Straight Trace for Clock

11.3.3 Data Signal Routing

QSPI Flash has a 4-bit data bus, IO0 - IO3. In order to keep the correct timing for the data transfer, in the PCB routing, the data traces should match the time delay with the clock trace from the host controller to the Flash. The data signals should be routed with the traces of controlled impedance to reduce the signal reflection. It should be avoided to route the traces with 90 angle corner. The recommendation is to cut the corner and smooth the trace when trace route needs to change direction.

Figure 5 shows the example of trace routing at the corner. To further improve the signal integrity, it should be considered to avoid using multiple signal layers for data signal routing. All signal traces should have a continuous reference plane.

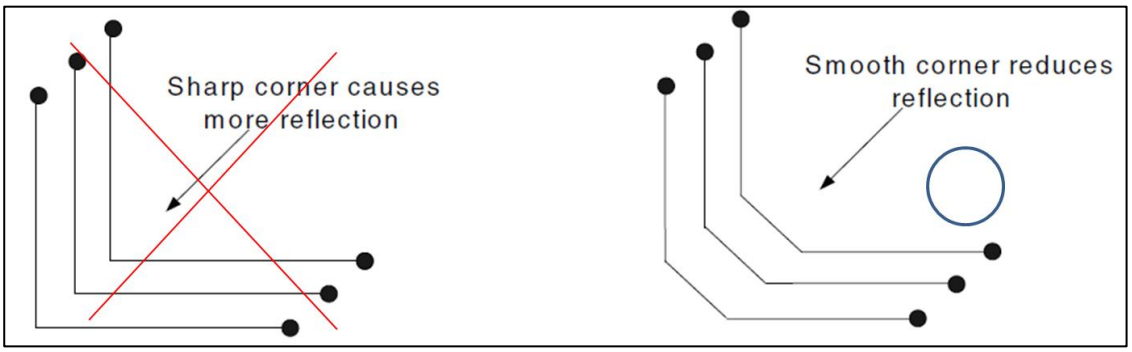


Figure 11.3.3 Signal Routing at the Corner

11.3.4 Recommendations

The following is a check list of PCB design recommendations.

- Put the decoupling capacitor as close as possible to the power pin. A value of around 0.1 μF ceramic capacitor with 0603/0402 package is a good choice.
- Clock should be routed straight and with less via if possible. Separation of clock and other signals is important to make the clock clean.
- All signal traces should go with a solid reference plane (either GND or VCC).
- All signals should be routed with controlled impedance. Typically, the PCB is recommended to be built using 50-75 Ohm trace impedance with +/- 5% tolerance.
- Data bus should be routed with matching length to the reference of the clock. The matching length, typically, is recommended within +/- 150 mils.

12 Controller Area Network (CAN) Interface

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high speed networks to low cost multiple wiring. The maximum signaling rate is 1 Mbps.

NUC980 have four sets of CAN 2.0B controllers, each supports 32 Message Objects; each Message Object has its own identifier mask.

CAN controller performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

12.1 Pin Configuration

Table 12.1 CAN interface pin-list

Group	Pin Name	GPIO	MFP	Type	Description
CAN0	CAN0_RXD	PC.3	MFP7	I	CAN0 bus receiver input.
		PD.6	MFP4	I	
		PG.11	MFP4	I	
		PE.0	MFP2	I	
	CAN0_TXD	PC.4	MFP7	O	CAN0 bus transmitter output.
		PD.7	MFP4	O	
		PG.12	MFP4	O	
		PE.1	MFP2	O	
CAN1	CAN1_RXD	PA.13	MFP5	I	CAN1 bus receiver input.
		PD.14	MFP4	I	
		PG.13	MFP4	I	
		PE.2	MFP2	I	
	CAN1_TXD	PA.14	MFP5	O	CAN1 bus transmitter output.
		PD.15	MFP4	O	
		PG.14	MFP4	O	
		PE.3	MFP2	O	
CAN2	CAN2_RXD	PA.15	MFP5	I	CAN2 bus receiver input.
		PB.1	MFP4	I	
		PB.8	MFP3	I	
		PD.12	MFP4	I	
		PE.4	MFP2	I	
	CAN2_TXD	PG.10	MFP5	O	CAN2 bus transmitter output.
		PB.3	MFP4	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PC.0	MFP3	O	
		PD.13	MFP4	O	
		PE.5	MFP2	O	
CAN3	CAN3_RXD	PA.0	MFP7	I	CAN3 bus receiver input.
		PE.6	MFP2	I	
		PE.10	MFP2	I	
	CAN3_TXD	PA.1	MFP7	O	CAN3 bus transmitter output.
		PE.7	MFP2	O	
		PE.12	MFP2	O	

12.2 Reference Connection

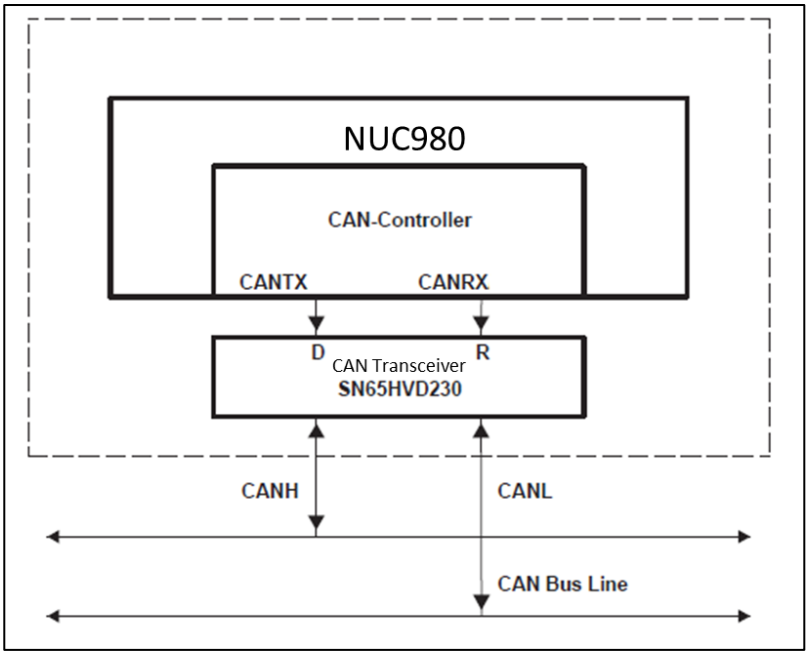


Figure 12.2-1 CAN BUS Connectivity

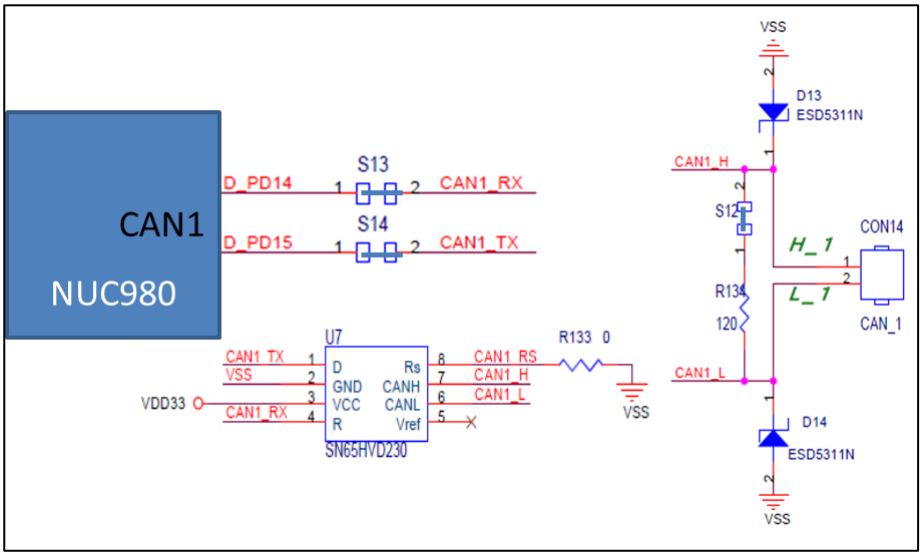


Figure 12.2-2 reference circuit for CAN BUS transceiver connection

12.3 CAN BUS Layout Recommendations

The following points should be considered to achieve best performance:

- It is recommended to place the CAN transceiver as close as possible to the ECU connector in order to minimize track length of bus lines.
- CAN Tx and Rx connections to NUC980 should be as short as possible.
- Place one 100nF capacitors close to CAN transceiver VCC, it is recommended to use ceramic capacitors.
- For EMI improvement maybe a CMC (common mode choke) is used, it has to be placed as close as possible to the transceiver bus pin CANH and CANL.
- Avoid routing CANH and CANL in parallel to fast-switching or off-board signals in order to reduce noise injection to the bus.
- Avoid routing digital signals in parallel to CANH and CANL.
- CANH and CANL tracks should have the same length. They should be routed symmetrically close together with smooth edges.
- Avoid routing transceiver GND and NUC980 GND in serial. GND connector should be placed as close as possible to the transceiver.

13 FMI NAND & SD/eMMC Interfaces

NUC980 Flash Memory Interface (FMI) controller has DMA unit and FMI unit. The DMA unit provides a DMA (Direct Memory Access) function for FMI to exchange data between system memory (ex. SDRAM) and shared buffer (128 bytes), and the FMI unit control the interface of SD0/eMMC0 or NAND flash. The interface controller can support SD0/eMMC0 (4-bit data mode) and NAND-type flash booting and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

NUC980 Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD1/eMMC1. The SD Host Controller can support SD1/eMMC1 (4-bit data mode) booting and cooperated with DMAC to provide a fast data transfer between system memory and cards.

13.1 Pin Configuration

Table 13.1-1 NAND interface pin-list

NAND	NAND_ALE	PC.3	MFP3	I	NAND Flash address latch enable.
	NAND_CLE	PC.4	MFP3	I	NAND Flash command latch enable.
	NAND_DATA0	PC.8	MFP3	I/O	NAND Flash date input/output.
	NAND_DATA1	PC.9	MFP3	I/O	NAND Flash date input/output.
	NAND_DATA2	PC.10	MFP3	I/O	NAND Flash date input/output.
	NAND_DATA3	PC.11	MFP3	I/O	NAND Flash date input/output.
	NAND_DATA4	PC.12	MFP3	I/O	NAND Flash date input/output.
	NAND_DATA5	PC.13	MFP3	I/O	NAND Flash date input/output.
	NAND_DATA6	PC.14	MFP3	I/O	NAND Flash date input/output.
	NAND_DATA7	PC.15	MFP3	I/O	NAND Flash date input/output.
	NAND_RDY0	PC.7	MFP3	I	NAND Flash ready/busy input.
	NAND_nCS0	PC.1	MFP3	I	NAND Flash chip enable input.
	NAND_nRE	PC.6	MFP3	I	NAND Flash read enable.
	NAND_nWE	PC.5	MFP3	I	NAND Flash write enable.
	NAND_nWP	PC.2	MFP3	I	NAND Flash write protect input.

Table 13.1-2 SD/eMMC interfaces pin-list

SD0/eMMC0	SD0_CLK eMMC0_CLK	PC.6	MFP6	O	SD0 clock output pin eMMC0 clock output pin
	SD0_CMD eMMC0_CMD	PC.5	MFP6	I/O	SD0 command/response pin eMMC0 command/response pin
	SD0_DATA0 eMMC0_DATA0	PC.7	MFP6	I/O	SD0 data line bit 0. eMMC0 data line bit 0.
	SD0_DATA1 eMMC0_DATA1	PC.8	MFP6	I/O	SD0 data line bit 1. eMMC0 data line bit 1.
	SD0_DATA2 eMMC0_DATA2	PC.9	MFP6	I/O	SD0 data line bit 2. eMMC0 data line bit 2.
	SD0_DATA3 eMMC0_DATA3	PC.10	MFP6	I/O	SD0 data line bit 3. eMMC0 data line bit 3.
	SD0_nCD	PB.8	MFP6	I	SD0 card detect input pin
		PC.12	MFP6	I	
SD1/eMMC1	SD1_CLK eMMC1_CLK	PF.1	MFP2	O	SD1 clock output pin eMMC1 clock output pin
	SD1_CMD eMMC1_CMD	PF.0	MFP2	I/O	SD1 command/response pin eMMC1 command/response pin
	SD1_DATA0 eMMC1_DATA0	PF.2	MFP2	I/O	SD1 data line bit 0. eMMC1 data line bit 0.
	SD1_DATA1 eMMC1_DATA1	PF.3	MFP2	I/O	SD1 data line bit 1. eMMC1 data line bit 1.
	SD1_DATA2 eMMC1_DATA2	PF.4	MFP2	I/O	SD1 data line bit 2. eMMC1 data line bit 2.
	SD1_DATA3 eMMC1_DATA3	PF.5	MFP2	I/O	SD1 data line bit 3. eMMC1 data line bit 3.
	SD1_nCD	PF.6	MFP2	I	SD1 card detect input pin

13.2 FMI Reference Connection

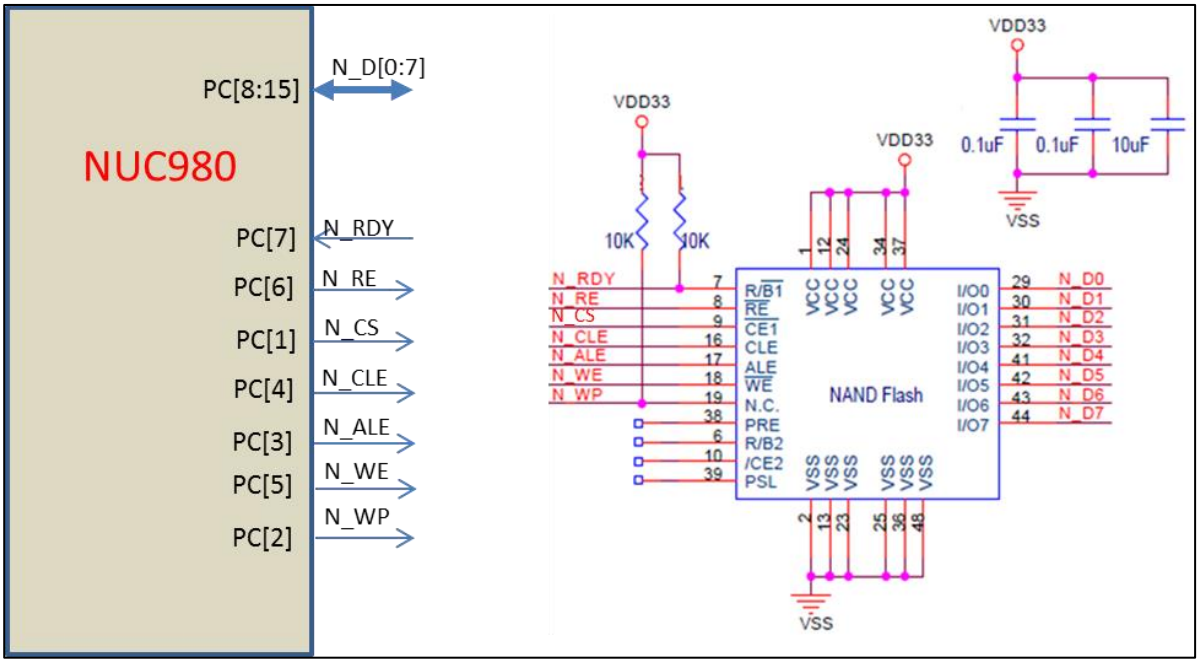


Figure 13.2-1 reference circuit for NAND Flash connectivity

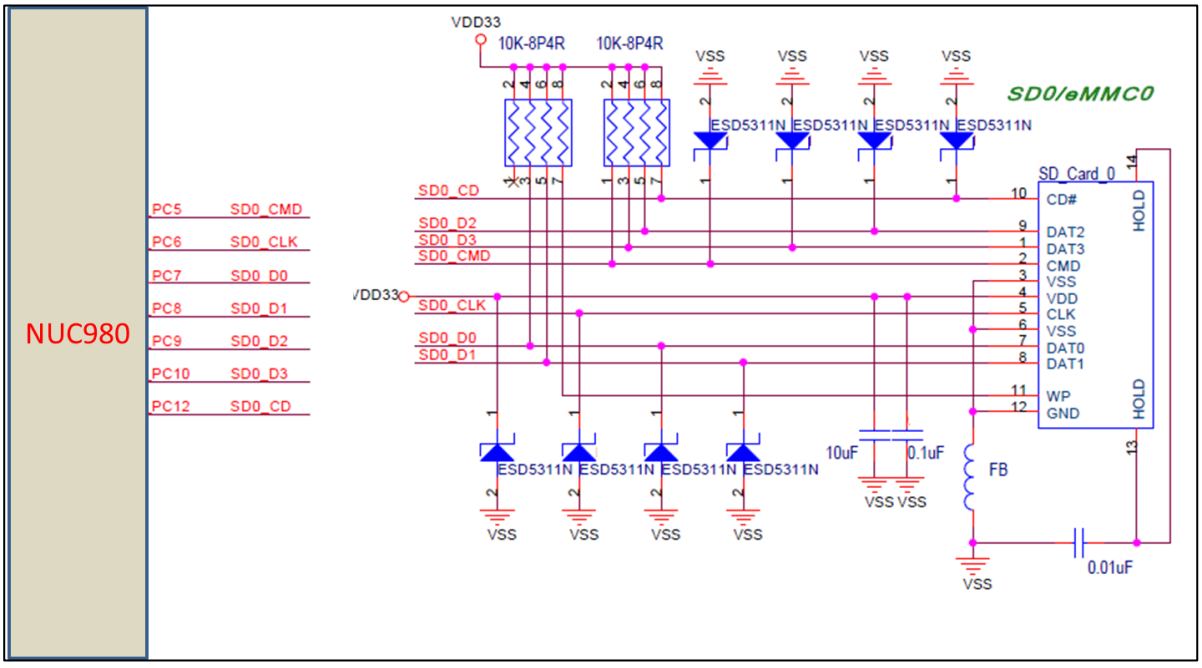


Figure 13.2-2 reference circuit for SD0/eMMC0 connectivity with PC port

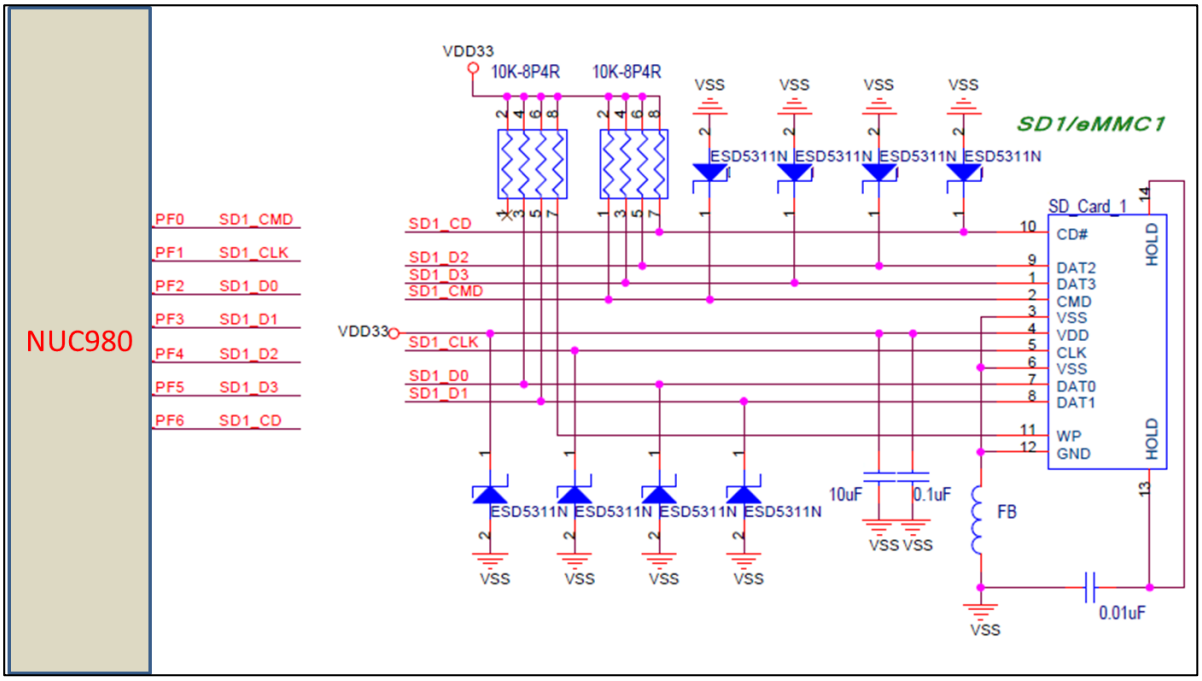


Figure 13.2-3 reference circuit for SD1/eMMC1 connectivity with PC port

13.3 General PCB Signal Routing Guidelines

The following general guidelines must be considered before and throughout the PCB layout design effort:

- Use the VSS plane as a primary reference or return path for all signals. Power should only be considered as secondary reference option where a solid continuous ground reference is also present.
- Avoid multiple via on reference planes to eliminate or minimize return current discontinuity.
- Try to avoid routing signal traces at the edge of the reference plane.
- Route the identified longest signal trace first before routing and adjusting the length of other signal traces.
- Route the same signal groups on the same signal layer and follow the routing from pin to pin as a group (that is, route them together).
- Isolate the ground return path of analog signals from digital signals; i.e. separate digital and analog grounds.
- For SD connectivity, if SD_CLK has serials a resistor for signal quality recovery that it should be placed to NUC980 side ASAP.
- About ESD protection parts for SD, the ESD parts location must close to SD connector side ASAP and also need to use low capacitance CL value to avoid that side-effect what SDHC memory card accesses at SD_CLK 50MHz.

14 I²C, SPI & I²S Interfaces

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. NUC980 provides 4 sets of I²C devices with Master/Slave mode, it supports Standard mode (100kbps), Fast mode (400kbps) and Fast mode plus (1Mbps), it can support SMBus and PMBus and with PDMA operation.

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. NUC980 except for one QSPI controller and also have up to 2 sets of SPI controllers to support Master or Slave mode operation, Master mode up to 100MHz and Slave mode up to 100MHz. Each SPI controller can support the PDMA function to access the data buffer.

The I²S controller consists of I²S and PCM protocols to interface with external audio CODEC. The I²S and PCM interface supports 8, 16, 18, 20 and 24-bit left/right precision in record and playback. NUC980 has one set of I²S controller use DMA to playback and record data with interrupt, it supports I²S interface record and playback with mater and slave mode, also support PCM interface record and playback with master mode only.

14.1 Pin Configuration

Table 14.1-1 I2C0/1/2/3 interfaces pin-list

I2C0	I2C0_SCL	PA.1	MFP3	I/O	I2C0 clock pin.
		PG.10	MFP2	I/O	
		PE.12	MFP6	I/O	
	I2C0_SDA	PA.0	MFP3	I/O	I2C0 data input/output pin.
		PA.15	MFP2	I/O	
		PE.10	MFP6	I/O	
I2C1	I2C1_SCL	PA.14	MFP2	I/O	I2C1 clock pin.
		PB.4	MFP2	I/O	
		PC.3	MFP4	I/O	
	I2C1_SDA	PA.13	MFP2	I/O	I2C1 data input/output pin.
		PB.6	MFP2	I/O	
		PC.4	MFP4	I/O	
I2C2	I2C2_SCL	PB.5	MFP2	I/O	I2C2 clock pin.
		PB.8	MFP2	I/O	
	I2C2_SDA	PB.7	MFP2	I/O	I2C2 data input/output pin.
		PC.0	MFP2	I/O	
I2C3	I2C3_SCL	PB.3	MFP2	I/O	I2C3 clock pin.
		PD.14	MFP3	I/O	
	I2C3_SDA	PB.1	MFP2	I/O	I2C3 data input/output pin.

Table 14.1-2 SPI0/1 interfaces pin-list

SPI0	SPI0_CLK	PC.6	MFP5	I/O	SPI0 serial clock pin.
		PD.9	MFP1	I/O	
	SPI0_MISO	PC.8	MFP5	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PD.11	MFP1	I/O	
	SPI0_MOSI	PC.4	MFP6	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PC.7	MFP5	I/O	
		PC.14	MFP5	I/O	
		PD.10	MFP1	I/O	
	SPI0_SS0	PC.5	MFP5	I/O	SPI0 slave select 0 pin.
		PD.8	MFP1	I/O	
	SPI0_SS1	PB.3	MFP6	I/O	SPI0 slave select 1 pin.
		PC.0	MFP5	I/O	
		PD.1	MFP1	I/O	
		PG.15	MFP1	I/O	
SPI1	SPI1_CLK	PG.10	MFP6	I/O	SPI1 serial clock pin.
		PB.4	MFP6	I/O	
		PB.10	MFP5	I/O	
		PG.12	MFP2	I/O	
	SPI1_MISO	PB.5	MFP6	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PB.12	MFP5	I/O	
		PG.14	MFP2	I/O	
	SPI1_MOSI	PB.7	MFP6	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PB.11	MFP5	I/O	
		PG.13	MFP2	I/O	
	SPI1_SS0	PA.15	MFP6	I/O	SPI1 slave select 0 pin.
		PB.6	MFP6	I/O	
		PB.9	MFP5	I/O	
		PG.11	MFP2	I/O	
	SPI1_SS1	PB.1	MFP6	I/O	SPI1 slave select 1 pin.

Table 14.1-3 I²S interface pin-list

I2S	I2S_BCLK	PA.3	MFP2	O	I2S bit clock output pin.
		PG.10	MFP8	O	
		PB.4	MFP3	O	
	I2S_DI	PA.4	MFP2	I	I2S data input pin.
		PB.7	MFP3	I	
	I2S_DO	PA.5	MFP2	O	I2S data output pin.
		PB.5	MFP3	O	
	I2S_LRCK	PA.2	MFP2	O	I2S left right channel clock output pin.
		PA.15	MFP8	O	
		PB.6	MFP3	O	
	I2S_MCLK	PA.6	MFP2	O	I2S master clock output pin.
		PB.1	MFP3	O	

14.2 Reference Connection

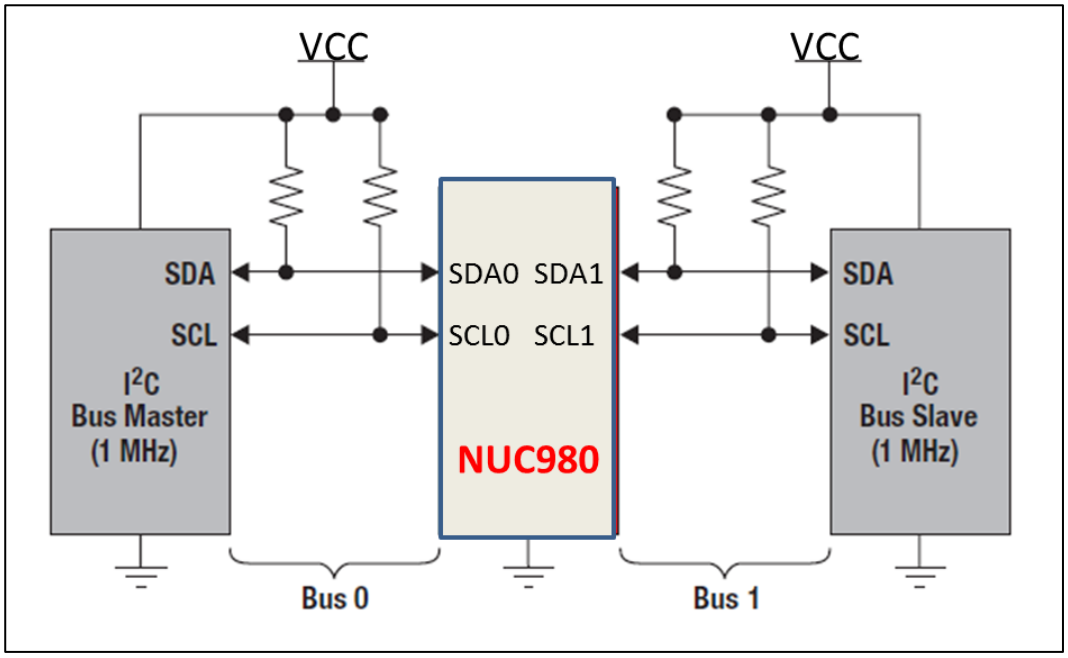


Figure 14.2-1 I²C Application Block Diagram

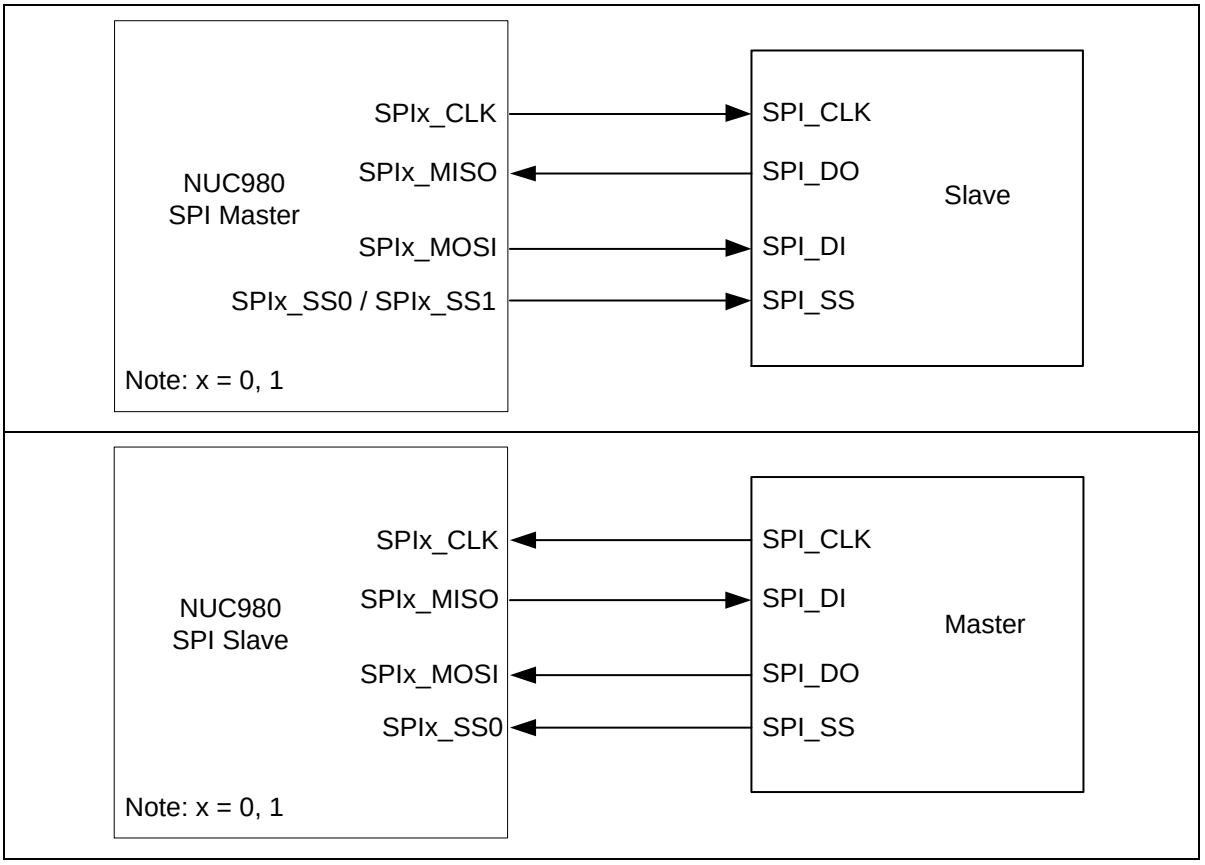
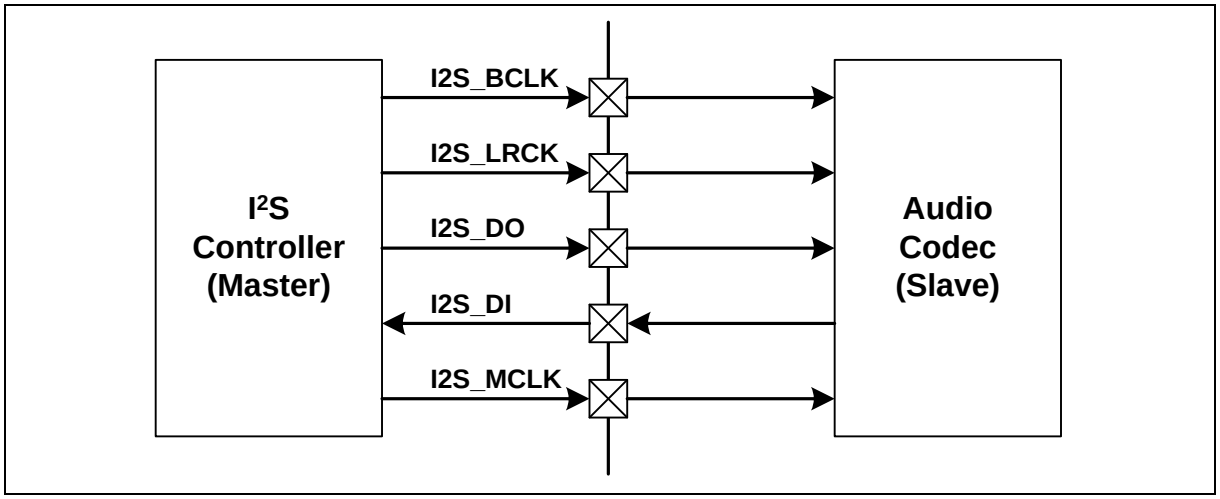


Figure 14.2-2 SPI0/1 Application Block Diagram



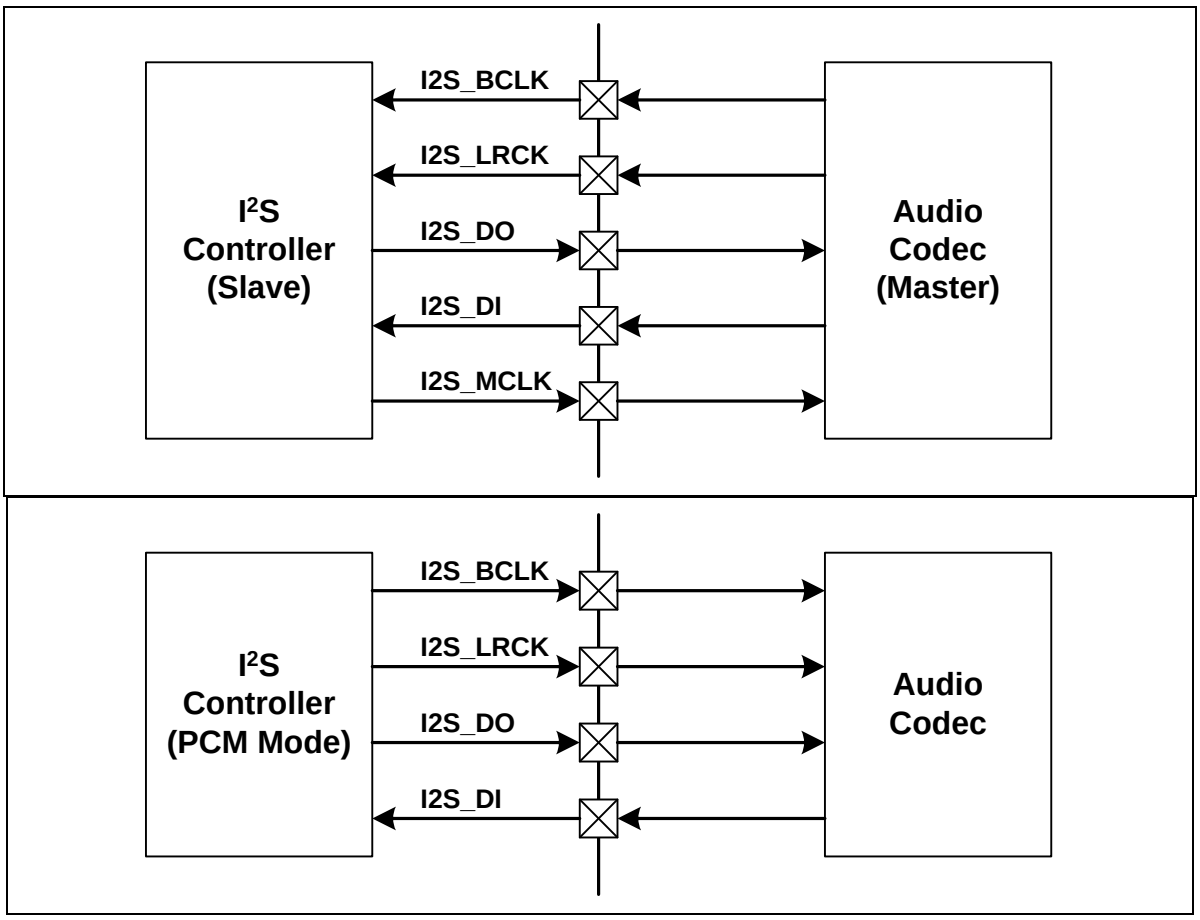


Figure 14.2-3 I²S Application Block Diagram

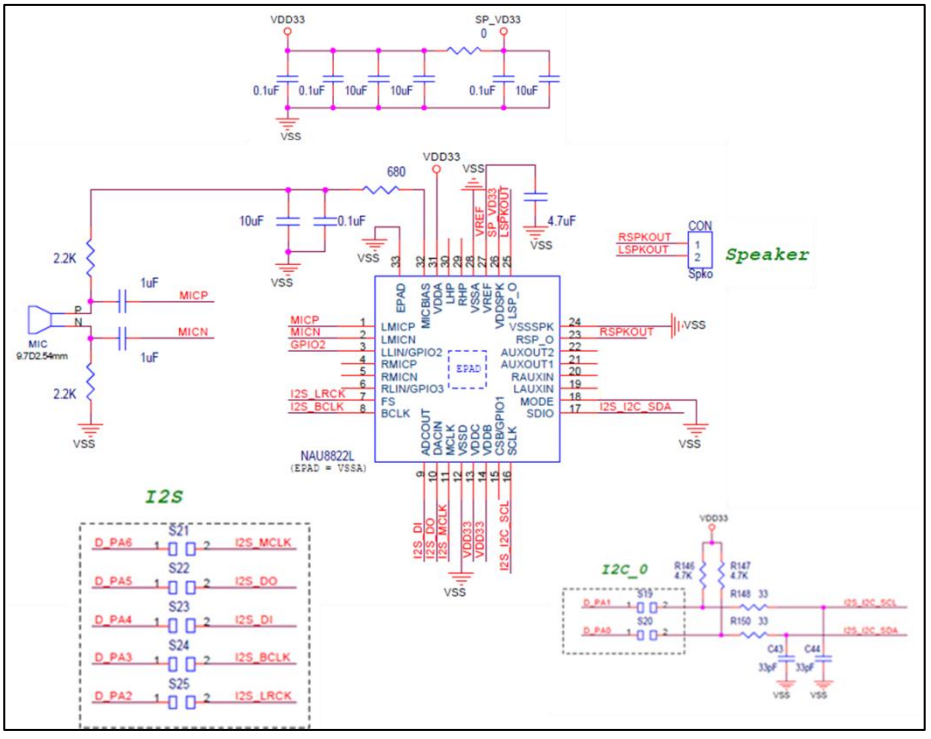


Figure 14.2-4 I²C & I²S connectivity with external audio codec

14.3 PCB Layout Considerations

14.3.1 I²C

The I²C bus is a world standard over thousands different ICs manufactured. Additionally, the I²C bus is used in various control architectures such as System Management Bus (SMBus), Power Management Bus (PMBus). Serial, 8-bit, bi-directional data transfers can be made at up to 100 Kbit/s in Standard-mode, up to 400Kbit/s in Fast-mode, or up to 1Mbit/s in Fast-mode Plus, also up to 3.4 Mbit/s in High-speed mode.

PCB design should be have spike rejection filter on the bus data line to preserve data integrity. The number of ICs that can be connected to the same bus is limited only by the maximum bus capacitance. More capacitance may be allowed under some conditions. As the figure 16-4 reserved the serial resistor and capacitor of termination for I²C bus signals integrity preservation.

14.3.2 SPI

The Serial Peripheral Interface (SPI) bus is a full duplex synchronous serial communication interface specification used for short distance communication. SPI devices communicate in full duplex mode using Master-Slave architecture with a single master. The master device originates the frame for reading and writing. Multiple slave devices are supported through selection, with individual slaves selected by CS lines.

The NUC980 may be configurable as a SPI master or slave depending on the application, with two SPI devices that can be used. The SPI interface could be an external serial flash or application processor that needs to be configurable to different memory maps.

Same as QSPI0, SPI CLK speed also supports up to 100MHz, about the PCB layout consideration can be follow up.

14.3.3 I²S

NUC980 development board provides I²S interface and connected with an external audio codec NAU8822L shown as the figure 16-4. The driver of the I²S device is available for now.

I²S is a digital audio interface can connect to master/slave device directly without concerns, regarding to device’s quality and performance, such as NAU8822L audio codec, please refer to the NAU8822L design guidelines.

15 UART & Smart Card Interface (ISO/IEC 7816-3)

The NUC980 provides 10 channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. NUC980 provides up to two ISO-7816-3 ports. It has separated receive/transmit 4 byte entry FIFO for data payloads can support UART mode with Full duplex, asynchronous communications.

15.1 Pin Configuration

Table 15.1-1 UART[0..9] interfaces pin-list

UART0	UART0_RXD	PF.11	MFP1	I	UART0 data receiver input pin.
	UART0_TXD	PF.12	MFP1	O	UART0 data transmitter output pin.
UART1	UART1_CTS	PC.8	MFP7	I	UART1 clear to Send input pin.
		PF.7	MFP2	I	
	UART1_RTS	PC.7	MFP7	O	UART1 request to Send output pin.
		PF.8	MFP2	O	
	UART1_RXD	PA.0	MFP4	I	UART1 data receiver input pin.
		PC.6	MFP7	I	
		PF.9	MFP2	I	
	UART1_TXD	PA.1	MFP4	O	UART1 data transmitter output pin.
		PC.5	MFP7	O	
		PF.10	MFP2	O	
UART2	UART2_CTS	PA.7	MFP2	I	UART2 clear to Send input pin.
		PG.2	MFP2	I	
		PB.0	MFP2	I	
	UART2_RTS	PA.8	MFP2	O	UART2 request to Send output pin.
		PG.3	MFP2	O	
	UART2_RXD	PA.9	MFP2	I	UART2 data receiver input pin.
		PG.0	MFP2	I	
		PD.7	MFP2	I	
	UART2_TXD	PA.10	MFP2	O	UART2 data transmitter output pin.
		PG.1	MFP2	O	
		PD.6	MFP2	O	

UART3	UART3_CTS	PB.12	MFP1	I	UART3 clear to Send input pin.
		PD.5	MFP2	I	
		PF.4	MFP5	I	
	UART3_RTS	PB.11	MFP1	O	UART3 request to Send output pin.
		PD.4	MFP2	O	
		PF.5	MFP5	O	
	UART3_RXD	PC.4	MFP5	I	UART3 data receiver input pin.
		PB.10	MFP1	I	
		PD.3	MFP2	I	
		PF.6	MFP5	I	
	UART3_TXD	PC.3	MFP5	O	UART3 data transmitter output pin.
		PB.9	MFP1	O	
		PD.2	MFP2	O	
		PB.13	MFP5	O	
		PF.7	MFP5	O	
UART4	UART4_CTS	PD.15	MFP1	I	UART4 clear to Send input pin.
		PE.0	MFP5	I	
	UART4_RTS	PD.14	MFP1	O	UART4 request to Send output pin.
		PE.1	MFP5	O	
	UART4_RXD	PC.10	MFP7	I	UART4 data receiver input pin.
		PD.13	MFP1	I	
		PE.2	MFP5	I	
	UART4_TXD	PC.9	MFP7	O	UART4 data transmitter output pin.
		PD.12	MFP1	O	
		PE.3	MFP5	O	
UART5	UART5_CTS	PG.4	MFP2	I	UART5 clear to Send input pin.
		PG.11	MFP5	I	
	UART5_RTS	PG.5	MFP2	O	UART5 request to Send output pin.
		PG.12	MFP5	O	
	UART5_RXD	PG.6	MFP2	I	UART5 data receiver input pin.
		PD.1	MFP2	I	
		PG.13	MFP5	I	
	UART5_TXD	PG.7	MFP2	O	UART5 data transmitter output pin.
		PD.0	MFP2	O	
		PG.14	MFP5	O	
UART6	UART6_CTS	PA.2	MFP1	I	UART6 clear to Send input pin.
		PD.8	MFP2	I	

	UART6_RTS	PA.3	MFP1	O	UART6 request to Send output pin.
		PD.9	MFP2	O	
	UART6_RXD	PA.4	MFP1	I	UART6 data receiver input pin.
		PD.11	MFP2	I	
		PE.8	MFP5	I	
	UART6_TXD	PA.5	MFP1	O	UART6 data transmitter output pin.
		PD.10	MFP2	O	
		PE.9	MFP5	O	
UART7	UART7_CTS	PB.7	MFP5	I	UART7 clear to Send input pin.
		PF.0	MFP5	I	
	UART7_RTS	PB.5	MFP5	O	UART7 request to Send output pin.
		PF.1	MFP5	O	
	UART7_RXD	PA.14	MFP6	I	UART7 data receiver input pin.
		PB.4	MFP5	I	
		PC.2	MFP4	I	
		PF.2	MFP5	I	
	UART7_TXD	PA.13	MFP6	O	UART7 data transmitter output pin.
		PB.6	MFP5	O	
		PC.1	MFP4	O	
		PF.3	MFP5	O	
UART8	UART8_CTS	PG.9	MFP2	I	UART8 clear to Send input pin.
		PC.15	MFP7	I	
	UART8_RTS	PG.8	MFP2	O	UART8 request to Send output pin.
		PC.14	MFP7	O	
	UART8_RXD	PA.11	MFP2	I	UART8 data receiver input pin.
		PC.0	MFP4	I	
		PC.13	MFP7	I	
	UART8_TXD	PA.12	MFP2	O	UART8 data transmitter output pin.
		PB.8	MFP4	O	
		PC.12	MFP7	O	
UART9	UART9_CTS	PE.4	MFP5	I	UART9 clear to Send input pin.
	UART9_RTS	PB.2	MFP7	O	UART9 request to Send output pin.
		PE.5	MFP5	O	
	UART9_RXD	PB.3	MFP7	I	UART9 data receiver input pin.
		PE.6	MFP5	I	
		PE.10	MFP3	I	
	UART9_TXD	PB.1	MFP7	O	UART9 data transmitter output pin.

		PE.7	MFP5	O	
		PE.12	MFP3	O	

Table 15.1-1 SMART Card0/1 interfaces pin-list

SC0	SC0_CD	PA.2	MFP3	I	Smart Card 0 card detect pin.
		PC.15	MFP4	I	
	SC0_CLK	PA.5	MFP3	O	Smart Card 0 clock pin.
		PC.12	MFP4	O	
	SC0_DAT	PA.4	MFP3	I/O	Smart Card 0 data pin.
		PC.13	MFP4	I/O	
	SC0_PWR	PA.3	MFP3	O	Smart Card 0 power pin.
		PC.14	MFP4	O	
	SC0_RST	PA.6	MFP3	O	Smart Card 0 reset pin.
		PC.11	MFP4	O	
SC1	SC1_CD	PC.10	MFP4	I	Smart Card 1 card detect pin.
		PF.4	MFP4	I	
	SC1_CLK	PC.7	MFP4	O	Smart Card 1 clock pin.
		PF.1	MFP4	O	
	SC1_DAT	PC.8	MFP4	I/O	Smart Card 1 data pin.
		PF.2	MFP4	I/O	
	SC1_PWR	PC.9	MFP4	O	Smart Card 1 power pin.
		PF.3	MFP4	O	
	SC1_RST	PC.6	MFP4	O	Smart Card 1 reset pin.
		PF.0	MFP4	O	

15.2 Reference Connection

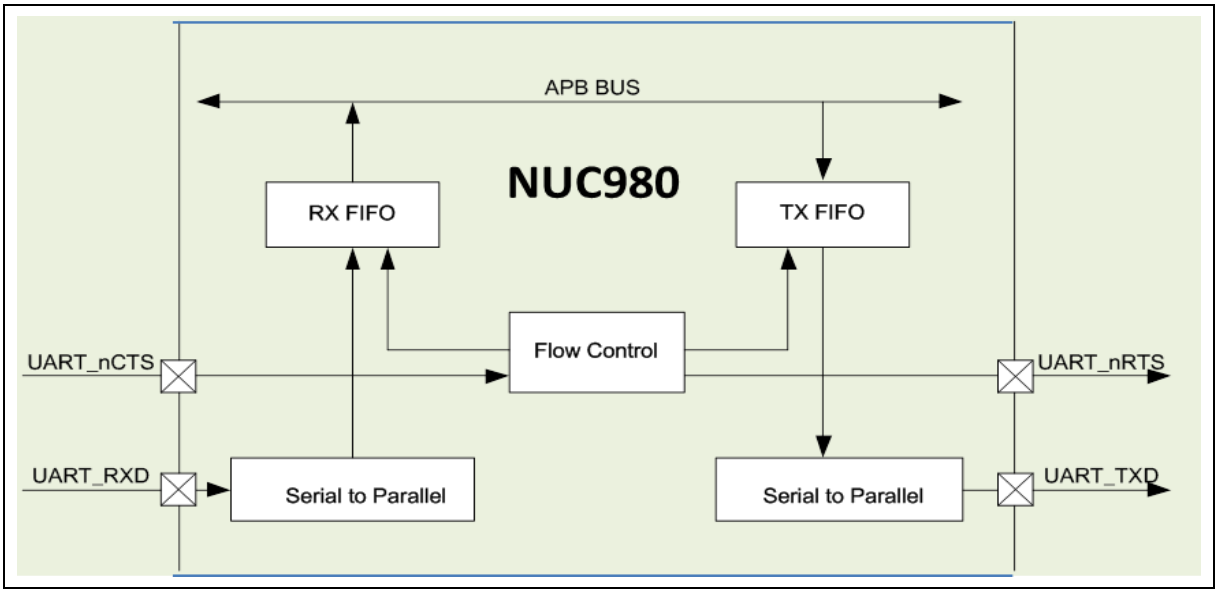


Figure 15.2-1 UART with Control Flow Block Diagram

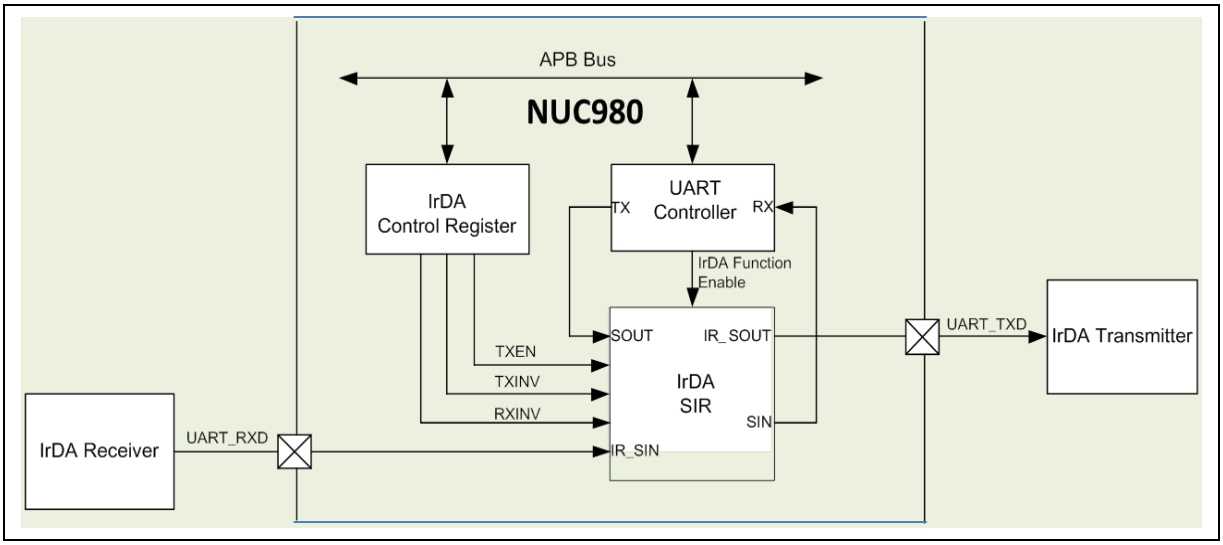


Figure 15.2-2 IrDA Control Block Diagram

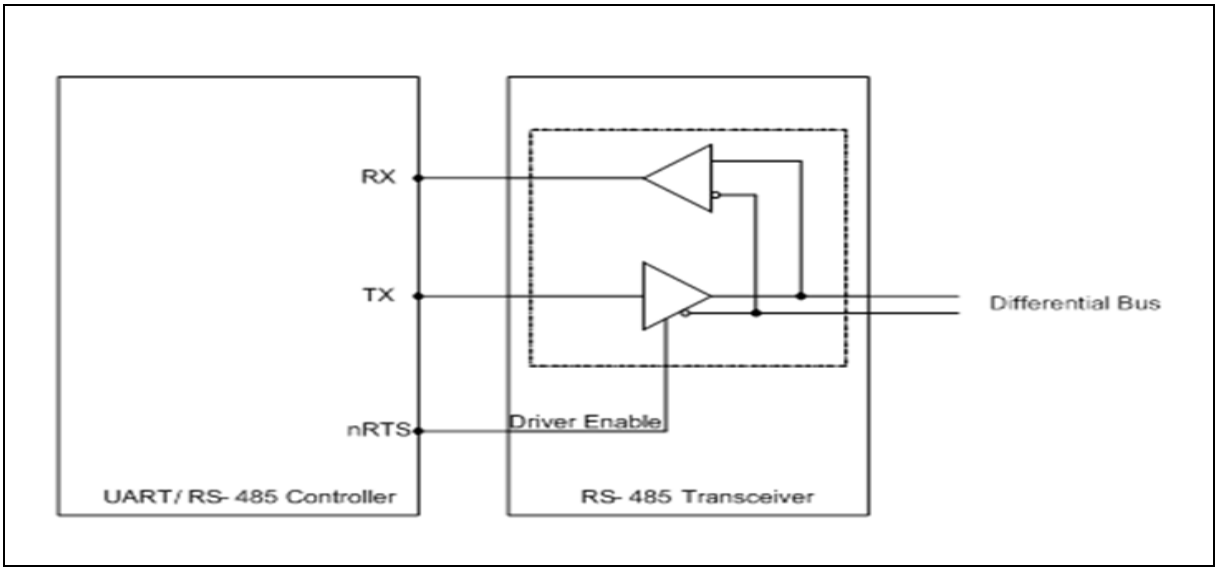


Figure 15.2-3 RS485 mode Block Diagram

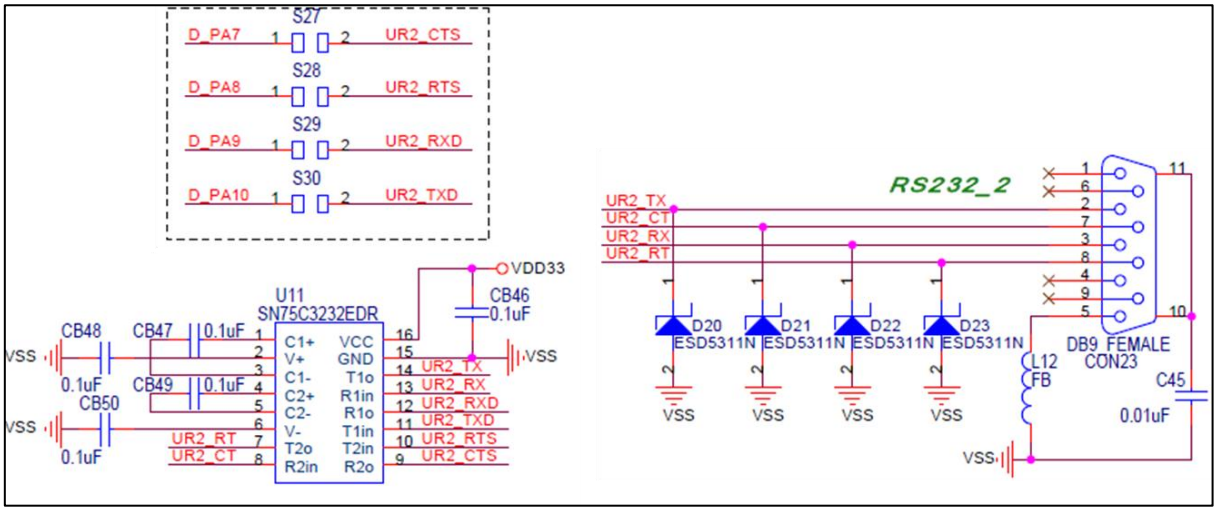


Figure 15.2-4 RS232 connectivity with UART2

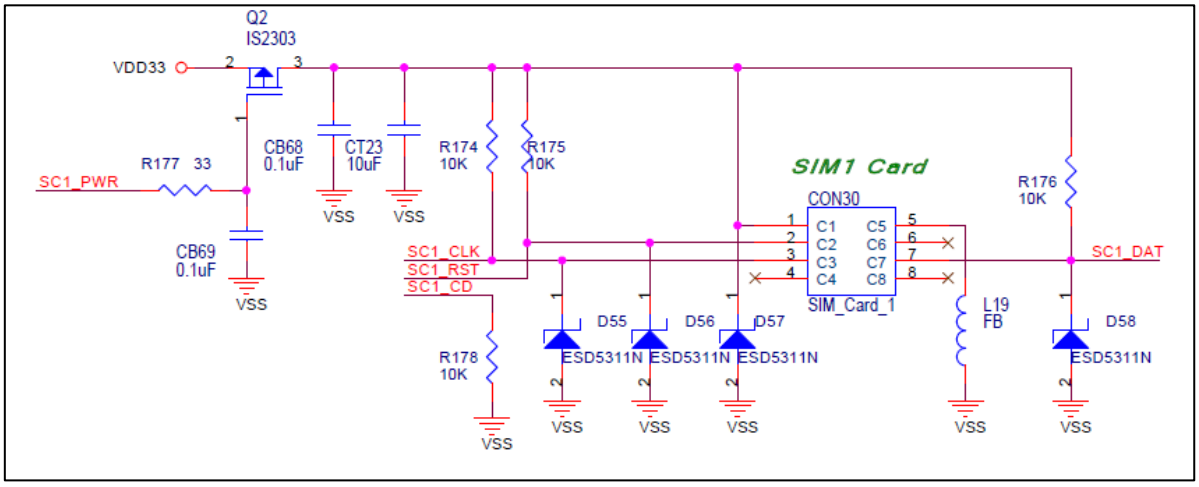
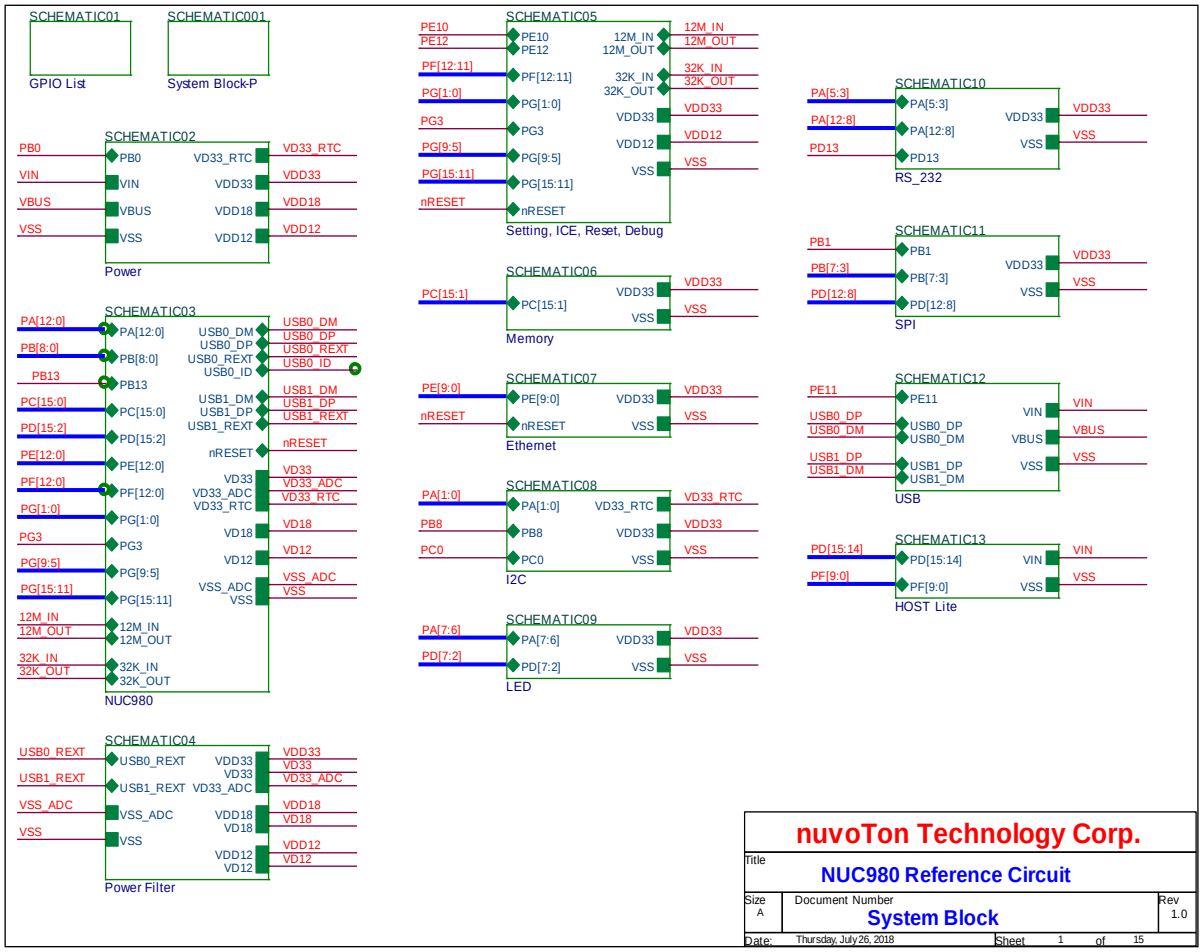


Figure 15.2-5 SMART Card connectivity with SC1

16 Reference Schematic

This section shows the NUC980 reference design circuit.

System Block Diagram



GPIO Pin Assignment List

PIN	FUNCTION
PA0	I2C0_SDA
PA1	I2C0_SCL
PA2	
PA3	UART6_RTS
PA4	UART6_RXD
PA5	UART6_TXD
PA6	LED7
PA7	LED8
PA8	UART2_RTS
PA9	UART2_RXD
PA10	UART2_TXD
PA11	UART8_RXD
PA12	UART8_TXD

PIN	FUNCTION
PB0	ADC_AIN[0]
PB1	Measure IC
PB2	
PB3	Measure IC
PB4	SPI1_CLK
PB5	SPI1_DI
PB6	SPI1_SS0
PB7	SPI1_DO
PB8	I2C2_SCL
PB13	

PIN	FUNCTION
PC0	I2C2_SDA
PC1	NAND_CS0
PC2	NAND_WP
PC3	NAND_ALE
PC4	NAND_CLE
PC5	NAND_WE
PC6	NAND_RE
PC7	NAND_RDY0
PC8	NAND_D0
PC9	NAND_D1
PC10	NAND_D2
PC11	NAND_D3
PC12	NAND_D4
PC13	NAND_D5
PC14	NAND_D6
PC15	NAND_D7

PIN	FUNCTION
PD2	LED1
PD3	LED2
PD4	LED3
PD5	LED4
PD6	LED5
PD7	LED6
PD8	SPI0_SS0
PD9	SPI0_CLK
PD10	SPI0_DO
PD11	SPI0_DI
PD12	ESAM ID
PD13	PWM01
PD14	USBHL0_DM
PD15	USBHL0_DP

PIN	FUNCTION
PE0	RMII0_RXERR
PE1	RMII0_CRSDV
PE2	RMII0_RXD1
PE3	RMII0_RXD0
PE4	RMII0_REFCLK
PE5	RMII0_TXEN
PE6	RMII0_TXD1
PE7	RMII0_TXD0
PE8	RMII0_MDIO
PE9	RMII0_MDC
PE10	Watchdog
PE11	USB0_VBUSVLD
PE12	Watchdog

PIN	FUNCTION
PF0	USBHL1_DM
PF1	USBHL1_DP
PF2	USBHL2_DM
PF3	USBHL2_DP
PF4	USBHL3_DM
PF5	USBHL3_DP
PF6	USBHL4_DM
PF7	USBHL4_DP
PF8	USBHL5_DM
PF9	USBHL5_DP
PF10	
PF11	UART0_RXD
PF12	UART0_TXD

PIN	FUNCTION
PG0	CFG[0]
PG1	CFG[1]
PG3	CFG[3]
PG5	CFG[5]
PG6	CFG[6]
PG7	CFG[7]
PG8	CFG[8]
PG9	CFG[9]
PG11	JTAG0_TDO
PG12	JTAG0_TCK
PG13	JTAG0_TMS
PG14	JTAG0_TDI
PG15	JTAG0_NTRST

FUNCTION:
NAND Flash x1
SPI_0/1 x2
I2C_0/2 x2
RMII_0 x1
ADC_0 x1
UART_2/6/8 x3
UART_0 debug port x1
PWM_01 x1
LED x8
ICE_0 x1
USB_0 Device x1
USB_1 HOST x1
USB_0/1/2/3/4/5 HOST Lite x6
GPIO x12

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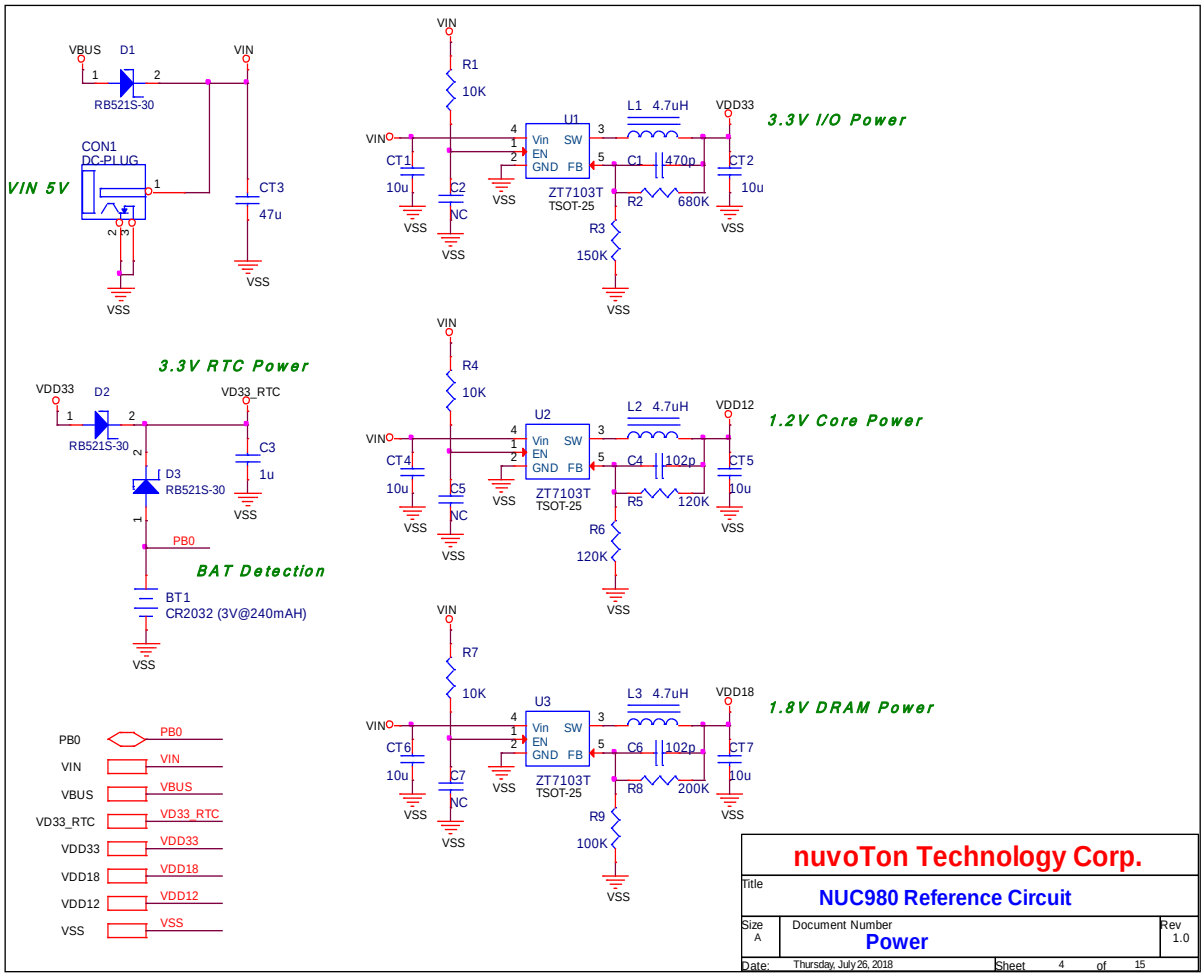
Title: NUC980 Reference Circuit

Size: A | Document Number: GPIO List | Rev: 1.0

Date: Thursday, July 26, 2018 | Sheet 3 of 15

System Power Supply



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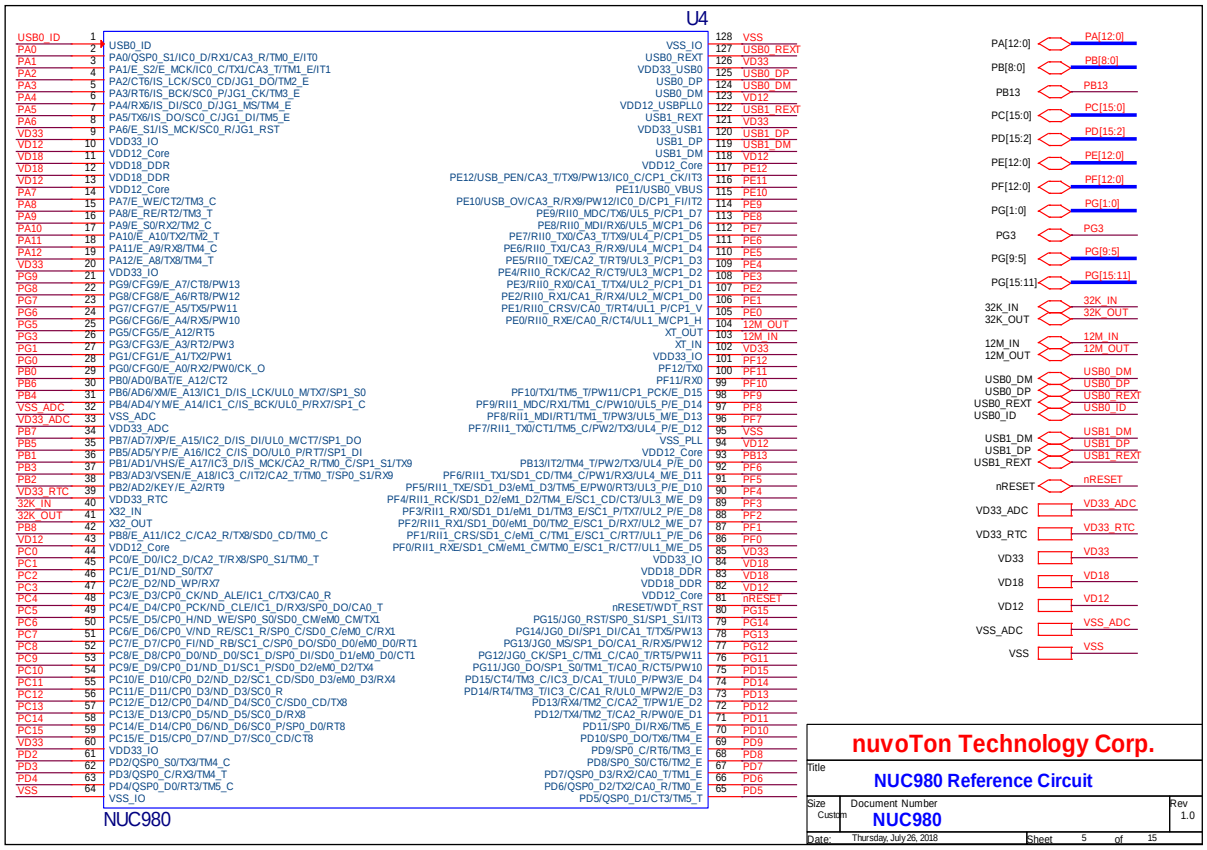
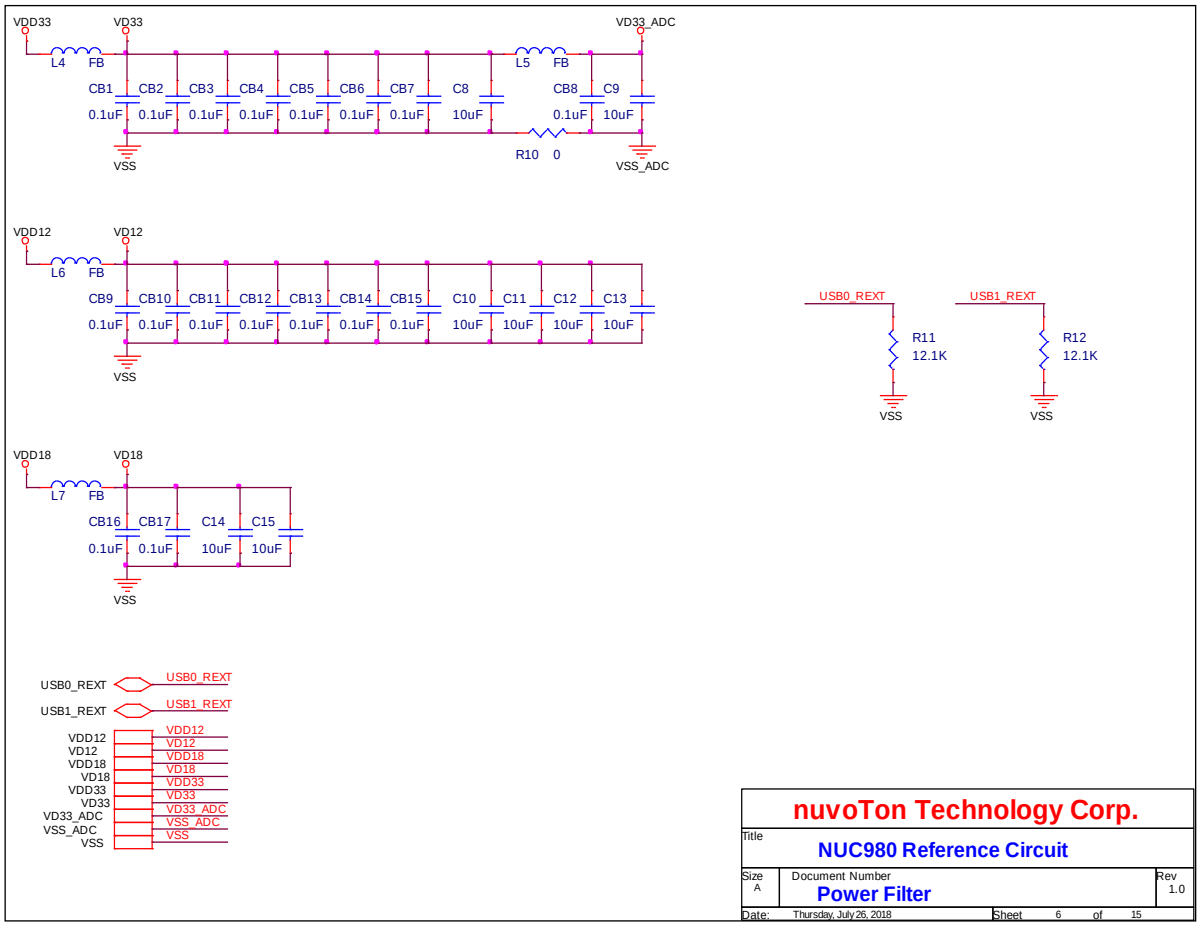
Title	NUC980 Reference Circuit	
Size A	Document Number: Power	Rev 1.0
Date: Thursday, July 26, 2018	Sheet 4 of 15	

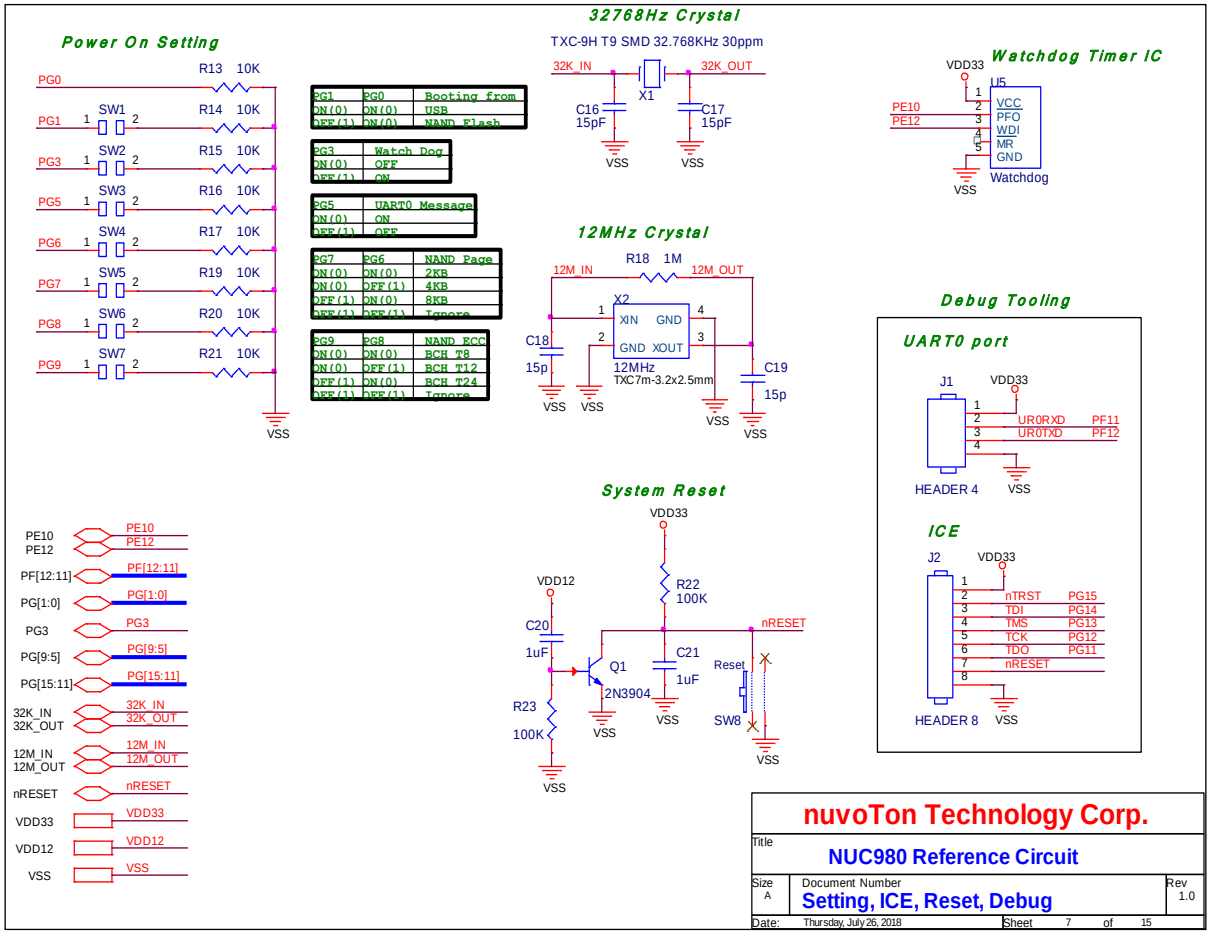
NUC980 Main Chip



Power CAP Filter



RESET, Power-ON Setting, XTAL & Debugging



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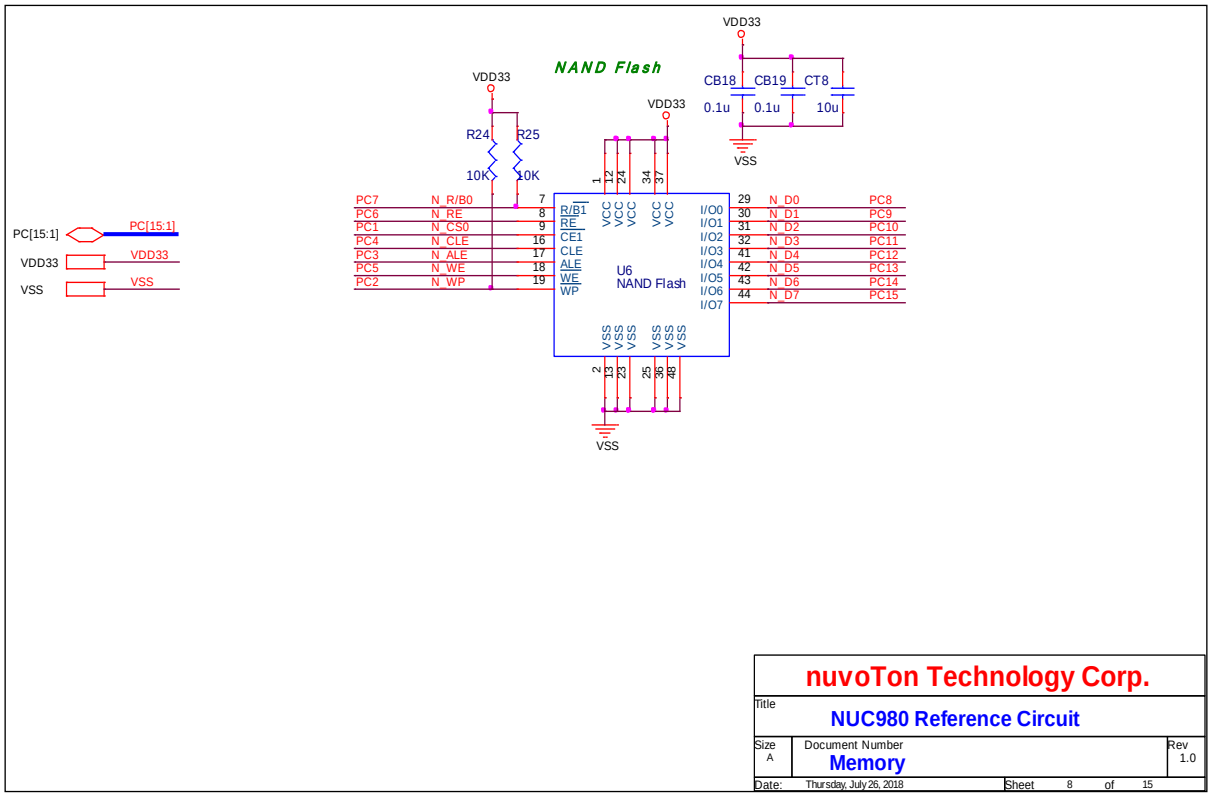
Title	NUC980 Reference Circuit	
Size A	Document Number: Setting, ICE, Reset, Debug	Rev 1.0
Date: Thursday, July 26, 2018	Sheet 7 of 15	

NAND Flash


NAND Flash
VDD33
VSS
R24
R25
10K
10K
CB18
CB19
CT8
0.1u
0.1u
10u
PC[15:1]
PC7
PC6
PC1
PC4
PC3
PC5
PC2
N_R/B0
N_RE
N_CS0
N_CLE
N_ALE
N_WE
N_WP
U6
NAND Flash
R/B1
RE
CE1
CLE
ALE
WE
WP
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
N_D0
N_D1
N_D2
N_D3
N_D4
N_D5
N_D6
N_D7
PC8
PC9
PC10
PC11
PC12
PC13
PC14
PC15
VCC
VSS
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Title
NUC980 Reference Circuit
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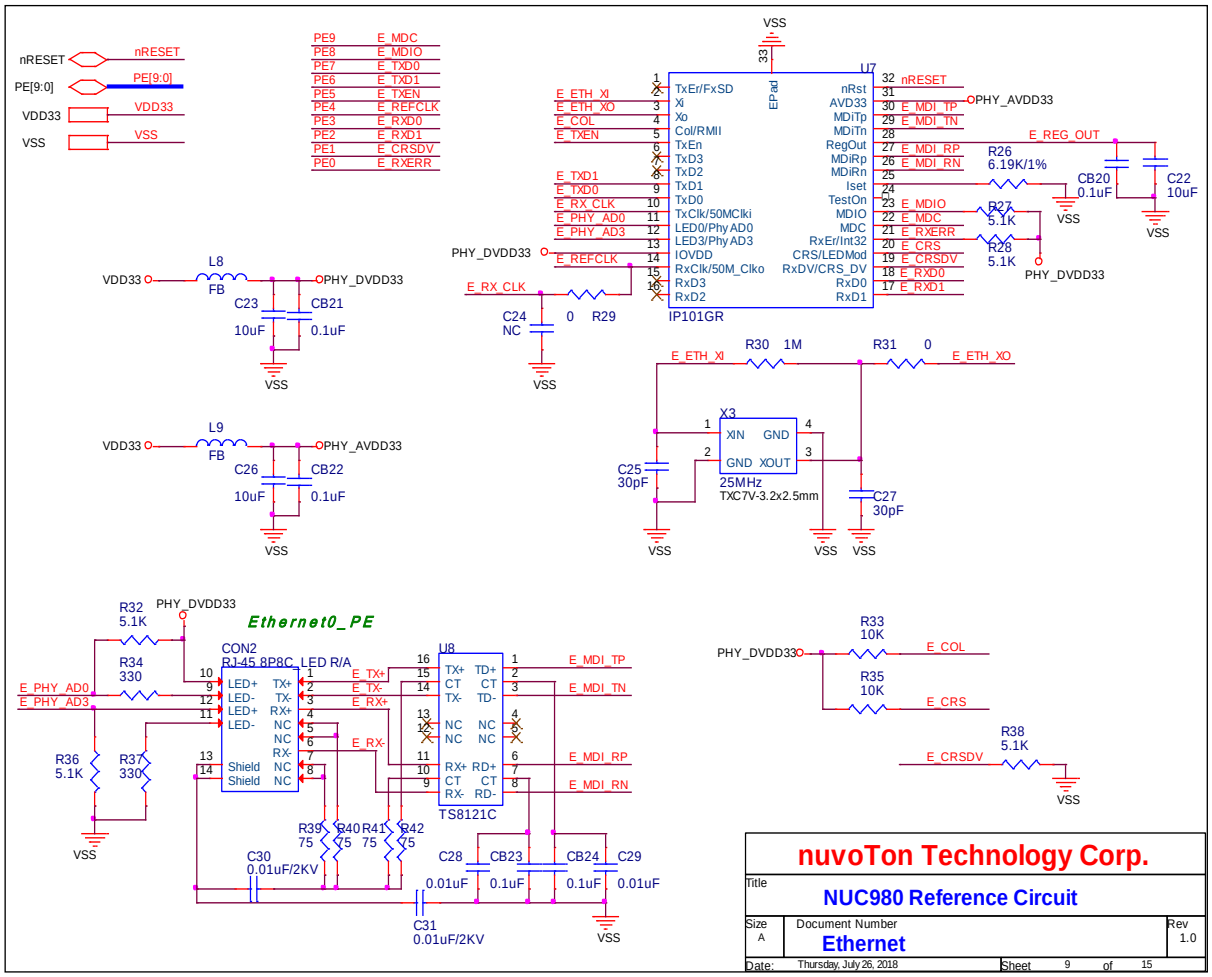
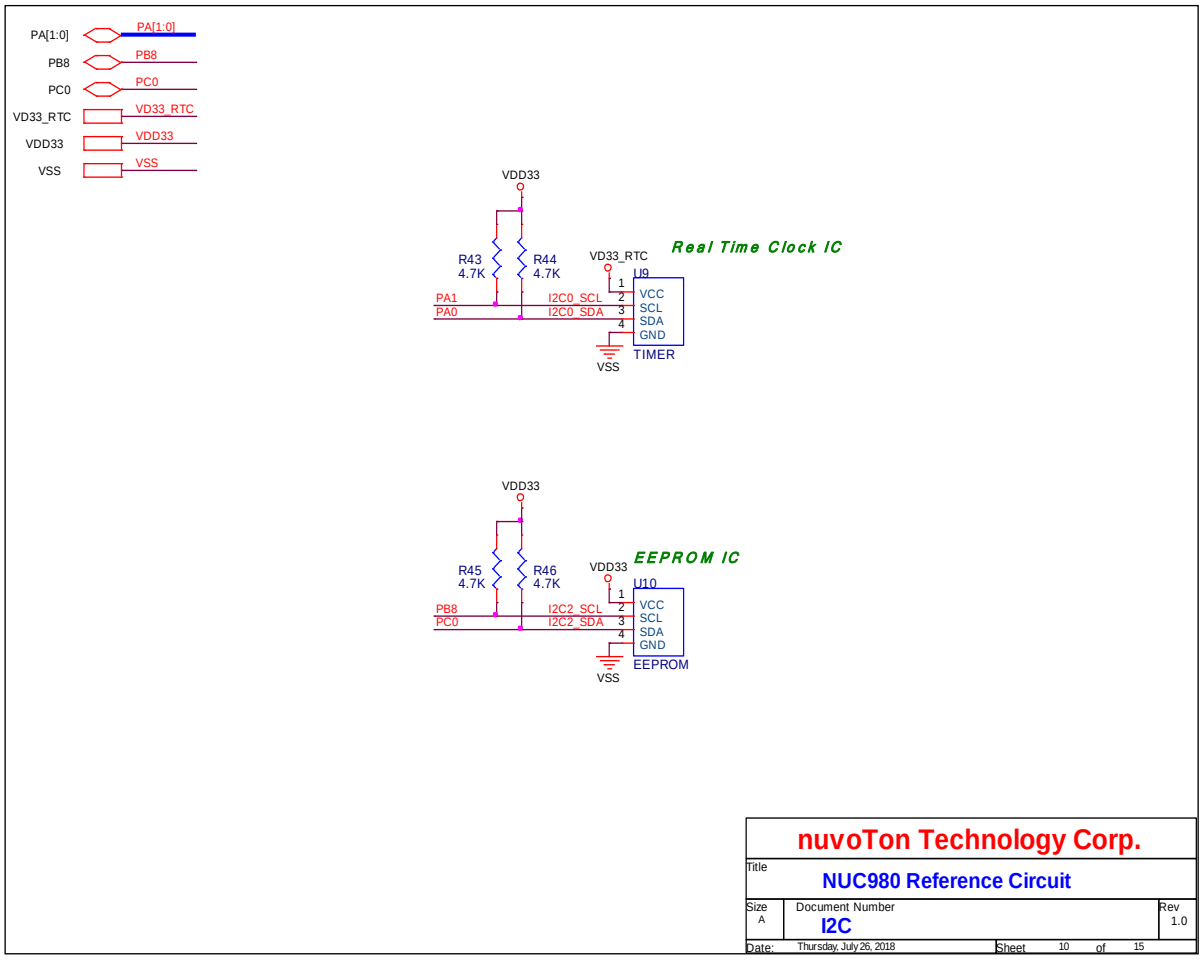
Memory
Rev
1.0
Date:
Thursday, July 26, 2018
Sheet
8
of
15

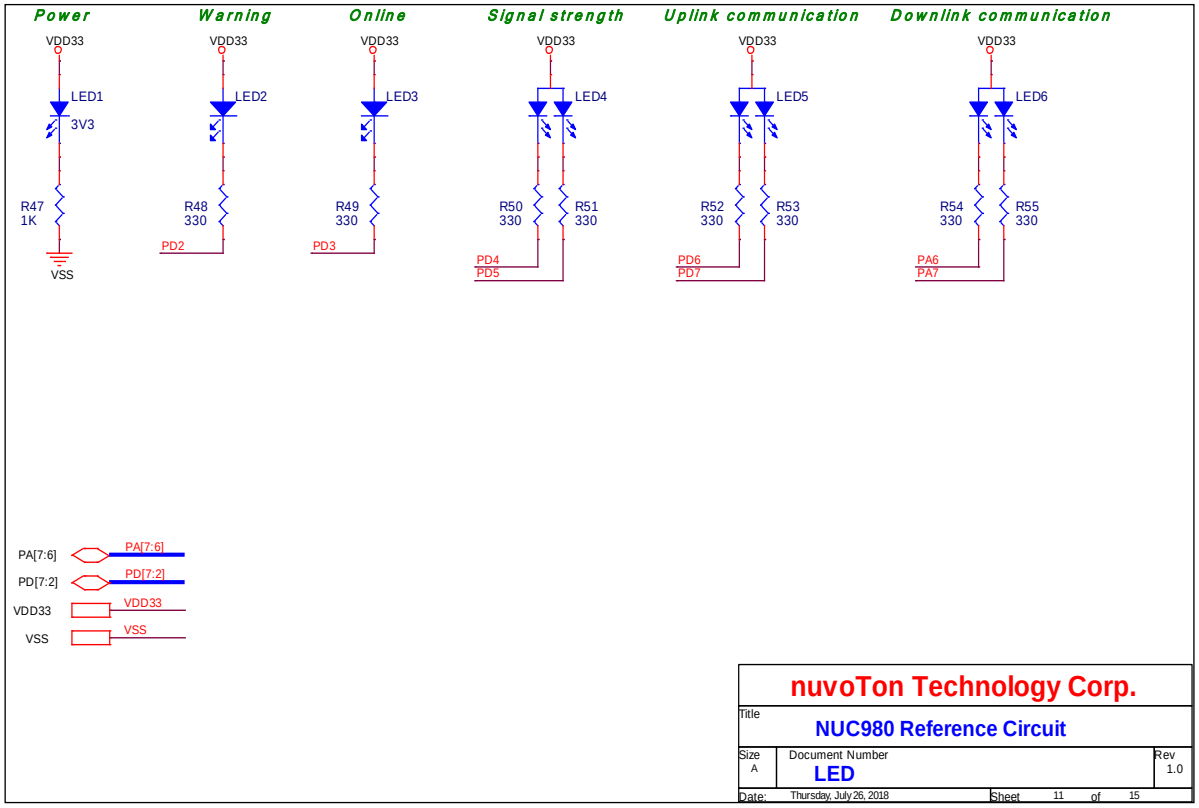
Ethernet RMII PHY + RJ45



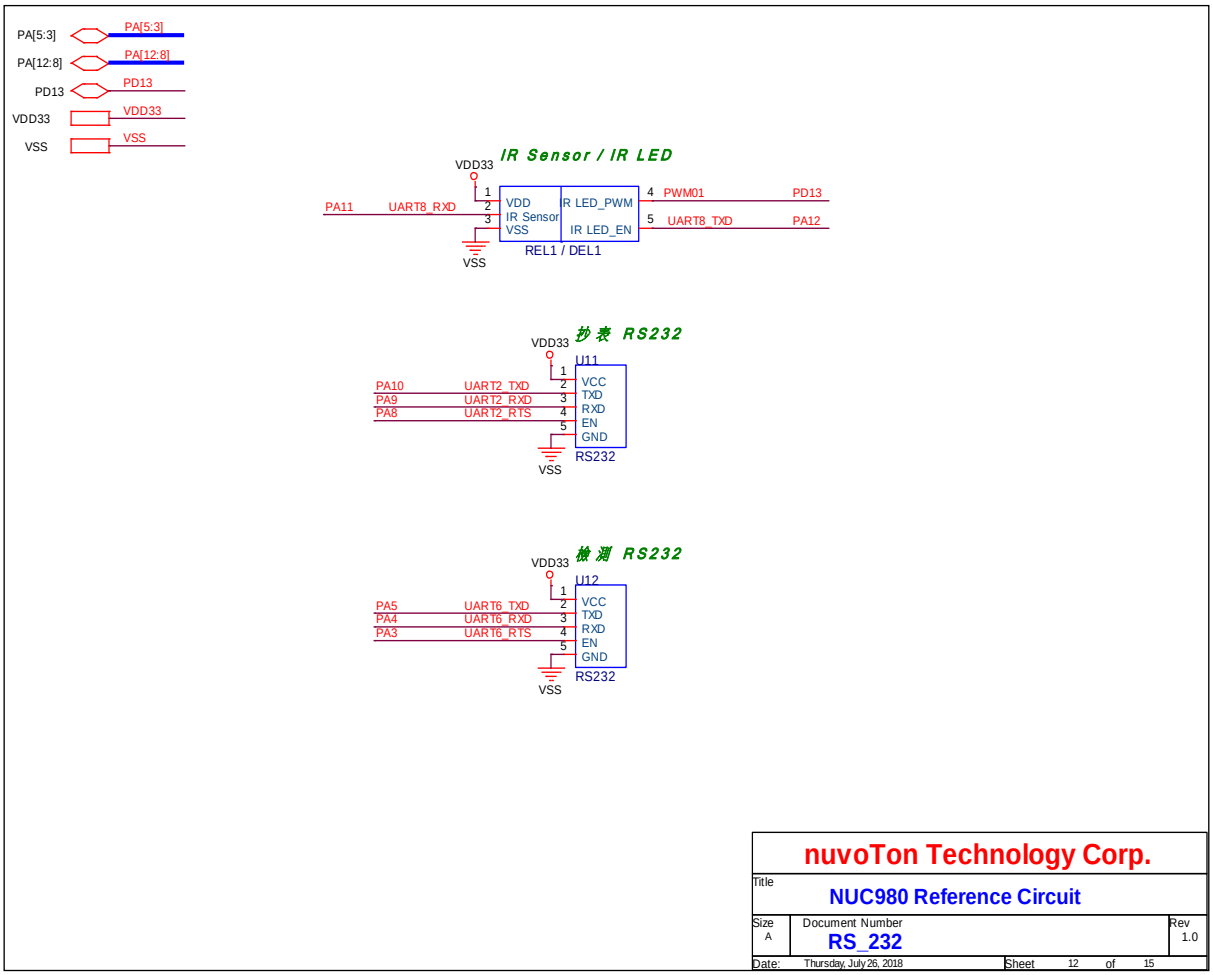
I²C Interface



LED indication



UART Interface



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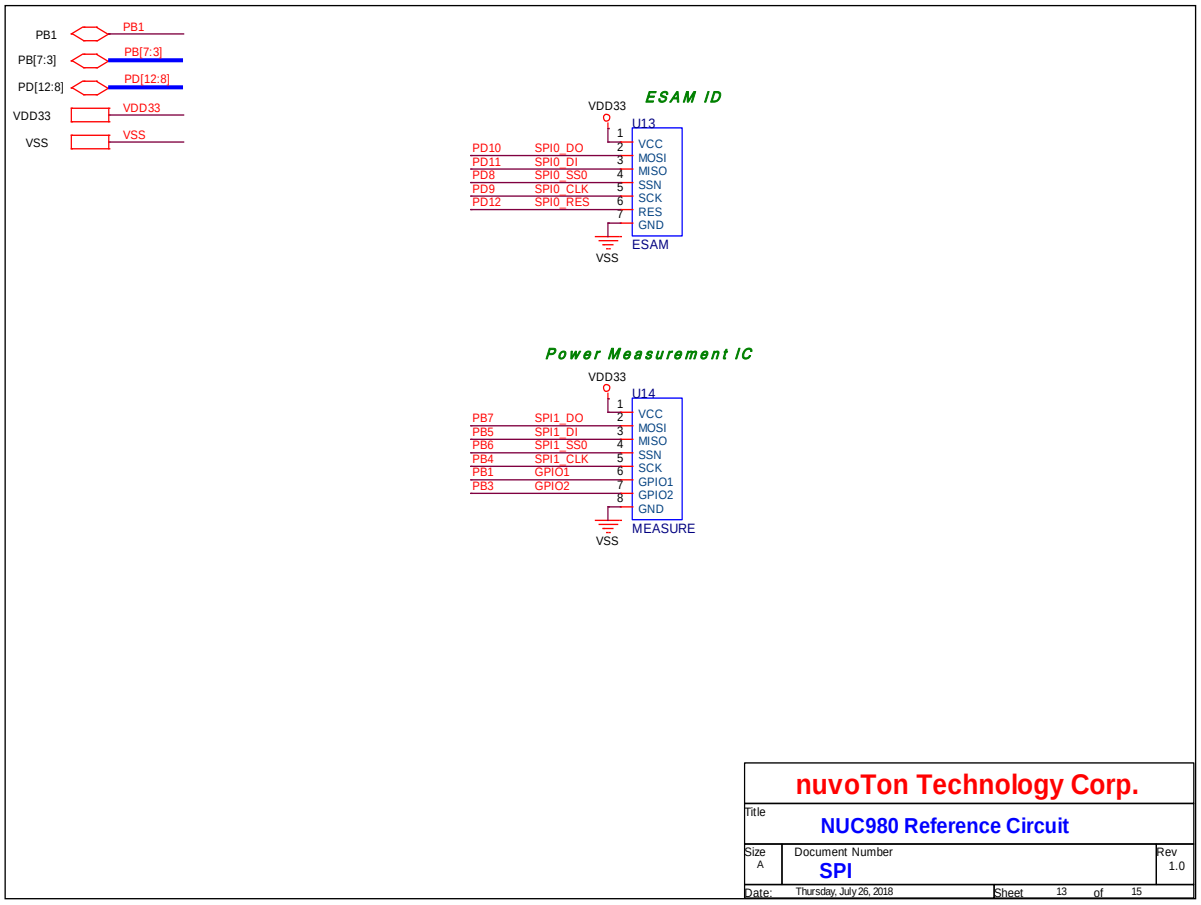
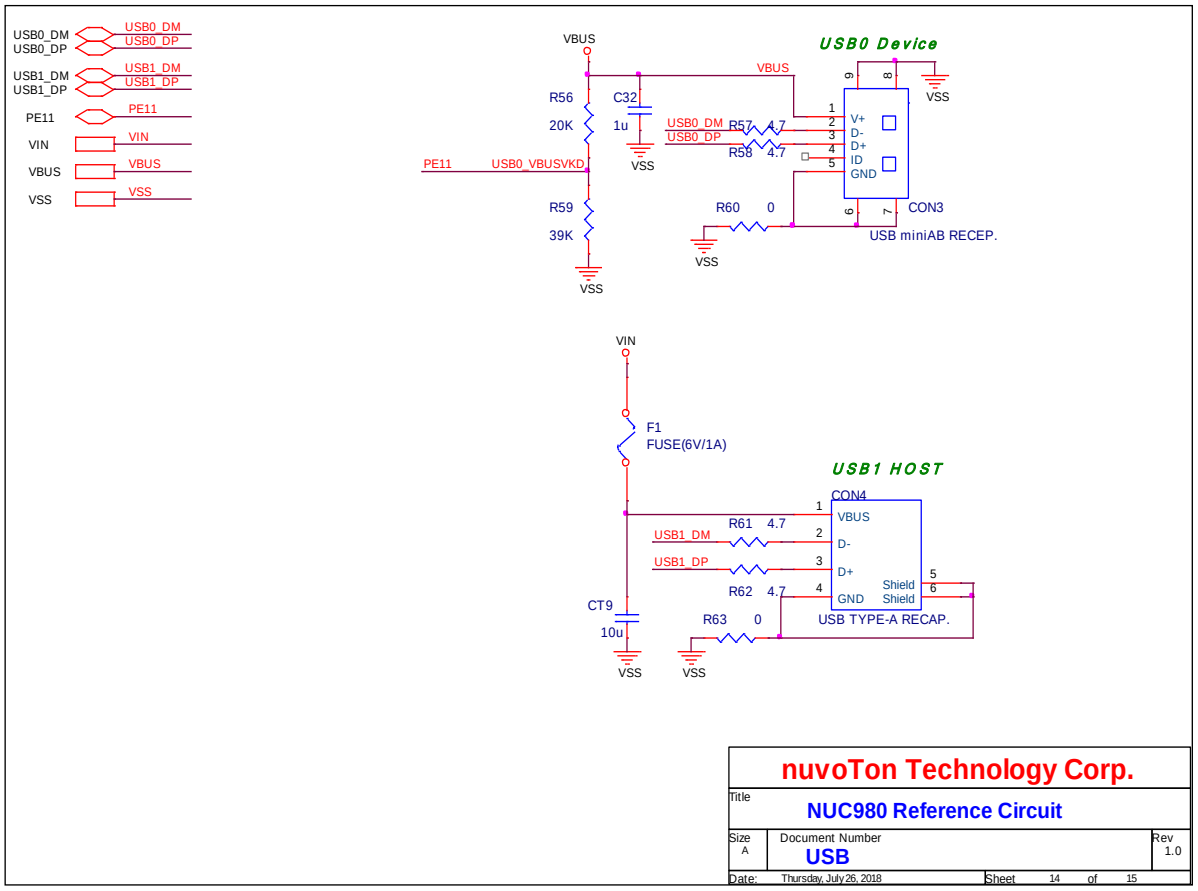
Title: NUC980 Reference Circuit		
Size: A	Document Number: RS_232	Rev: 1.0
Date: Thursday, July 26, 2018	Sheet 12 of 15	

SPI Interface



USB HS HOST & Device



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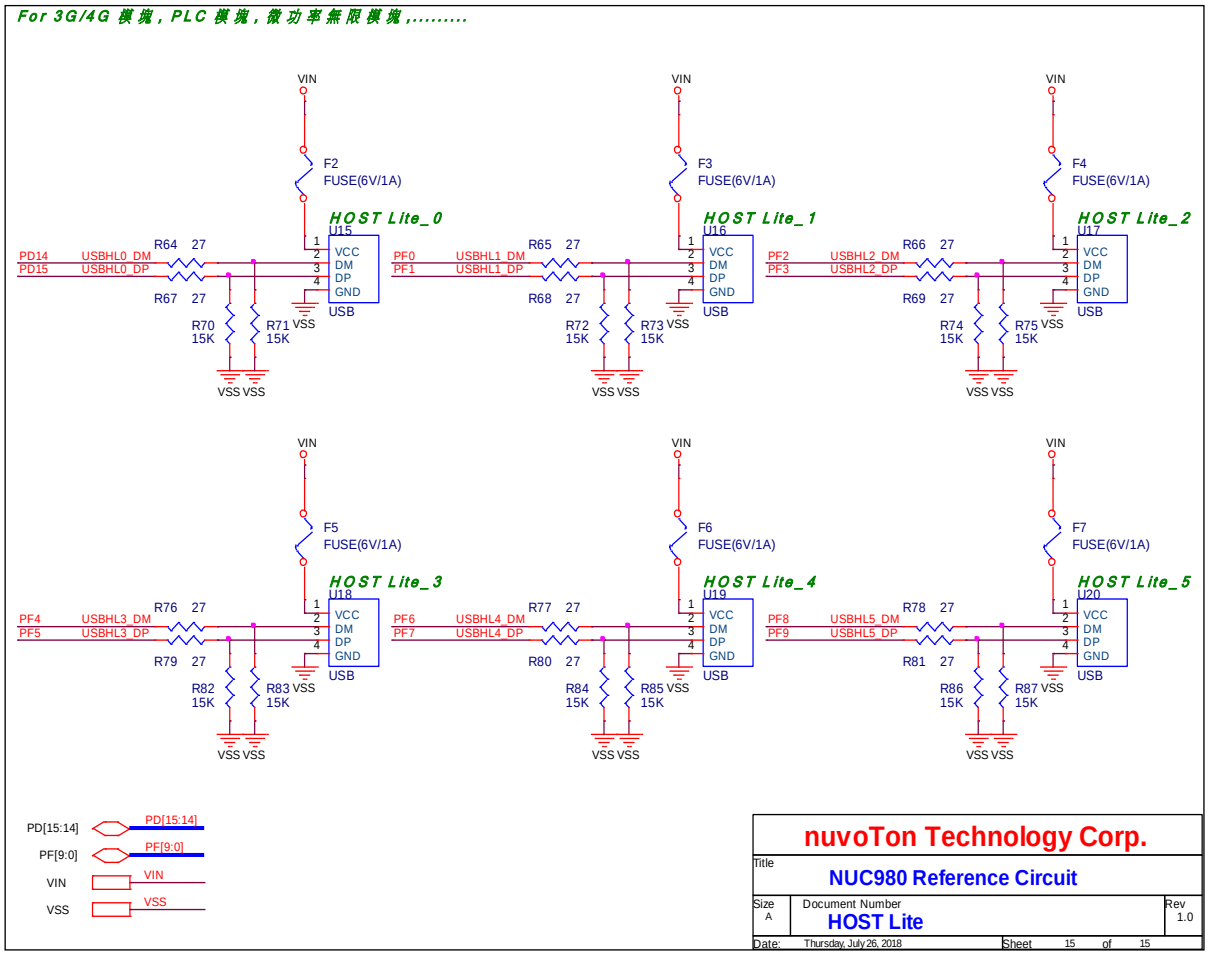
Title: NUC980 Reference Circuit		
Size: A	Document Number: USB	Rev: 1.0
Date: Thursday, July 26, 2018	Sheet 14 of 15	

USB1.1 FS HOST lite



Revision History

Date	Revision	Description
2018.12.12	1.00	1. Initially issued.

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