

NAU8331 Datasheet

Revision 3.2

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1 GENERAL DESCRIPTION

1.1 Overview

The NAU8331 is a Class-D monophonic boost amplifier device with V/I-Sense such that it can work with external speaker excursion control algorithms, which may be running on a separate Digital Signal Processor (DSP) or inside a main processor. Compared to traditional Class-D amplifiers, the NAU8331 has two Analog-to-Digital Converters (ADCs) integrated into the chip. The two ADCs support a stereo interface and enable speaker voltage and current to be sensed and sent back to the main processor or DSP for speaker excursion control. This speaker excursion control along with boost amplifier technology can prevent the speaker membrane excursion from exceeding its rated limit and also provides ample headroom for overall loudness and sound quality.

Target applications for this device include mobile devices such as smartphones, personal media players, notebook and tablet computers, and laptops, where small speakers are essential. Other applications well served by the NAU8331 include: portable televisions, MP3 players, portable game players and digital camcorders, as well as other computer types.

1.2 Features

The NAU8331 Boosted Amplifier with I/V Sense is a powerful Class-D Amplifier with a high-efficiency Class-G Boost Converter. The chip features high output power capability, low-output noise in Receiver Mode, low-current shutdown mode, and click-and-pop suppression. Numerous types of device protection schemes are supported, as well as speaker protection schemes, including ambient temperature monitoring input for enhanced speaker module design. The temperature monitoring in the NAU8331 protects both the chip and the speaker from overheating. A stereo digital microphone interface is also provided for ease of product design. The chip is available in a 35-ball Wafer Level Chip Scale Package (WLCSP).

Key Feature List

- Powerful Class-D Amplifier:
 - Up to 6 Watts into an 8 Ohm load at 10% Total Harmonic Distortion and Noise (THD+N)
 - Up to 8 Watts into an 4 Ohm load at 10% Total Harmonic Distortion and Noise (THD+N)
- High Efficiency Class-G Boost Converter
- Low Output Noise in Receiver Mode: 18 μ VRMS
- ≥ 90 dB Power Supply Rejection Ratio (PSRR)
- Low Current Shutdown Mode
- Click-and-Pop Suppression (30 μ VRMS)
- Programmable Serial Interfaces:
 - I2C Interface
 - I2S Interface
 - PCM Interface
 - Stereo Digital Microphone Interface
- Device Protection:
 - Over Current Protection (OCP),
 - Over Voltage Protection (OVP)
 - Under Voltage Lock Out (UVLO)
 - Over Temperature Protection (OTP)
 - Clock Termination Protection (CTP)
- Speaker Protection:
 - Current & Voltage Sensing
 - Anti-Clip Protection (ACP)
 - Speaker Module Temperature Sense Input
- Battery Protection: Limiter
- Filter-less Electro Magnetic Interference (EMI) mitigation
- 35-Ball Wafer Level Chip Scale Package (WLCSP) (0.5 mm Pitch)

Applications

- Smartphones
- Notebooks /Tablets/ Personal Computers
- Personal Media Players/Portable Televisions
- MP3 Lossless Standard Audio Compression Format Players
- Portable Game Players
- Digital Camcorders

2 PIN CONFIGURATIONS

2.1 Pin Diagrams

The NAU8331 Boosted Monophonic Class-D Amplifier with I/V-Sense is available in a 35-Ball WLCSP package as shown in **Figure 1**.

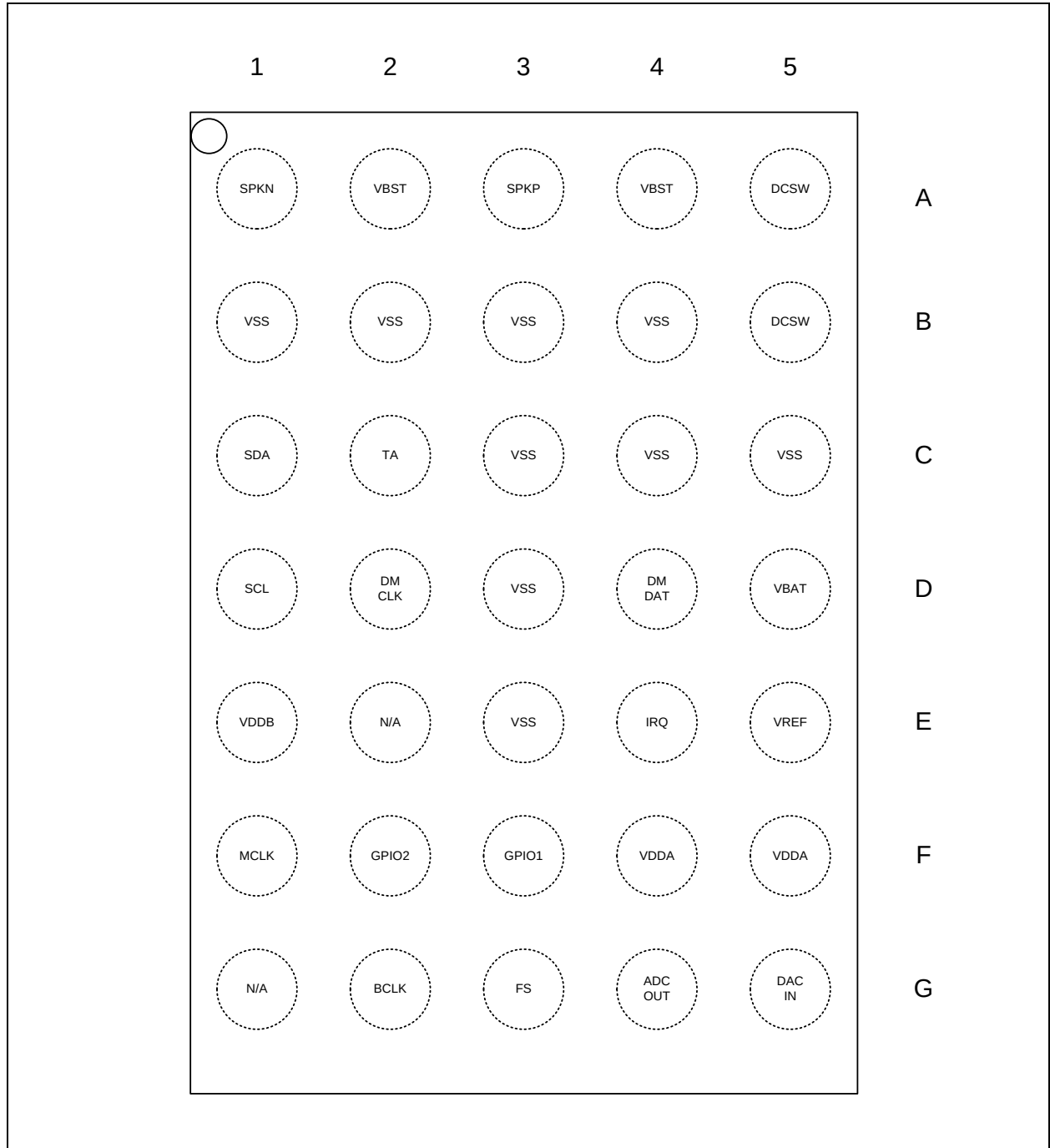


Figure 1 Pin Diagram of NAU8331 (Top Down View)

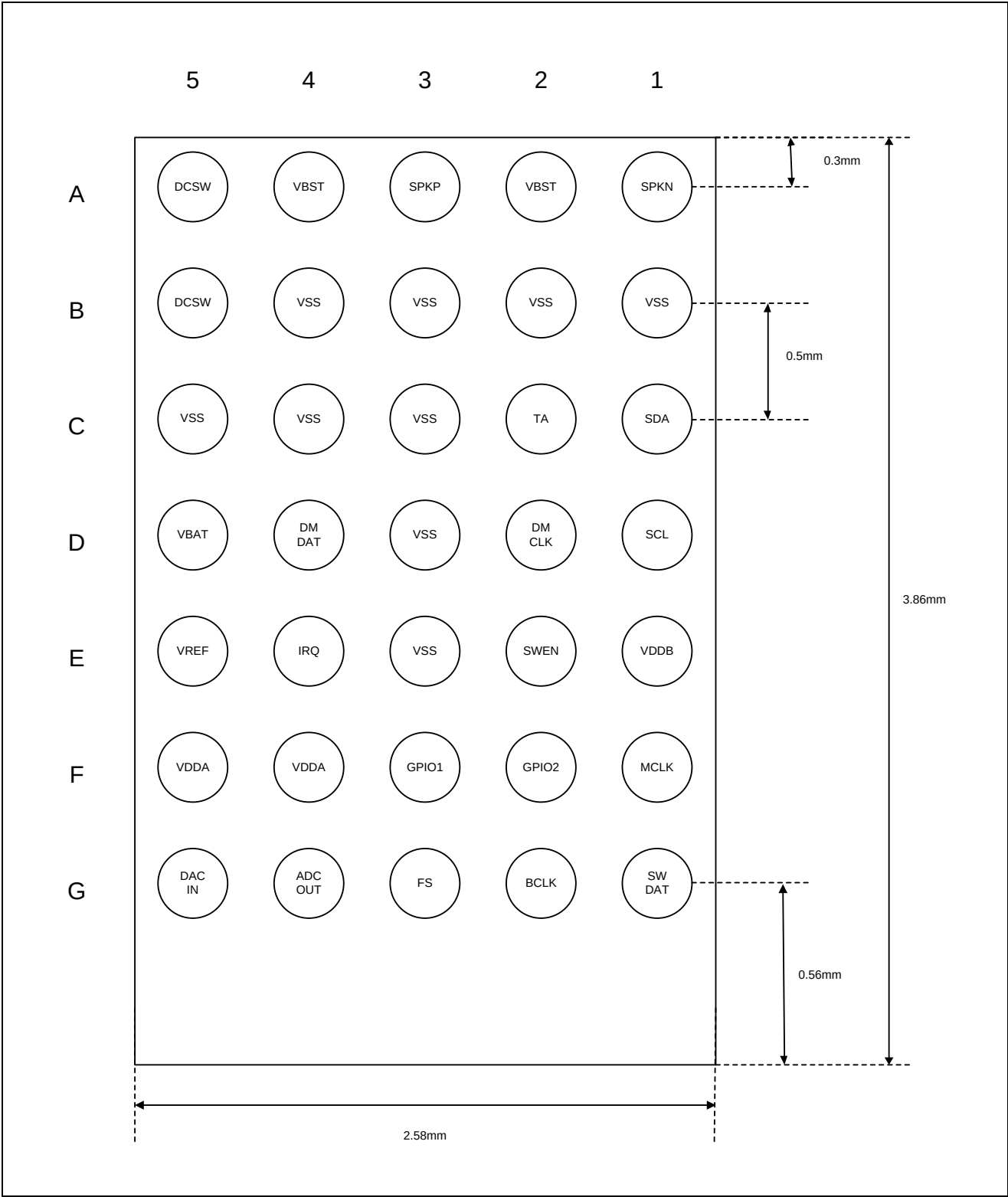


Figure 2 Pin Diagram of NAU8331 (Bottom Up View)

2.2 PIN DESCRIPTIONS

Pin descriptions for the NAU8331 Boosted Mono Class-D Amplifier with I/V Sense are provided in **Table 1**.

Table 1 Pin Descriptions for the NAU8331

Pin #	Name	Type, (Supply Domain)	Description
A1	SPKN	Analog Output, (VBAT)	Class-D Negative Speaker Output Terminal; Current Sense Input
A2	VBST	Analog I/O, (VBAT)	DC-DC Boost Converter Output
A3	SPKP	Analog Output, (VBAT)	Class-D Positive Speaker Output Terminal; Current Sense Input
A4	VBST	Analog I/O, (VBAT)	DC-DC Boost Converter Output
A5	DCSW	Analog I/O, (VBAT)	DC-DC Boost Converter Switch
B1	VSS	Ground	Supply Ground
B2	VSS	Ground	Supply Ground
B3	VSS	Ground	Supply Ground
B4	VSS	Ground	Supply Ground
B5	DCSW	Analog I/O, (VBAT)	DC-DC Boost Converter Switch
C1	SDA	Digital I/O, (VDDDB)	Serial Data for I2C
C2	TA	Analog Input, (VDDA)	Ambient Temperature Sense Input, tie to VSS if not used
C3	VSS	Ground	Supply Ground
C4	VSS	Ground	Supply Ground
C5	VSS	Ground	Supply Ground
D1	SCLK	Digital Input, (VDDDB)	Serial Data Clock for I2C
D2	DMCLK	Digital Output, (VDDA)	Serial Data Clock for Digital Microphone
D3	VSS	Ground	Supply Ground
D4	DMDAT	Digital Input, (VDDA)	Serial Data Input from Digital Microphones
D5	VBAT	Supply	Battery Supply Voltage
E1	VDDDB	Supply	Digital IO Supply
E2	N/A		
E3	VSS	Ground	Supply Ground
E4	IRQ	Digital Output, (VDDDB)	Programmable Interrupt Output
E5	VREF	Analog I/O, (VDDA)	Internal DAC & ADC Voltage Reference Decoupling I/O
F1	MCLK	Digital Input, (VDDDB)	Master Clock
F2	GPIO2	Digital I/O, (VDDDB)	General Purpose IO2/Address Selection 2
F3	GPIO1	Digital I/O, (VDDDB)	General Purpose IO1/Address Selection 1
F4	VDDA	Supply	1.8 V Analog & Digital Core Supply. F4 and F5 are tied together.
F5	VDDA	Supply	
G1	N/A		

Pin #	Name	Type, (Supply Domain)	Description
G2	BCLK	Digital I/O, (VDDDB)	Serial Audio Data Bit Clock I2S/PCM Input
G3	FS	Digital I/O, (VDDDB)	Frame Sync I2S/PCM Input
G4	ADCOUT	Digital Output, (VDDDB)	Serial Audio I2S/PCM Data Output
G5	DACIN	Digital Input, (VDDDB)	Serial Audio Data I2S/PCM Input

3 BLOCK DIAGRAM

A Block Diagram for the NAU8331 is provided in **Figure 3**.

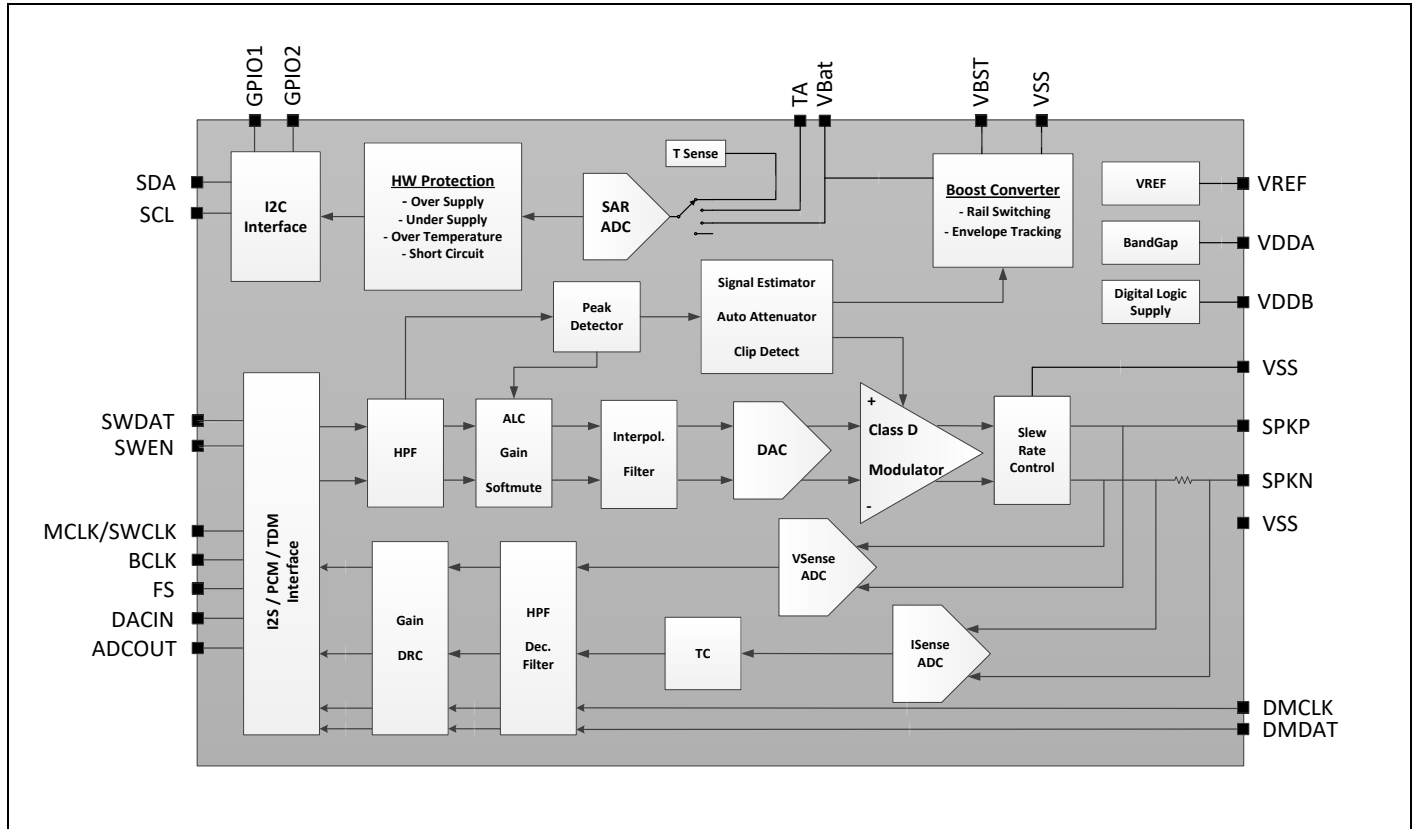


Figure 3 NAU8331 Block Diagram

4 ELECTRICAL CHARACTERISTICS

The tables in this chapter provide the various electrical parameters for the NAU8331 and their values.

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Min	Max	Units
VDDDB Digital I/O Supply Range	-0.3	4.0	V
VBAT Battery Supply Range	-0.3	6.0	V
VDDA Analog Supply Range	-0.3	2.2	V
Voltage Input Analog Range	VSS - 0.3	VDDA + 0.3	V
Voltage Input I/O Range	VSS - 0.3	VDDDB + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

4.2 Operating Conditions

Table 3 Recommended Operating Conditions for the NAU8331

Condition	Symbol	Min	Typical	Max	Units
Battery Supply Range	VBAT	2.90	4.2	5.50	V
Analog Supply Range	VDDA	1.62	1.8	1.98	V
Digital I/O Supply Range	VDDDB	1.62	3.0	3.6	V
Ground	VSS		0		V
Industrial Operating Temperature		-40		+85	°C

CAUTION: The following conditions needed to be followed for regular operation: $V_{BAT} > V_{DDA} - 1.2V$; $V_{DDDB} > V_{DDA} - 0.6V$.

4.3 Electrical Parameters

Table 4 Electrical Characteristics

Conditions: $V_{DDA} = V_{ddb} = 1.8V$; $V_{BAT} = 4.2V$. $R_L = 8\ \Omega + 33\ \mu H$, $f = 1kHz$, 48kHz sample rate, MCLK=12.88MHz, Boost Inductor = $1\ \mu H$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Typical	Limit	Units
ISD	Shutdown Supply Current	V _{DDA} , all clocks off	2.0	10	μA
		V _{ddb} , all clocks off	0.3	2	
		V _{BAT} , all clocks off	0.4	4	
ISB	Standby Mode Supply Current	V _{DDA} , MCLK off, clock gating on	2.0		μA
		V _{ddb} , MCLK off, clock gating on	0.3		μA
		V _{BAT} , MCLK off, clock gating on	0.4		μA
IDD	Operating Mode Supply Current	V _{DDA} , idle Channel	10		mA
		V _{ddb} , idle Channel	0.2		mA
		V _{BAT} , idle Channel	3		mA
Class-D Channel					
P _o	Output Power	RL = 8 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 1%	5.5		W
		RL = 8 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 10%	6		W
		RL = 4 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 1%	6.5		W
		RL = 4 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 10%	8		W
THD+N	Total Harmonic Distortion + Noise	R _L = 8 Ω + 33 μH, f=1kHz, P _O = 2 W	0.017		%
e _{os}	Output Noise	A-Weighted, 20Hz-20kHz, Receiver mode or Auto attenuate, no DAC input signal, gain = 0dB	18		μVrms
		A-Weighted, 20Hz-20kHz, no DAC input signal, gain = 16.8dB	50		μVrms
PSRR	Power Supply Rejection Ratio	DC, V _{BAT} = 2.9V – 5.5V, GAIN = 16.8dB	92		dB
		f _{ripple} = 217Hz, V _{ripple} = 200mV _{P-P} GAIN = 16.8dB	92		dB

Symbol	Parameter	Conditions	Typical	Limit	Units
		$f_{\text{RIPPLE}} = 1020\text{Hz}$, $V_{\text{RIPPLE}} = 200\text{mV}_{\text{P-P}}$ GAIN = 16.8dB	92		dB
		$f_{\text{RIPPLE}} = 4\text{kHz}$, $V_{\text{RIPPLE}} = 200\text{mV}_{\text{P-P}}$ GAIN = 16.8dB	88		dB
Fres	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, $R_L = 8\ \Omega + 33\ \mu\text{H}$	+0.8/-0.1		dB
Vos	Output Offset Voltage	Idle Channel, Gain= 0dB	± 1	± 5	mV
Kpop	Pop and Click Noise	A-weighted, Idle DAC input, Clock Gating, toggling clocks on/off	0.03		mVrms
		A-weighted, Idle DAC input, toggling between -120dBfs DAC In & 2048 zero samples	0.03		mVrms
Rdson-P	Driver P MOS-FET ON-resistance	$V_{\text{BAT}} = 5.0\text{V}$, $R_L = 8\ \Omega + 33\ \mu\text{H}$, DC Output Clipping	0.112		Ohm
Rdson-N	Driver N MOS-FET ON-resistance	$V_{\text{BAT}} = 5.0\text{V}$, $R_L = 8\ \Omega + 33\ \mu\text{H}$, DC Output Clipping	0.116		Ohm
Fsw	Switching Frequency	Average	300		kHz
Voltage Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise	$V_{\text{BAT}} = 5.5\text{V}$, +10dBVrms, Class-D off	0.004		%
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	101		dB
FS _{ADC}	ADC Full Scale Input Level		14.4		V _{PK}
Current Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise	$V_{\text{BAT}} = 5.5$ with 80hm + 33uH, $P_o = 3\text{W}$	0.37		%
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	69		dB
FS _{ADC}	ADC Full Scale Input Level		4.04		A _{PK}
Battery Sense ADC					
INL	Integrated Non-Linearity	$V_{\text{BAT}} = 2.9\text{V}-5.5\text{V}$ (gain & offset compensated)	+/-1		LSB
DNL	Differential Non-Linearity	$V_{\text{BAT}} = 2.9\text{V}-5.5\text{V}$	+/-1		LSB
Boost Converter					
Fsw	Switching Frequency		2.0		MHz
Vbstmax	Boost Converter Maximum Output Voltage		10.98		V
Vbstmin	Boost Converter Minimum Output Voltage		2.9		V

Symbol	Parameter	Conditions	Typical	Limit	Units
Vbststp	Boost Converter Step Voltage		0.16		V
Vovp	Boost Converter Overvoltage Protection Threshold		12.7		V
Rdson-P	Boost Converter P MOS-FET ON-resistance		0.1		Ohm
Rdson-N	Boost Converter N MOS-FET ON- resistance		0.1		Ohm
Boost Converter + Class-D					
Neff	Power Efficiency	Output Power = 0.45 W, VBAT= 5.0 V	75		%
		Output Power = 1.0 W, VBAT = 5.0 V	78		%
		Output Power = 6.0 W, VBAT = 5.0 V	80		%

4.4 Digital I/O Parameters

Table 5 Digital I/O Characteristics

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V _{IL}	V _{DD} B = 1.8V			0.33*V _{DD} B	V
		V _{DD} B = 3.3V			0.37*V _{DD} B	
Input HIGH level	V _{IH}	V _{DD} B = 1.8V		0.67*V _{DD} B		V
		V _{DD} B = 3.3V		0.63*V _{DD} B		
Output HIGH level	V _{OH}	I _{Load} = 1mA	V _{DD} B=1.8V	0.9*V _{DD} B		V
			V _{DD} B = 3.3V	0.95*V _{DD} B		
Output LOW level	V _{OL}	I _{Load} = 1mA	V _{DD} B = 1.8V		0.1*V _{DD} B	V
			V _{DD} B=3.3V		0.05*V _{DD} B	

4.5 THD+N Plots

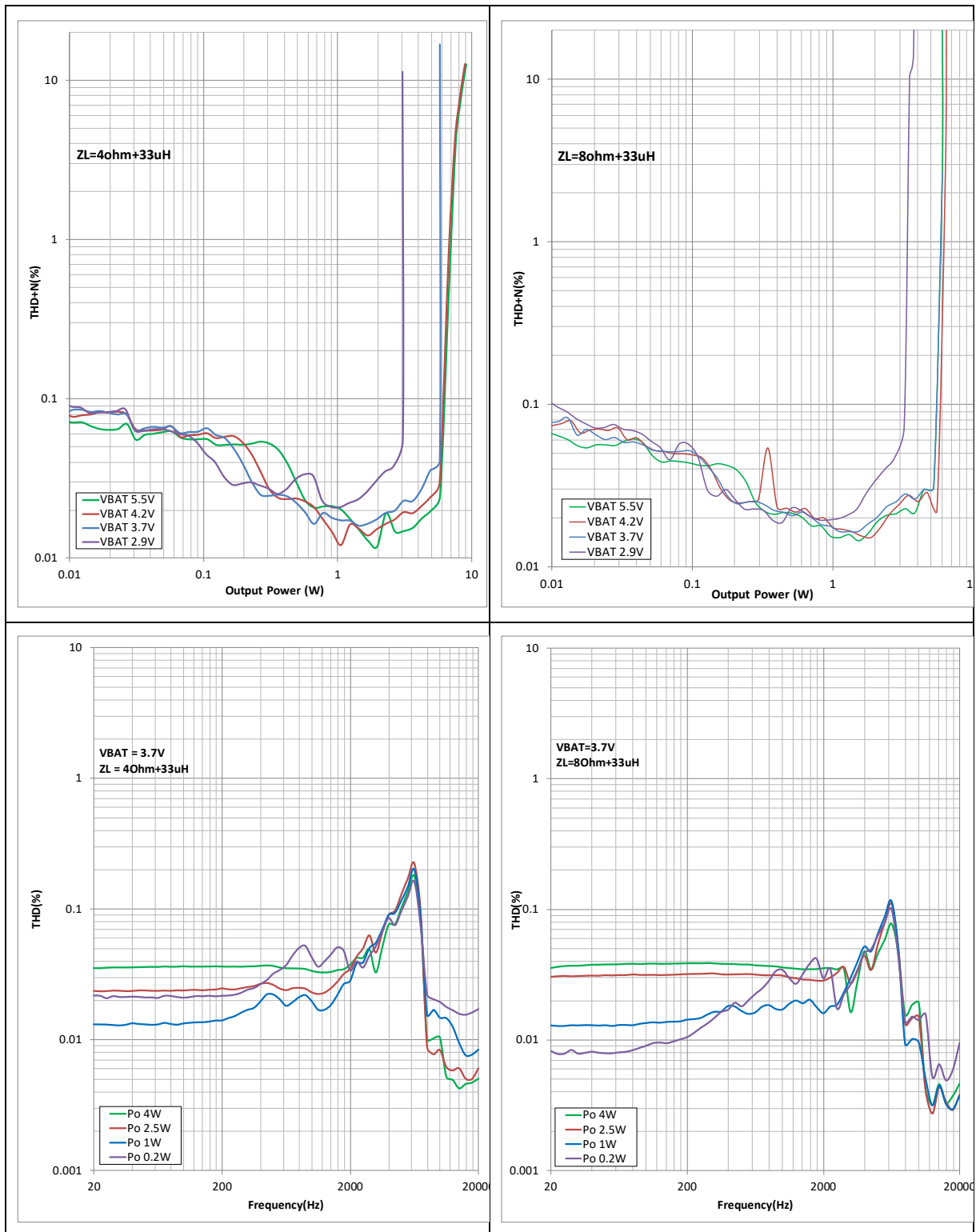


Figure 4 NAU8331 THDN Plots

4.6 PSRR Plots

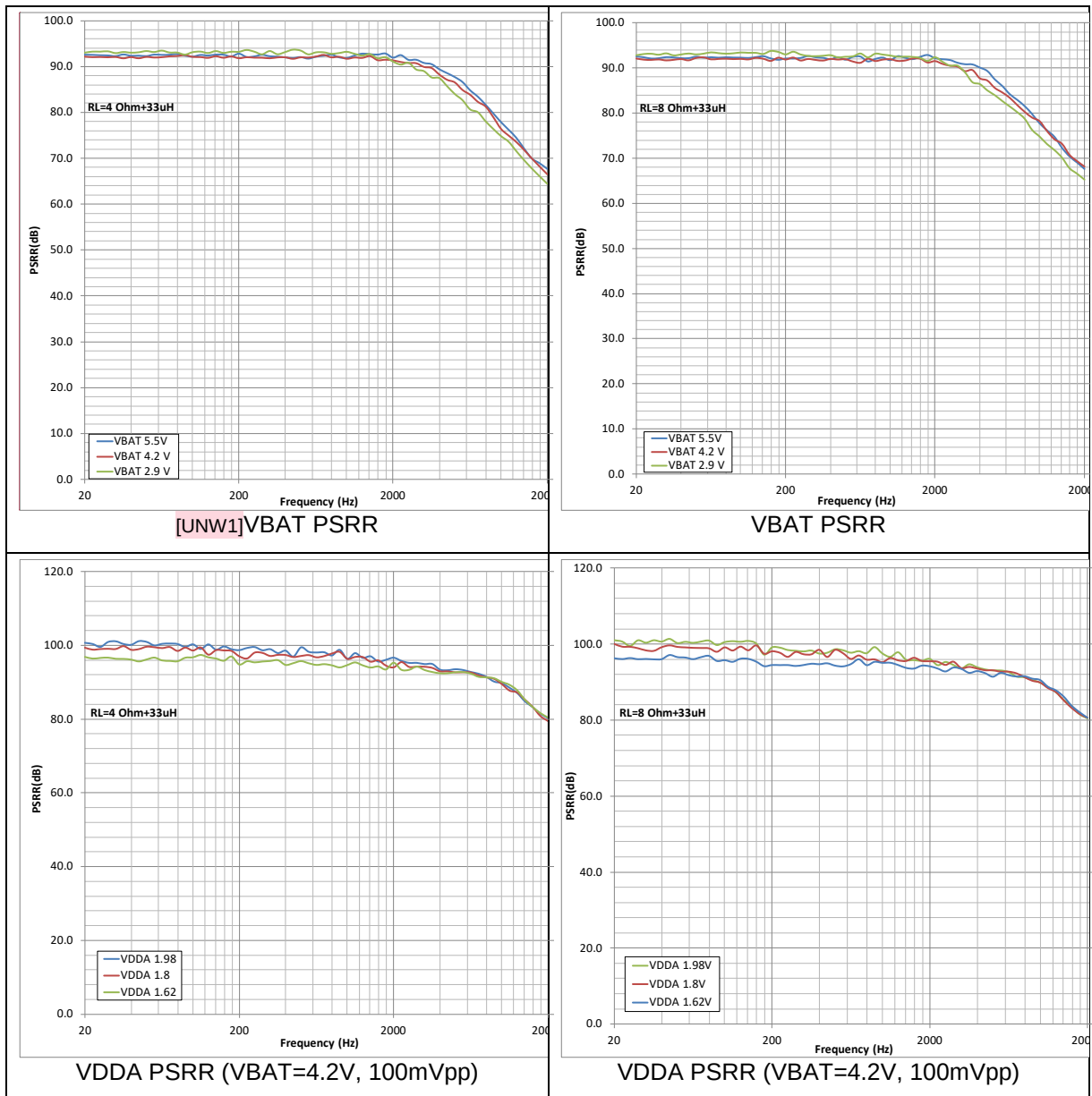


Figure 5 NAU8331 PSRR Plots

4.7 Frequency Response Plots

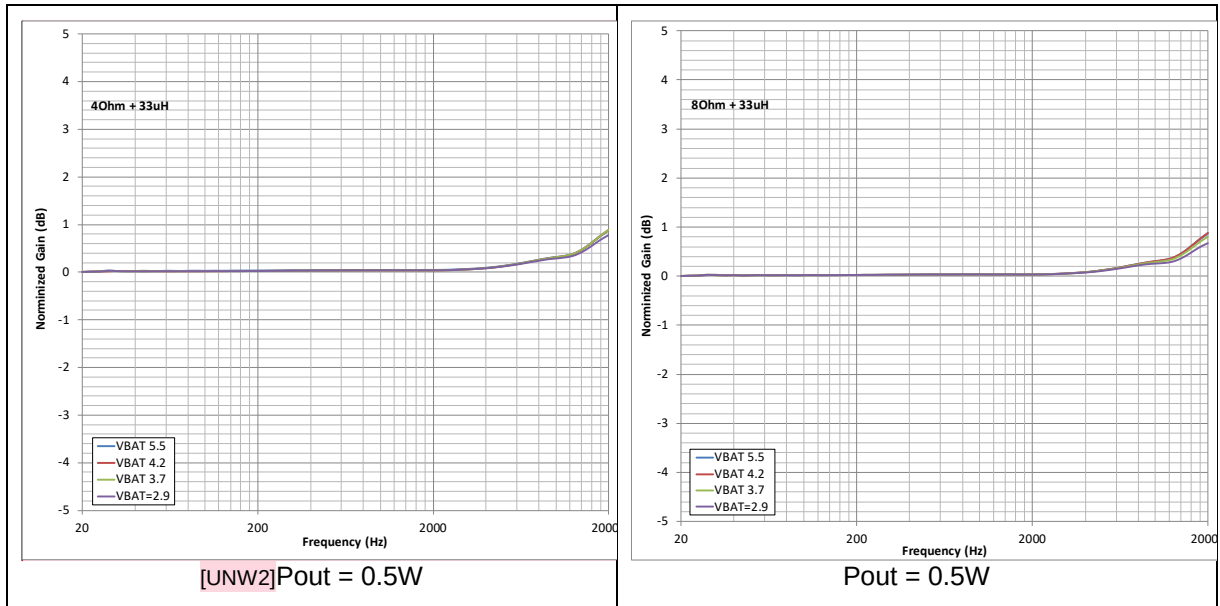


Figure 6 NAU8331 Frequency Response Plots

4.8 Power Plots

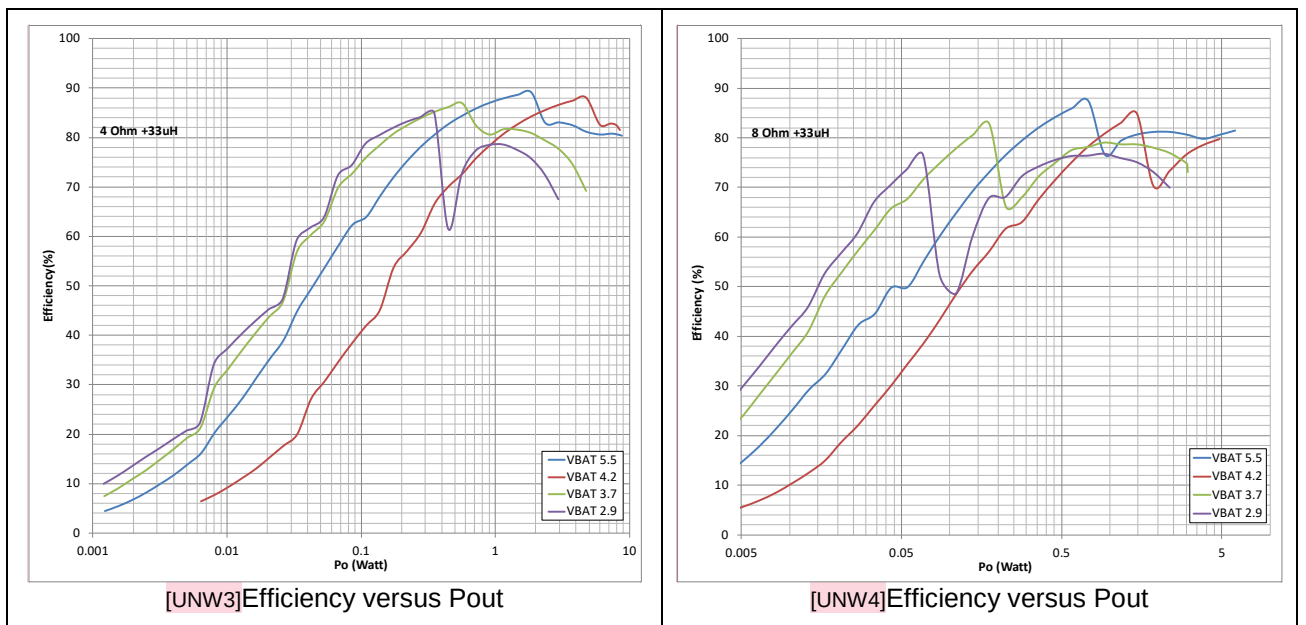


Figure 7 NAU8331 Output Power Plots

5 FUNCTIONAL DESCRIPTION

This chapter provides detailed descriptions of the major functions of the NAU8331 Boosted Amplifier.

5.1 Inputs

The NAU8331 provides digital inputs to acquire and process audio signals with high fidelity and flexibility. There is an input path from an I2S/PCM Interface. Additionally, the NAU8331 has logic control inputs, a stereo digital microphone input and a temperature monitoring input.

5.2 Outputs

The NAU8331 Amplifier has a Class-D PWM driver that can drive an 8 Ohm speaker up a peak voltage of 10 V. A boost converter output provides the supply voltage for the Class-D amplifier. The Class-D output voltage and current sensing data are provided at the I2S/PCM Interface output. Additionally, the NAU8331 has an output for the interrupt and the digital microphone clock.

5.3 ADC, DAC and Digital Signal Processing

The NAU8331 has two independent, high-quality Analog-to-Digital Converters (ADCs) and one Digital-to-Analog Converter (DAC). These are high-performance, 24-bit sigma-delta converters, which are suitable for a very wide range of applications.

The ADC and DAC blocks also support advanced Digital Signal Processing (DSP) subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and to maximize the audio dynamic range supported by the NAU8331.

The ADC and DAC digital signal process can support four-point Dynamic Range Compressors (DRCs), high-pass filters, Automatic Level Control (ALC), soft mute, soft unmute and gain compensation. Two-point DRCs can be programmed to limit the maximum output level and/or boost a low output level.

5.4 Digital Interface

Command and control of the device are accomplished by using either a Serial Control Interface. The simple, but highly flexible, 2-wire Serial Control Interface is compatible with most commonly used command and control serial data protocols and host drivers, and industry standard I2S and PCM devices.

The digital audio I/O data streams can be transferred separately from command and control using either I2S or PCM audio data protocols.

5.5 Power Supply

This NAU8331 has been designed to operate reliably under a wide range of power supply conditions and Power-On/Power-Off sequences. However, the Electro Static Detection (ESD) protection diodes between the supplies impact the application of the supplies. Because of these diodes, the following conditions need to be met:

$$VBAT > VDDA - 1.2 \text{ V and } VDDB > VDDA - 0.6 \text{ V}$$

5.6 Power-On-and-Off Reset

The NAU8331 includes a Power-On-and-Off Reset circuit on-chip. The circuit resets the internal logic control at VBAT and VDDA supply power-up and this reset function is automatically generated internally when power supplies are too low for reliable operation. Reset thresholds are 1.4 V for VDDA during a power-on ramp and 1.2 V for VDDA during a power-down ramp. Reset thresholds are 1.9 V for VBAT during a power-on ramp, and 0.8 V for VBAT during a power-down ramp. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held ON while the power levels for VBAT and VDDA are below their respective thresholds. Once the power levels rise above their thresholds, the reset is released. Once the reset is released, the registers are ready to be written to.

NOTE: It is also important that all the registers should be kept in their reset state for at least 6 μsec .

An additional internal RC filter-based circuit is added which helps the circuit to respond for fast ramp rates ($\sim 3 \mu\text{sec}$) and to generate the desired reset period width ($\sim 3 \mu\text{sec}$ at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50 nsec.

For reliable operation, it is recommended to write to register **REG0X00** through the provided I²C bus upon power-up. This will reset all registers to the known default state.

NOTE: When VDDA is below the power-on reset threshold, the digital IO pins will go to a tri-state condition.

5.7 Voltage Reference (VREF)

The NAU8331 includes a mid-supply, reference circuit that produces voltage close to $VDDA/2$ that is decoupled to VSS through the VREF pin by means of an external bypass capacitor. Because VREF is used as a reference voltage for the majority of the NAU8331, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 μF is used. The Reference Voltage circuitry is shown in **Figure 8**.

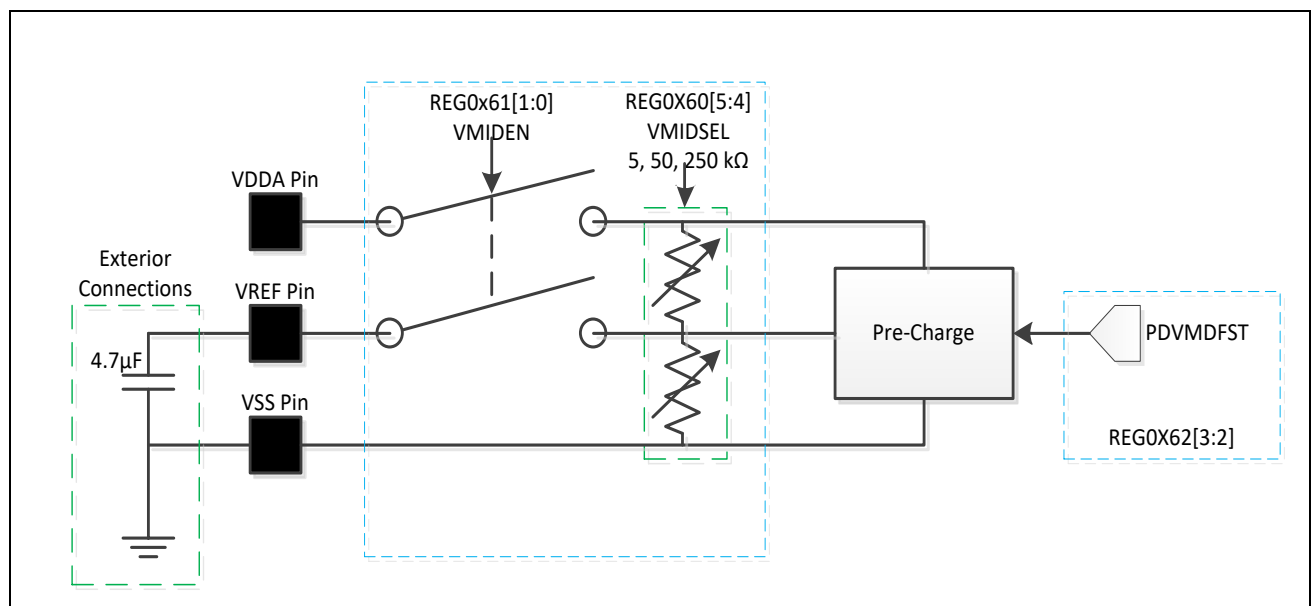


Figure 8 VREF Circuitry

The output impedance can be set using **VMID_SEL** [REG0X60\[5:4\]](#). Refer to **Table 6**.

Table 6 VREF Output Impedance Selection

VMID_SEL REG0X60[5:4]	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50 kOhm	2.5 kOhm
10	250 kOhm	125 kOhm
11	5 kOhm	2.5 kOhm

APPLICATION NOTES:

- Larger capacitances can be used but increase the rise time of VREF and delay the line output signal.
- Due to the high impedance of the VREF pin, it is important to use a low-leakage capacitor.
- A pre-charge circuit has been implemented to reduce the VREF rise time. Once charged, this can be disabled using **PDVMDFAST** [REG0X62\[3:2\]](#) to save power or to prevent rapid changes in level due to fluctuations in VDDA.

5.8 DAC Soft Mute

The Soft Mute function ramps down the DAC digital volume to zero when it is enabled by **SMUTE_EN** [REG0X13\[15\]](#). When disabled, the volume increases to the register-specified volume level for each channel. This function is beneficial for using the DAC without introducing pop-and-click sounds. When **DACEN_SM** [REG0X13\[13\]](#) is set to '0', the volume will ramp up to the register-specified volume level if the DAC path has been enabled by setting **DACEN** [REG0X4\[3\]](#). The volume will ramp down to zero if the DAC path is disabled.

5.9 Companding

Companding is used in digital communication systems to optimize Signal-to-Noise Ratios (SNR) with reduced data bit rates using non-linear algorithms. The NAU8331 supports the two main telecommunications companding standards -- A-Law and μ -Law -- in both transmit and receive directions. The A-Law algorithm is primarily used in European communication systems; the μ -Law algorithm is primarily used in North American, Japanese, and Australian communications systems.

Companding converts 14 bits (μ -Law) or 13 bits (A-Law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits and 4 mantissa bits. This option can be enabled for the DAC and ADC using the **DACCM0** [REG0X0D\[15:14\]](#) and **ADCCM0** [REG0X0D\[13:12\]](#) registers, respectively. When the Companding Mode is enabled, **CMB8_0** [REG0X0D\[10\]](#) must be enabled for 8-bit operation. This will disable the word length selection in **WLEN0** [REG0X0D\[3:2\]](#) for this port and allow the companding functions to use an 8-bit word length.

The compression equations set by the ITU-T G.711 Standard and implemented in the NAU8331 Amplifier are provided here for reference:

μ-Law

$$F(x) = \frac{\ln(1 + \mu \times |x|)}{\ln(1 + \mu)}, \quad -1 < x < 1$$

$$\mu = 255$$

A-Law

$$F(x) = \frac{A \times |x|}{(1 + \ln(A))}, \quad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1 + \ln(A \times |x|))}{(1 + \ln(A))}, \quad \frac{1}{A} \leq x \leq 1$$

$$A = 87.6$$

5.10 Hardware and Software Reset

The NAU8331 and all of its control registers can be reset to initial default power-up conditions by writing any value to **REG0X00** **once** using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will be set to their power-on default values. This is typically done during hardware reset.

The NAU8331 can be reset to initialized power-up conditions by writing any value to **REG0X01** **twice** using any of the control interface modes. Writing to **REG0X01** will reset the NAU8331, but all registers values will be unaffected. This is typically done during operation to quickly force NAU8331 in the known initialized startup state.

5.11 SAR ADC

The SAR ADC is an 8-bit Analog-to-Digital Converter (ADC) used to detect the voltage level on the VBAT supply voltage, the junction temperature sensor, and the ambient temperature sensor.

5.11.1 SAR ADC Functions

The SAR ADC is enabled by **SAR_ENA_REG0X07[0]**. Setting this bit to 1 enables the SAR ADC; setting the bit to 0 disables the function. After the SAR ADC has been enabled using **SAR_ENA**, the SAR ADC enters a sampling phase. During this phase, the voltage level on the input is sampled at a speed determined by **SAMPLE_SPEED_REG0X07[3:2]**. This time can be adjusted from 2 μsec to 16 μsec, doubling each step, as shown in Table 7 Voltage Sampling Phase Time. During the sampling phase, the sample signal will be high together with the Most Significant Bit (MSB) and low with the Least Significant Bit (LSB).

Table 7 Voltage Sampling Phase Time

<u>SAMPLE_SPEED REG0X07[3:2]</u>	Voltage Sampling Time
00	2 μ sec
01	4 μ sec
10	8 μ sec
11	16 μ sec

The maximum input current of the ADC can be reduced by selecting a bigger input resistor in series with the sampling capacitor. The value of the input resistor can track the sampling time. The SAR series resistor default setting = 001. Additional input limit resistor values and settings are shown in Table 8 SAR ADC Current Limit Resistor Selection.

Table 8 SAR ADC Current Limit Resistor Selection

<u>REL_SEL REG0X07[9:7]</u>	Input Resistor Value
000	35 kOhm
001	70 kOhm
010	170 kOhm
011	360 kOhm
1xx	Short

After the sampling phase, the ADC enters a conversion phase that consists of eight compare cycles. Each of these compare cycles can last from 500 nsec to 4 μ sec, doubling each step. See Table 9 Compare Cycle Time Settings. Use COMP_SPEED REG0X07[6:5] to adjust the compare time. The total conversion has 8 compare cycles.

Table 9 Compare Cycle Time Settings

<u>COMP_SPEED REG0X07[6:5]</u>	Time Settings
00	500 nsec
01	1 μ sec
10	2 μ sec
11	4 μ sec

APPLICATION NOTE:

- SAMPLE_SPEED REG0x07[3:2] is used for the SAR ADC sampling rate. Before changing the sampling rate, SAR_ENA REG0X07[0] needs to be set to 0. After the sample speed is set, SAR_ENA sets to 1.

5.11.2 SAR ADC Control

The NAU8331 needs to process and monitor three inputs: Battery Supply Voltage (VBAT), Junction Temperature (Tj), and Ambient Temperature (Ta), as shown in **Figure 9**.

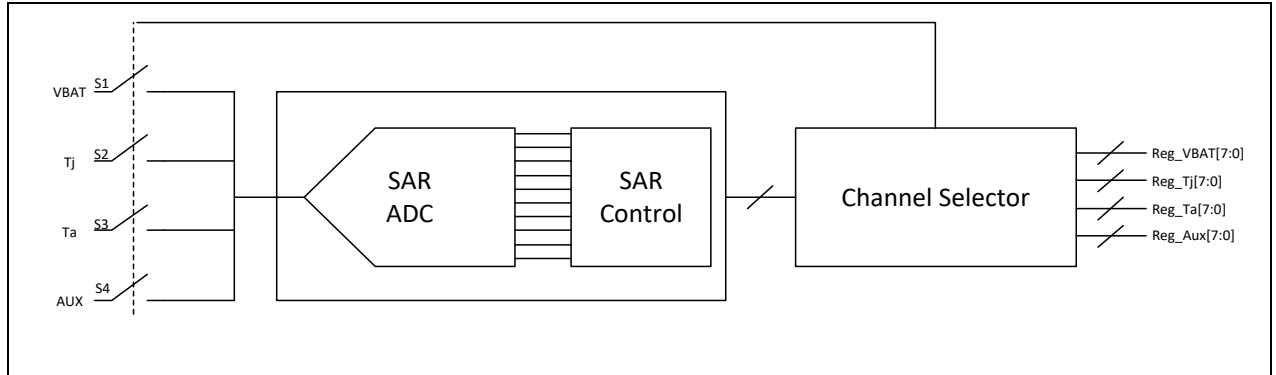


Figure 9 SAR ADC Control

It is important to set the gain in **SAR_TRACKGAIN REG0X07[13:11]** with Target Full Scale Levels of S2, and S3 inputs. **Table 10** lists the register settings.

Table 10 SAR ADC Gain Settings

Gain Settings	SAR_TRACKGAIN REG0X07[13:11]
1.0 * VDDA	000
1.0 * VDDA	001
1.1 * VDDA	010
1.2 * VDDA	011
1.3 * VDDA	100
1.4 * VDDA	101
1.54 * VDDA	110
3.12 * VDDA	111

Notes: The gain for SAR ADC Channel S1 (VBAT) is fixed to 3.12 * VDDA. Table 10 applies only to the Tj and Ta inputs. It is recommended to keep the gain set to 1.0 * VDDA; the raw data can be read from **SAR_ADC_OUT_01 REG0x020** and **SAR_ADC_OUT_23 REG0x021**. To convert from raw SAR ADC from **SAR_ADCOUT_01** and **SAR_ADC_OUT23** please refer to the equations below:

$$VBAT = \frac{(raw \ VBAT)}{255} * (3.12 * VDDA)$$

$$Tj = [(raw \ Tj) - 89] * 1.6077$$

Ta requires additional configuration through the output pin to activate its output.

5.12.1 Enabling Clock Detection

Clock detection in the NAU8331 is enabled by setting **REG0X40 REG_CLKPWRUPN** = 0 (default) and meeting three or four conditions, depending on the configuration. If all conditions are met, the **PWRUPEN** signal will be asserted to 1. If any of the conditions are not met, the **PWRUPEN** signal is set to 0.

Conditions for enabling clock detection:

- 1) The NAU8331 has custom logic clock detection circuits that detect if MCLK is present. Upon MCLK detection, the detector output MCLKDET goes to 1. When the MCLK disappears, MCLKDET goes back to 0. Up to 1 μ sec is required to detect MCLK and the MCLK release time is about 50 μ sec.
- 2) If **REG0X40 REG_APWRUPEN** is set to 1, clock detection will require non-zero samples to enable output of a power-up signal. Any non-zero sample will be sufficient. After power-up, if 2048 zero samples are detected, the **PWRUPEN** signal is asserted to 0. If **REG_APWRUPEN** is set to 0, this function does not control the **PWRUPEN** signal.

5.12.2 Disabling Clock Detection

Clock detection in the NAU8331 is disabled by setting **REG_CLKPWRUPEN** to 1. In this state, **PWRUPEN** is no longer controlled by the enabling conditions listed above, but is set to 1. However, the MCLKDET and clock dividers are still active.

The range of the input clocks is shown in **Table 11**.

Table 11 Range of Input Clocks

Signal	Min	Max
Frame Synch (FS) (kHz)	8	96
Master Clock MCLK (MHz)	2.048	24.576

5.12.3 Sample and Over Sampling Rates

Possible Sample Rate and MCLK_SRC selections are shown in **Table 12** and **Table 13**. Note that **REG_SRATE REG0X40** must be programmed to identify the target sample rate.

Table 12 Sampling and Over Sampling Rates (Ranges 1-3)

REG_SRATE												
MCLK_SRC/FS Ratio	Range 1 000				Range 2 001				Range 3 010			
	FS (kHz)		MCLK_SRC (MHz)		FS (kHz)		MCLK_SRC (MHz)		FS (kHz)		MCLK_SRC (MHz)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
256	8	12	2.048	3.072	16	24	4.096	6.144	32	48	8.192	12.288
400	8	12	3.2	4.8	16	24	6.4	9.6	32	48	12.8	19.2
500	8	12	4	6	16	24	8	12	32	48	16	24

Table 13 Sampling and Over Sampling Rates (Ranges 4-5)

REG_SRATE				
MCLK_SRC/FS Ratio	Range 4 011			
	FS (kHz)		MCLK_SRC (MHz)	
	Min	Max	Min	Max
256	64	96	16,384	24,576
400	64	96	25.6	38.4
500	64	96	32	48

The only internal MCLK_SRC/FS ratios allowed are: 256, 400 & 500. The clock divider or multiplier in register 0x03 needs to be setup to achieve one these three possible ratios.

Effective MCLK/FS ratios can be achieved with the clock multiplier under MCLK > 2Mhz condition, as shown in **Table 14**.

Table 14 Effective MCLK/FS Ratios (MCLK > 2Mhz)

MCLK_SRC/FS ratio	Clock Multiplier (Reg0x03)	Effective ratio MCLK/FS
256	8	32
400	8	50
500	8	62.5
256	4	64
400	4	100
500	4	125
256	2	128
400	2	200
500	2	250
256	1	256
400	1	400
500	1	500

- For MCLK_SRC/FS ratios of 256 the Over Sampling Ratio (OSR) can be set in register 0x28 & 0x29 to: 32, 64, 128 & 256. Note that the ADC & DAC clocks need to be set to their matching values in register 0x03.
- For MCLK_SRC/FS ratios of 400 & 500 the Over Sampling Ratio (OSR) is fixed to 100. For MCLK_SRC/FS ratios of 400 the ADC & DAC clock dividers need to be set to ¼ in register 0x03. For MCLK_SRC/FS ratios of 500 the ADC & DAC clock dividers are automatically set to 1/5.

5.12.4 Boost Clock Divider

The NAU8331 includes a divider that provides a fixed clock of about 2 MHz, depending on the sample rate setting and the MCLK_SRC/FS ratio. The boost converter clock is derived from the **MCLK_SRC**. As well as programming the **REG_SRATE** **REG REG0X40** register, the user can program **REG_MINMAX** to identify the approximate sample rate within the selected range. Based on this, the divider is determined as shown in **Table 15** and

Table 16.

Table 15 Boost Clock Divider Settings (Ranges 1-3)

REG_SRATE												
MCLK_SRC/FS Ratio	Range 1 000				Range 2 001				Range 3 010			
	FS (kHz)		CLK2 (MHz) Divider		FS (kHz)		CLK2 (MHz) Divider		FS (kHz)		CLK2 (MHz) Divider	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
256	8	12	1	1.5	16	24	2	3	32	48	4	6
400	8	12	1.5	2.5	16	24	3	5	32	48	6	10
500	8	12	2	3	16	24	4	6	32	48	8	12

Table 16 Boost Clock Divider Settings (Ranges 4-5)

REG_SRATE				
MCLK_SRC/FS Ratio	Range 4 011			
	FS (kHz)		CLK2 (MHz) Divider	
	Min	Max	Min	Max
256	64	96	8	12
400	64	96	12	20
500	64	96	16	24

5.13 Boost Control

The NAU8331 has a boost converter with digitally programmable levels. The boost converter output level is determined by the absolute peak signal level at the output of the DAC AGC amplifier. When the peak signal level is below VBAT, the boost converter is switched off and, in the default off state, the boost converter will connect the output VBST to VBAT. For higher output levels, the boost converter will target a level, depending on the actual signal level. In order for the output signal to remain undistorted, the boost converter responds immediately to a level increase. Also, an offset level (programmable) is maintained between the signal level and target VBST. For a level decrease, the boost target can be decreased after a programmable delay time.

To reduce the stress and current spikes on the boost capacitor, the boost target voltage is not instantly changed. Instead, the voltage is stepped up and down in about 0.160 V increments at 4 µsec or more per step (programmable). This limits the boost capacitor charge/discharge current to about:

$$I = 22 \mu\text{sec} \times 0.160/4 \mu\text{sec} = 0.880 \text{ A}$$

The boost input target has a resolution of 6 bits. Not all of the possible target levels are used due to the minimum VBAT supply voltage of 2.9 V. If the target level is below 2.7 V, the boost converter will be off. Target levels are listed in **Table 17**.

Table 17 Boost Input Target Voltage Selection

BSTTARGET[5:0]	Boost Target Voltage (V)	Comment
0	0.9	Boost OFF (Below Minimum VBAT of 2.7 V)
1	1.06	
2	1.22	
3	1.38	
4	1.54	
5	1.7	
6	1.86	
7	2.02	
8	2.18	
9	2.34	
10	2.5	
11	2.66	
12	2.82	Boost ON (Above Minimum VBAT of 2.7 V)
13	2.98	
14	3.14	
61	10.66	
62	10.82	
63	10.98	

The Target Boost Voltage, **BSTTARGET[5:0]** (**REG0X1C**), is an unsigned binary number described as:

$$\text{VBST, target} = 0.9 \text{ V} + 0.16 \text{ V} \times \text{BSTTARGET}[5:0].$$

The **BSTTARGET[5:0]** signal is derived from the peak signal level at the DAC ALC amplifier signal output and **VBAT**.

To avoid distortion, a Boost Signal Margin (**REG0X17**) **BSTMARGIN[5:0]** (programmable, 64 x 0.16 V) is retained between the Boost Target Voltage and the Peak Output Level. **BSTMARGIN[5:0]** is an unsigned binary number that is programmed in a register. Additionally, **BSTTARGET[5:0]** is limited to the maximum set in the Boost Limit register, (**REG0X17**) **BSTLIMIT[5:0]**, an programmable unsigned binary number. Thus, the **BSTTARGET[5:0]** signal is described as:

$$\text{BSTTARGET}[5:0] = \text{MINIMUM} (\text{BSTLIMIT}[5:0], (\text{DACPEAK}[5:0] + \text{BSTMARGIN}[5:0]))$$

DACPEAK[5:0] is an unsigned binary number that represents the DAC AGC amplifier output real time rectified peak level. '000000' represents no signal and '111111' represents full scale. If the computation, of **BSTTARGET[5:0]** exceeds 0x3F (63 decimal), then it will clip to 0x3F.

Additionally, a signal **BSTVBATB** (**REG0X4A**) is set low when the Boost Target is less than VBAT or less than 2.7 V. It indicates when the boost converter is enabled.

The Boost Voltage VBST only changes one LSB per step, until it reaches the computed **BSTTARGET[5:0]** value.

The step time is programmable and is set by register **BSTSTEPTIME[2:0]** as shown in **Table 18**. The time step values can be derived from the internal 2 MHz reference clock.

Table 18 Programmable Step Time Settings

BSTSTEPTIME[2:0]	Time per 0.16 V step (usec)
000	4 (default)
001	8
010	16
011	32
100	1
101	2
110	64
111	128

When **BSTVBATB** = 1 AND the computed **BSTTARGET[5:0]** has decreased from the previous target for more than a programmable delay, set in **BSTDELAY[3:0]**, then the Boost Voltage VBST is reduced to the new target, one step at a time. The time per step is programmable per the settings given in **Table 18**. The programmable delay is shown in **Table 19**.

Table 19 Programmable Boost Delay

BSTDELAY[3:0]	Boost Step Down Delay (msec)
0	0
1	1
2	2
3	4
4	8
5	16
6	32
7	64
8	128

5.14 Automatic Level Control

The digital Automatic Level Control (ALC) supports the input digital audio path of the NAU8331 by providing an optimized signal level at the output of the Class-D Amplifier. This is achieved by automatically decreasing the amplitude of the input signal according to the user's set amplitude, clipping, or low battery voltage, and restoring amplitude when conditions are lifted. **Figure 11** illustrates the basic relationship of the ALC to other major functions of the NAU8331.

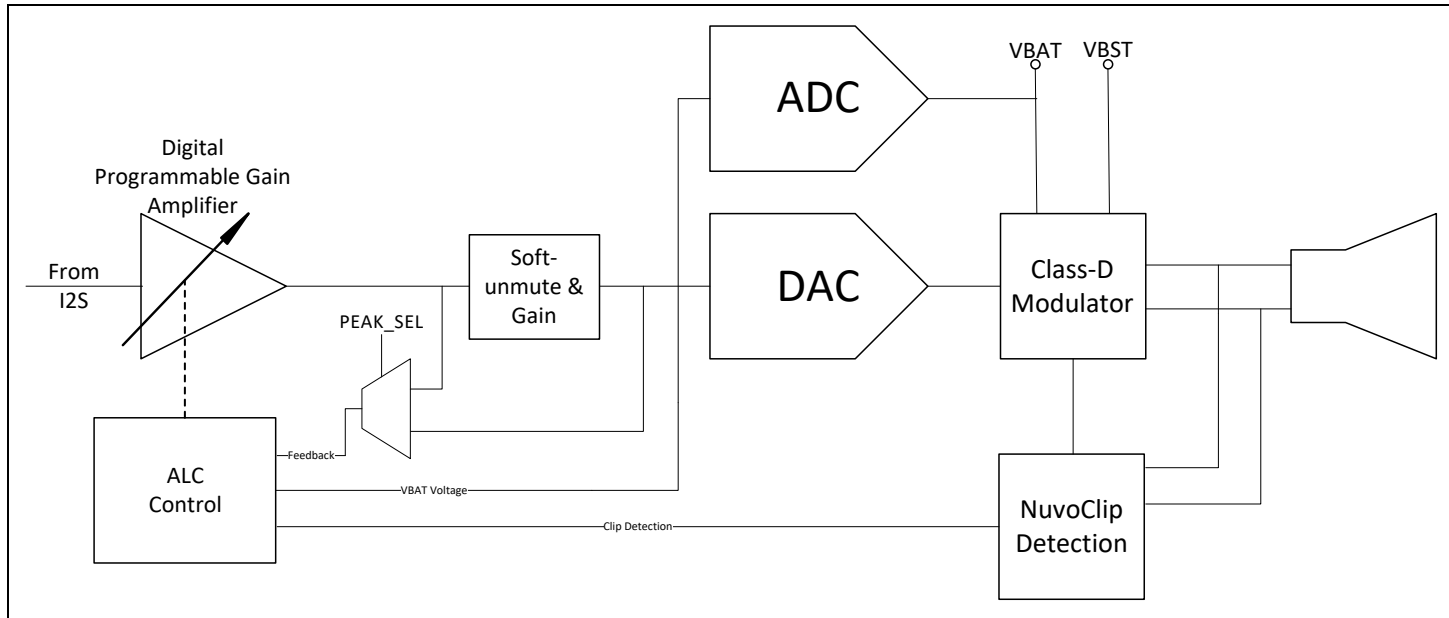


Figure 11 Automatic Level Control

5.14.1 ALC Operation

The ALC is enabled by [ALC_CTRL3.ALC_EN_REG0x2E\[15\]](#) and operates according to the Limiter Mode register [ALC_CTRL3.LIM_MDE_REG0x2E\[14:12\]](#). It uses feedback to detect the signal output level from either the output of the digital Programmable Gain Amplifier (dPGA) or output of the soft mute gain compensation through a Peak Detector, set by [ALC_CTRL4.PEAK_SEL_REG0x2F\[13\]](#) which controls the peak selection for both the ALC and Boost Converter. Using the output of the dPGA provides a direct feedback for control while using the output of the soft mute gain compensation allows for the ALC to adjust based on the activation of the soft mute, deactivating when the soft-mute function drops the signal below the user's set amplitude or reactivating when disabling the soft-mute when signal rises above the set amplitude and/or clipping. More information can be read about the soft mute in [Section 5.8](#).

The Peak Detector can be configured by either using a full-wave rectification peak, ensuring equal ALC operation on both positive and negative signals, or absolute value calculated peak, which updates at every peak and degrades until a new peak is detected. This is set in [ALC_CTRL1.ALCPKSEL_REG0x2C\[11\]](#). Additionally, the ALC can update either from the zero crossing point of the signal or immediately upon triggering. This is determined by the register [ALC_CTRL1.ALC_ZC_REG0x2C\[14\]](#) and when enabled also overrides the register [ALC_CTRL4.LPGA_ZC_REG0x2F\[14\]](#) to ensure zero crossing point reference consistency. ALC updating on the zero crossing point ensures that if the ALC responds faster than the signal degrades, the ALC will wait until the signal reaches close to zero before changing the gain on the dPGA, or input signal gain. This may be helpful depending on the application and can reduce popping on speakers. If immediate action is needed for input signal attenuation then [ALC_ZC](#) can be disabled. The ALC has

three operational states: *ALC Attack*, *ALC Release*, and *ALC Hold*. In the *ALC Attack* state, the ALC decreases the **dPGA** gain at a single dB decrement at a time, gradually based on the **ALCATK** register; in the *ALC Release* state, the ALC increases the **dPGA** gain at a single dB increment at a time gradually based on the **ALCDCY** register; in the *ALC Hold* state, the ALC holds constant the **dPGA** gain for a specified time determined by the **ALCHLD** register. While the attack state is immediate upon meeting conditions, the ALC will enter the hold state before releasing the signal. This is to account for any noise or fluctuations that may occur on the input signal.

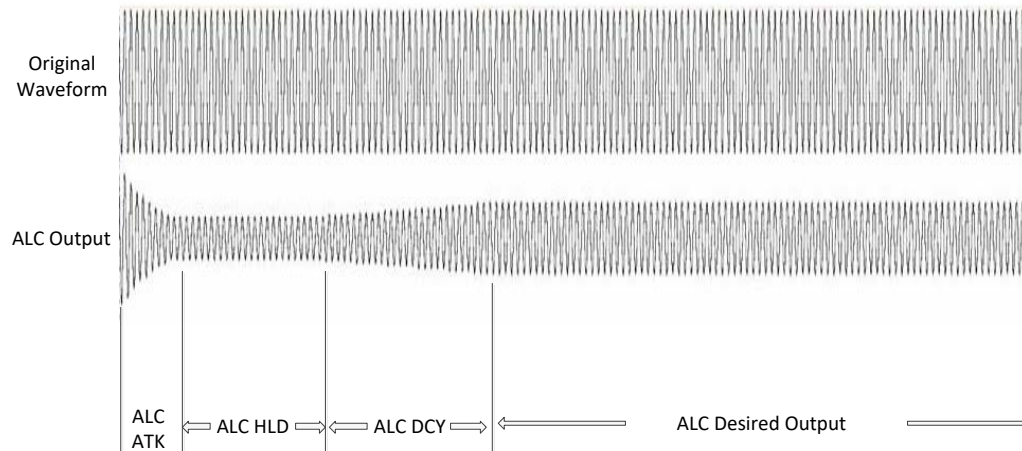


Figure 12 ALC Attack, Hold and Decay

The registers below are used in every ALC operational mode that are defined in **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]**.

- **ALC_CTRL3.ALC_EN_REG0x2E[15]** – ALC Enable Register, enables the ALC for operation.
- **ALC_CTRL4.PEAK_SEL_REG0x2F[13]** – Selects the feedback for peak detection from the output of the **dPGA** of which the ALC controls (1) or the soft mute gain compensation (0).
- **ALC_CTRL1.ALCPKSEL_REG0x2C[11]** – Selects between full-wave rectification peak (0) or absolute value calculated peak (1).
- **ALC_CTRL1.ALC_ZC_REG0x2C[14]** – Selects whether the ALC should update immediately at peak detection or at the zero crossing point of the signal. This is recommended as it prevents sudden changes that may occur.
- **ALC_CTRL1.ALCMAXGAIN_REG0x2C[7:5]** – The maximum gain level allowed to be set by the ALC on the **dPGA** when enabled. This is applied automatically when ALC is enabled and acts as the upper limit the input signal is allowed until ALC is disabled.
- **ALC_CTRL1.ALCMINGAIN_REG0x2C[3:1]** – The minimum gain level allowed to be set by the ALC on the **dPGA** when enabled. This acts as the lowest limit the input signal is allowed until the ALC is disabled.
- **ALC_CTRL2.ALCDCY_REG0x2D[15:12]** – The rate at which the ALC will *release*, or increase the gain of, the signal determined by step time doubling its increment from 2μs to 4196μs at 0.1875dB per step. Typically, the decay time is much slower than the attack time. When the DAC output level is below the ALC Target value by at least 1.5 dB, the gain increases at a rate determined by this parameter. In Limiter Mode, the time constants are faster than in ALC mode.
- **ALC_CTRL2.ALCATK_REG0x2D[11:8]** – The rate at which the ALC will *attack*, or attenuate, the signal determined by step time doubling its increment from 2μs to 4196μs at 0.1875dB per step.

Typically, the attack time is much faster than the decay time. In the NAU8331, when the absolute value of the DAC output exceeds the ALC Target Value **ALCLVL**, the gain will be reduced at a step-size and rate determined by this parameter. When the peak DAC output is at least 1.5 dB lower than the **ALCLVL**, the stepped gain reduction will halt.

- **ALC_CTRL2.ALCHLD_REG0x2D[7:4]** – The length of time at which the ALC will hold the signal for, ranging from 0ms to 512ms. Hold time refers to the duration of time when no action is taken. This is typically used to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU8331, the hold time value is the duration of time that the ADC output peak value must be less than the target value, **ALCLVL**, before there is an actual gain increase.
- **ALC_CTRL2.ALCLVL_REG0x2D[3:1]** – A requirement for the input signal level to hold at after clearing the conditions specified in each of the ALC operational mode for the amount of time set in the **ALCHLD** register before entering the ALC Release state, or increase the gain of the **dPGA** at the rate specified by the **ALCDCY** register. This value is expressed as a fraction of Full Scale (FS) output from the DAC. Depending on the logic conditions, the output value used in the comparison may be either the instantaneous value of the DAC *or* a time weighted average of the DAC peak output level.

NOTE: See **Chapter 6 Control and Status Registers**: Registers 0x2C to 0x2F for more information regarding settings for ALC functions.

The following are different operational modes allowed by the **LIM_MDE** control register:

- Clip Limiting Mode
- Low-Battery Clip Limiting Mode
- Normal Limiting Mode
- Low-Battery Limiting Mode
- Low-Battery Limiting Mode with Preprogrammed VBAT Ratio

NOTE: The gain range for the **dPGA** is restricted between **ALCMAXGAIN** and **ALCMINGAIN**. Upon enabling of the ALC, the **dPGA** is automatically set to the **ALCMAXGAIN** and when an ALC event triggers, the gain is adjusted according to the conditions as long as the target attenuation level is below the **ALCMAXGAIN** and above the **ALCMINGAIN** restrictions.

5.14.1.1 Clip Limiting Mode

Registers used in Clip Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=000** – ALC limiter mode set to **000** for operation based on clipping
- **ALC_CTRL4.CLIP_GAINADJUST_REG0x2F[12:10]** – *Maximum attenuation* adjustment level as a comparison from the level clipping is detected. This value can range between the ranges of 0 to -7dB and will act as a soft wall, limiting the max gain change in each *Attack* State session or clipping event. This adjustment is limited by the **ALCMINGAIN** register, restricted to -32dB in this mode, where the *maximum attenuation* change cannot surpass this value.
- **CLIP_CTRL_REG0x69[4]** – Activation register for clip detection circuit is set to enable for detecting clipping. This is required to detect clipping in this mode.

Description:

In **Clip Limiting Mode**, **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=000**, the DAC output is programmed to limit clipping by lowering the **dPGA** gain when clipping is detected. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay.

A clip detection signal is provided by the NuvoClip detection circuit so long as the **CLIP_CTRL** register is enabled. As soon as a clipping event is detected, the ALC goes into the *Attack* State, lowering the **dPGA** gain at the pre-programmed rate in the **ALCATK** register. This continues until the clipping detection no longer detects a clipping signal or if the *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached. If another consecutive clipping event occurs the ALC gain continues ramping down until another *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached or until the **ALCMINGAIN** has been reached. The gain setting applied by this method will remain constant until the output signal no longer clips **AND** the input signal level becomes 1.5dBFS **below** the ALC Target Level specified in the **ALCLVL** register for the entirety of the ALC *Hold* state specified in the ALC Hold Register **ALCHLD**, before the ALC enters the *Release* State to increase the gain at the rate specified in the **ALCDCY** register until the signal is at full scale or it clips again. If clipping again, the ALC will repeat this process to ensure no clipping.

Example Problem Set: Ensure that no clipping occurs. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0x2C** = 0x20E0
 - o [14] **ALC_ZC** set to update the ALC instantaneously prevent clipping as soon as possible
 - o [11] **ALCPK_SEL** set to update Peak Detection on rectified value.
 - o [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
 - o [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
 - o The rest is left at default.
- **ALC_CTRL2.REG0x2D** = 0x5353
 - o [15:12] **ALCDCY** set to 16ms/step at 0.1875dB **increase** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is **lower**, then the ALC takes another step. If the signal peak is **higher**, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
 - o [11:8] **ALCATK** set to 16us/step at 0.1875dB **decrease** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
 - o [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
 - o [3:1] **ALCLVL** set to -6dBFS. This is the comparison level which triggers the state of the ALC to go into Release or Hold and can affect stability of the signal.
 - o The rest is left at default.
- **ALC_CTRL3.REG0x2E** = 0x8010
 - o [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
 - o [14:12] **LIM_MDE** is set to 000. This is set to Clip Limiting mode and follows the operation explained in the description portion of this section.
 - o The rest is left at default.
- **ALC_CTRL4.REG0x2F** = 0x0C20
 - o [12:10] **CLIP_GAINADJUST** set to -3dB as a soft-wall to change at a single clipping event.
- **CLIP_CTRL_REG0x69** = 0x0010

- o [4] Enable the Nuvo Clip Detection Circuit.

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence from first to last: **0x2C**, **0x2D**, **0x2E**. The register **0x2E** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.14.1.2 Low Battery Clip Limiting Mode

Registers used in Low Battery Clip Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=001** – ALC limiter mode set to **001** for operation based on low battery and clipping mode
- **ALC_CTRL3.VBAT_THRESHOLD_REG0x2E[9:5]** – VBAT threshold value as an additional condition for ALC activation. This can be paired with other conditions or can require additional settings depending on the ALC operational mode.
- **ALC_CTRL4.CLIP_GAINADJUST_REG0x2F[12:10]** – *Maximum attenuation* adjustment level as a comparison from the level clipping is detected. This value can range between the ranges of 0 to -7dB and will act as a soft wall, limiting the max gain change in each *Attack* State session or clipping event. This adjustment is limited by the **ALCMINGAIN** register, restricted to -32dB in this mode, where the *maximum attenuation* change cannot surpass this value.
- **CLIP_CTRL_REG0x69[4]** – Activation register for clip detection circuit is set to enable for detecting clipping. This is required to detect clipping in this mode.

Description:

In **Low Battery Clip Limiting Mode**, **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=001**, the DAC output is programmed to limit clipping by lowering the **dPGA** gain when clipping is detected with the condition of activating during low battery voltage operation. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay. A clip detection signal is provided by the NuvoClip detection circuit so long as the **CLIP_CTRL** register is enabled. Immediately when a clipping event is detected **AND** the VBAT voltage is below the voltage specified in the **VBAT_THRESHOLD** register, ALC will go into ALC *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the **ALCATK** register until the clipping detection no longer detects a clipping signal or if the *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached. If another consecutive clipping event occurs the ALC gain continues ramping down until another *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached or until the **ALCMINGAIN** has been reached. If either of the conditions are lifted, i.e. battery voltage is above **VBAT_THRESHOLD** or the clipping is no longer detected, then the ALC will wait until the input signal level becomes 1.5dBFS **below** the ALC Target Level, set in the **ALCLVL** register, for the period of the ALC *Hold* state, based on time specified in the **ALCHLD** register. The ALC will then enter the *Release* state, increasing the gain at the rate specified in the **ALCDCY** register until reaching the maximum gain allowed, **ALCMAXGAIN**, or another clipping event is detected.

Example Problem Set: Ensure that no clipping occurs when VBAT lowers below 3.83V, this is most likely to happen when using a battery. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0x2C = 0x20E0**
 - o [14] **ALC_ZC** set to update the ALC instantaneously prevent clipping as soon as possible
 - o [11] **ALCPK_SEL** set to update Peak Detection on rectified value.

- o [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
- o [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
- o The rest is left at default.
- **ALC_CTRL2.REG0x2D = 0x5353**
 - o [15:12] **ALCDCY** set to 16ms/step at 0.1875dB **increase** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is **lower**, then the ALC takes another step. If the signal peak is **higher**, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
 - o [11:8] **ALCATK** set to 16us/step at 0.1875dB **decrease** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
 - o [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
 - o [3:1] **ALCLVL** set to -6dBFS. This is the comparison level which triggers the state of the ALC to go into Release or Hold and can affect stability of the signal.
 - o The rest is left at default.
- **ALC_CTRL3.REG0x2E = 0x9210**
 - o [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
 - o [14:12] **LIM_MDE** is set to 001. This is set to Low Battery Clip Limiting mode and follows the operation explained in the description portion of this section.
 - o [9:5] **VBAT_THRESHOLD** is set to 3.83V to ensure ALC activation at this voltage.
 - o The rest is left at default.
- **ALC_CTRL4.REG0x2F = 0x0C20**
 - o [12:10] **CLIP_GAINADJUST** set to -3dB as a soft-wall to change at a single clipping event.
- **CLIP_CTRL_REG0x69 = 0x0010**
 - o [4] Enable the Nuvo Clip Detection Circuit.

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence from first to last: **0x2C**, **0x2D**, **0x2E**. The register **0x2E** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.14.1.3 Normal Limiting Mode

Registers used in Normal Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=010** – ALC limiter mode set to **010** for operation based on user's set amplitude.

Description:

In **Normal Limiting Mode**, **ALC_CTRL3.LIM_MDE_REG0x2E[14:12] = 010**, a maximum DAC output level is programmed to limit the full scale output level. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay. The signal peak is read continuously until the level reaches above the user's set amplitude in the **ALCLVL** register. Upon

overstepping the set amplitude, the ALC will enter the *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a lower level than the **ALCLVL** register. When the input signal level becomes 1.5dBFS below the ALC target level (**ALCLVL** register), then the ALC enters *Hold* state, holding the **dPGA** gain for a specified time determined by the **ALCHLD** register. The ALC then goes into the *Release* state, increasing the **dPGA** gain at the pre-programmed rate specified in the **ALCDCY** register until the **dPGA** gain is at maximum or until the peak returns a level above the **ALCLVL** register, in which the ALC will be triggered and enter the *Attack* state again.

Example Problem Set: Limit maximum output to not exceed -3dBFS limit and update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0x2C = 0x68E0**
 - o [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
 - o [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
 - o [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
 - o [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
 - o The rest is left at default.
- **ALC_CTRL2.REG0x2D = 0x5350**
 - o [15:12] **ALCDCY** set to 16ms/step at 0.1875dB **increase** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is **lower**, then the ALC takes another step. If the signal peak is **higher**, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
 - o [11:8] **ALCATK** set to 16us/step at 0.1875dB **decrease** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
 - o [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
 - o [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
 - o The rest is left at default.
- **ALC_CTRL3.REG0x2E = 0xA010**
 - o [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
 - o [14:12] **LIM_MDE** is set to 010. This is set to Normal Limiting mode and follows the operation explained in the description portion of this section.
 - o The rest is left at default.
- **ALC_CTRL4.REG0x2F = 0x0020**
 - o Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence

from first to last: **0x2C**, **0x2D**, **0x2E**. The register **0x2E** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.14.1.4 Low Battery Limiting Mode

Registers used in Low Battery Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=011** – ALC limiter mode set to **011** for operation based on low battery mode.
- **ALC_CTRL3.VBAT_THRESHOLD_REG0x2E[9:5]** – VBAT threshold value as the condition for ALC activation within **LIM_MDE** = 011 and 100. The available values range from 3.14V (1111) to 4.61V (0000) at ~0.10V to 0.11V steps. For exact values, please refer to the Section **7.5**, the Control Register List.

Description:

In **Low-Battery Limiting Mode**, **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=011**, a maximum DAC output level is programmed to limit the full scale output level with the additional constraint of low-battery activation. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay.

The ALC activates when the VBAT voltage declines below the set value in the **VBAT_THRESHOLD** register. The signal peak is read continuously until the level reaches above the user's set amplitude in the **ALCLVL** register. Upon overstepping the set amplitude, the ALC will enter the *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a lower level than the **ALCLVL** register.

When the input signal level becomes 1.5dBFS below the ALC target level (**ALCLVL** register), then the ALC enters *Hold* state, holding the **dPGA** gain for a specified time determined by the **ALCHLD** register. The ALC then goes into the *Release* state, increasing the **dPGA** gain at the pre-programmed rate specified in the **ALCDCY** register until the **dPGA** gain is at maximum or until the peak returns a level above the **ALCLVL** register, in which the ALC will be triggered and enter the *Attack* state again.

If VBAT were to be recharged at any given moment, the ALC will cease triggering and return to an idle state until VBAT lowers its level below the **VBAT_THRESHOLD** register again.

Example Problem Set: When battery becomes discharged lower than 3.53V, limit maximum output to not exceed -3dBFS limit to lessen battery discharge. Additionally, update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0x2C = 0x68E0**
 - o [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
 - o [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
 - o [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
 - o [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
 - o The rest is left at default.
- **ALC_CTRL2.REG0x2D = 0x5350**
 - o [15:12] **ALCDCY** set to 16ms/step at 0.1875dB **increase** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is **lower**, then the ALC takes another step. If the

- o signal peak is **higher**, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
- o [11:8] **ALCATK** set to 16us/step at 0.1875dB **decrease** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
- o [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
- o [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
- o The rest is left at default.
- **ALC_CTRL3.REG0x2E = 0xB2D0**
 - o [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
 - o [14:12] **LIM_MDE** is set to 011. This is set to Low Battery Limiting mode and follows the operation explained in the description portion of this section.
 - o [9:5] **VBAT_THRESHOLD** is set to 3.53V for ALC activation at this voltage.
 - o The rest is left at default.
- **ALC_CTRL4.REG0x2F = 0x0020**
 - o Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence from first to last: **0x2C**, **0x2D**, **0x2E**. The register **0x2E** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.14.1.5 Low Battery Limiting Mode with Pre-programmed VBAT Ratio

Registers used in Low Battery Limiting Mode with Pre-programmed VBAT Ratio:

- **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=100** – ALC limiter mode set to **100** for operation based on a split operation, #1 or #2, between above or below VBAT threshold, respectively. Operation 1: Normal Limiting Mode as specified in **0**. Operation 2: ALC Target Level follows a ratio of the sense VBAT voltage. More information of the two modes can be found in the description of this section.
- **ALC_CTRL3.VBAT_THRESHOLD_REG0x2E[9:5]** – VBAT threshold value as the condition for ALC activation within **LIM_MDE** = 011 and 100. The available values range from 3.14V (1111) to 4.61V (0000) at ~0.10V to 0.11V steps. For exact values, please refer to the Section **7.5**, the Control Register List.
- **ALC_CTRL3.VBAT_RATIO_REG0x2E[11:10]** – VBAT ratio, an additional setting only used for LIM_MDE=100. This changes the ALC output level based on the sensed VBAT voltage.

Description:

In **Low-Battery Limiting Mode with Preprogrammed VBAT Ratio**, **ALC_CTRL3.LIM_MDE_REG0x2E[14:12]=100**, there are **two modes** within its **operation**, one above the VBAT Threshold and another below the VBAT Threshold, in which the threshold can be set in the **VBAT_THRESHOLD** register. Above the VBAT Threshold (**Operation 1**), the ALC functions the same as Normal Limiting Mode as specified in **0**. Below the VBAT Threshold (**Operation 2**), the maximum DAC output level is programmed to attenuate the full scale output level based on the ratio, specified in the **VBAT_RATIO** register, of the **VBAT_THRESHOLD**, also in its own register, minus the sensed VBAT voltage. The equation describing this operation is shown below:

$$V_{out} = V_{out (VBAT > VBAT_{threshold})} - [RATIO_{VBAT} * (VBAT_{threshold} - V_{BAT})]$$

The output voltage, V_{rms} , is determined by the VBAT acquired when VBAT is greater than the threshold voltage, minus by the ratio multiplied by the difference of threshold voltage and current VBAT voltage. The ALC activates when the VBAT voltage declines below the set value in the **VBAT_THRESHOLD** register. Before the activation, the peak voltage of the output is recorded from the peak detector and used for the variable $V_{out(VBAT > VBAT_{threshold})}$ in the equation above. Immediately upon activation, the ALC will enter the *Attack* state, lowering the **dPGA** gain by the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a level lower or equal to the V_{out} described in the equation above where V_{out} is the representation of the output ALC level. This level can be calculated from the equation below and is rounded to the nearest whole number:

$$ALC \text{ Attenuation Level} = 20 \log \left(\frac{V_{out}}{V_{out (VBAT > VBAT_{threshold})}} \right)$$

Take note that the ALC attenuation occurs at incremental steps of 1dB and thus the steps can be accurately calculated if the V_{out} is known. If the input signal extends beyond V_{out} while the VBAT voltage is lower than the VBAT Threshold, the ALC enters the ALC *Attack* state, lowering the **dPGA** gain at the pre-programmed rate set in the **ALCATK** register. This continues until the DAC output level has been reduced to below the limit threshold. This limits DAC clipping if there is a sudden increase in the input signal level. During the whole of Operation 2, while the VBAT is charging and the ALC has been activated, the ALC will remain at its current gain level until VBAT has increased above **VBAT_Threshold**. An example of this is when VBAT starts at 3.6V, while **VBAT_Threshold** is 3.4V, and drops to 2.7V, this is theoretically enough make the ALC gain at -1dB when there's constant input, i.e. music or a wave. When the VBAT is being charged, the ALC gain will remain at -1dB until the VBAT is above 3.4V.

NOTE: The maximum gain at full scale input is set by the ALC Target Level, **ALCLVL**.

Example Problem Set: When battery becomes discharged lower than 3.93V, limit maximum output to not exceed -3dBFS limit to lessen battery discharge. Additionally, update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0x2C** = 0x**68E0**
 - o [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
 - o [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
 - o [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
 - o [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
 - o The rest is left at default.
- **ALC_CTRL2.REG0x2D** = 0x**5350**
 - o [15:12] **ALCDCY** set to 16ms/step at 0.1875dB **increase** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is **lower**, then the ALC takes another step. If the signal peak is **higher**, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
 - o [11:8] **ALCATK** set to 16us/step at 0.1875dB **decrease** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak

is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.

- o [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
- o [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
- o The rest is left at default.
- **ALC_CTRL3.REG0x2E** = 0xB5D0
 - o [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
 - o [14:12] **LIM_MDE** is set to 011. This is set to Low Battery Limiting mode and follows the operation explained in the description portion of this section.
 - o [11:10] **VBAT_RATIO** is set to 2:1 to lower the input signal gain following this linear pattern based on VBAT. As VBAT lowers, the input signal gain will also lower by this amount in 1dB increments.
 - o [9:5] **VBAT_THRESHOLD** is set to 3.93V for ALC activation at this voltage.
 - o The rest is left at default.
- **ALC_CTRL4.REG0x2F** = 0x0020
 - o Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence from first to last: **0x2C**, **0x2D**, **0x2E**. The register **0x2E** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

The input and output waveforms for ALC during limiter operation are shown in **Figure 13** and **Figure 14**. The waveforms during ALC limiter operation as the gain is reduced are shown in **Figure 13**, while the input and output waveforms during ALC limiter operation as the gain is released are shown in **Figure 14**.

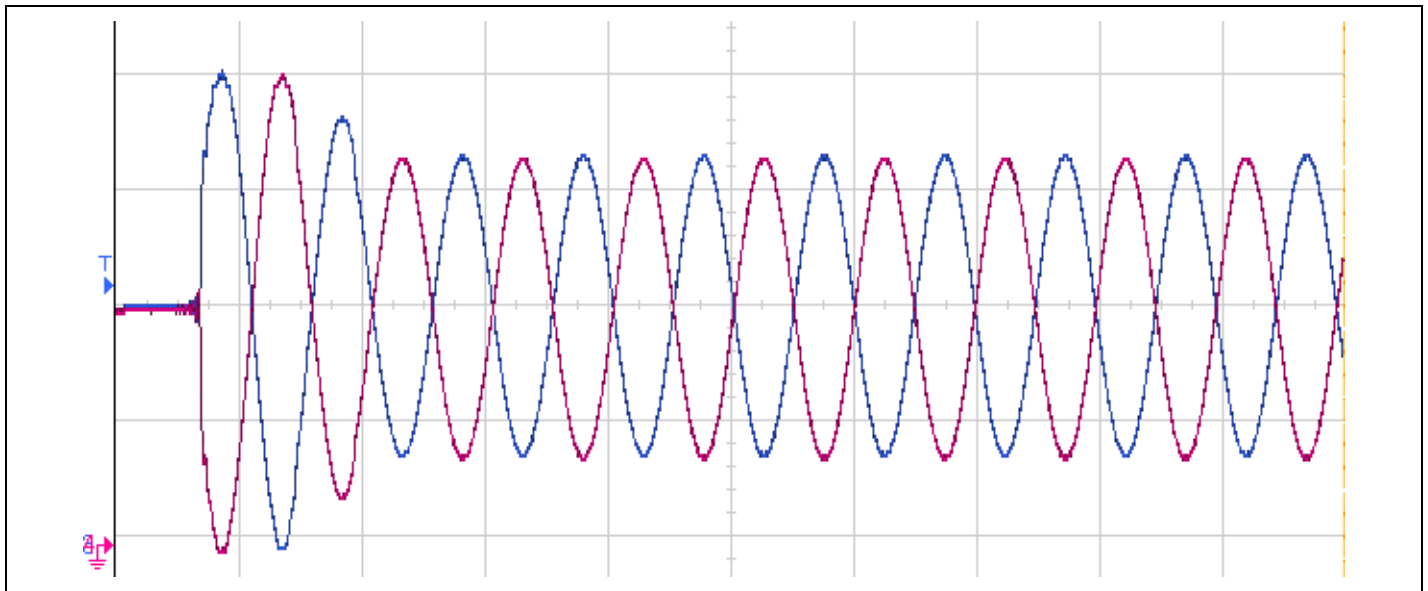


Figure 13 ALC Limiter Waveforms (Gain Reduced)

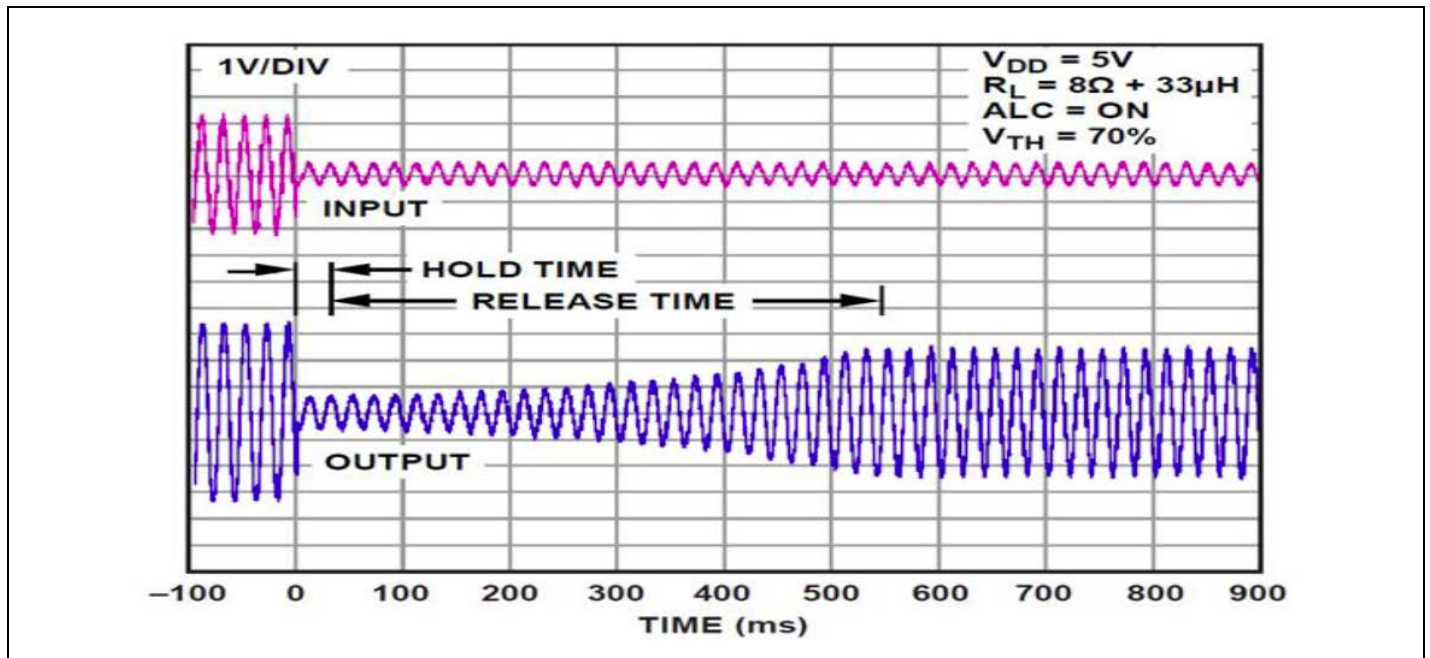


Figure 14 ALC Limiter Waveforms (Gain Released)

5.14.2 Example ALC Values ALC Hold Time

Input signals with different characteristics (such as voice vs. music) may require different settings of the ALC Hold Time parameter for optimum performance. A shorter Hold Time may be useful in voice applications where a faster reaction time helps adjust the volume setting for speakers with different volumes. **Figure 15** shows ALC Input and Output waveforms when no Hold Time is set.

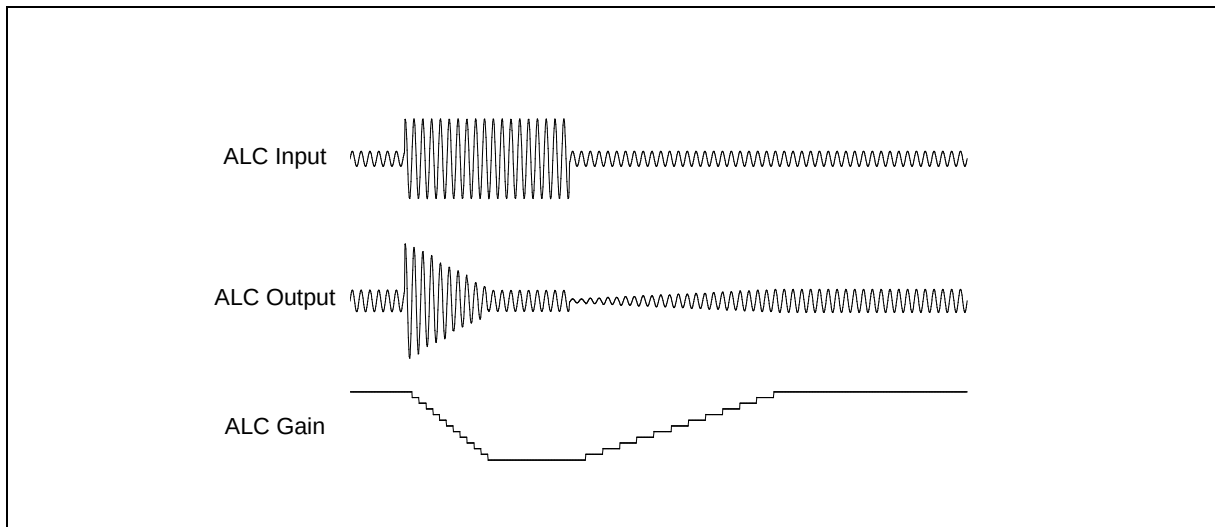


Figure 15 ALC Operation without Hold Time

Increasing the ALC Hold Time prevents the ALC from reacting too quickly to brief periods of silence such as those that may occur in music recordings. **Figure 16** shows ALC Input and Output waveforms

when a Hold Time has been set. The Hold Time parameter is set in the **ALC_CTRL2 ALCHLD REG0x2D[7:4]**. In the example, a Hold Time of 16 msec has been set.

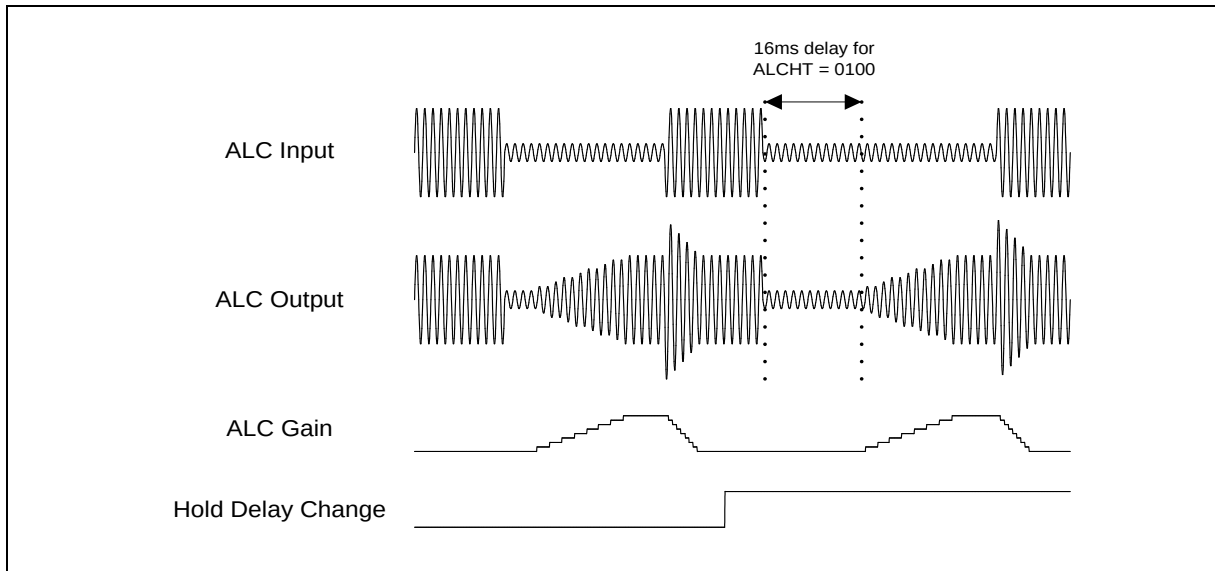


Figure 16 ALC Operation with Hold Time

5.15 Automatic Attenuation

The Automatic Attenuation Circuit reduces the output level and noise at very low output levels. It greatly enhances the Signal-to Noise Ratio (SNR). **Figure 17** shows the Auto Attenuation block diagram. The digital audio signal comes in from the I2S Interface, passes through the high-pass filter, and then to the Digital-to-Analog Converter (DAC), which drives the Class-D modulator which drives the speaker. The DAC input signal feeds into the Auto Attenuate Control circuit that measures signal level and generates the attenuation control signals which set the attenuation level inside the Class-D modulator.

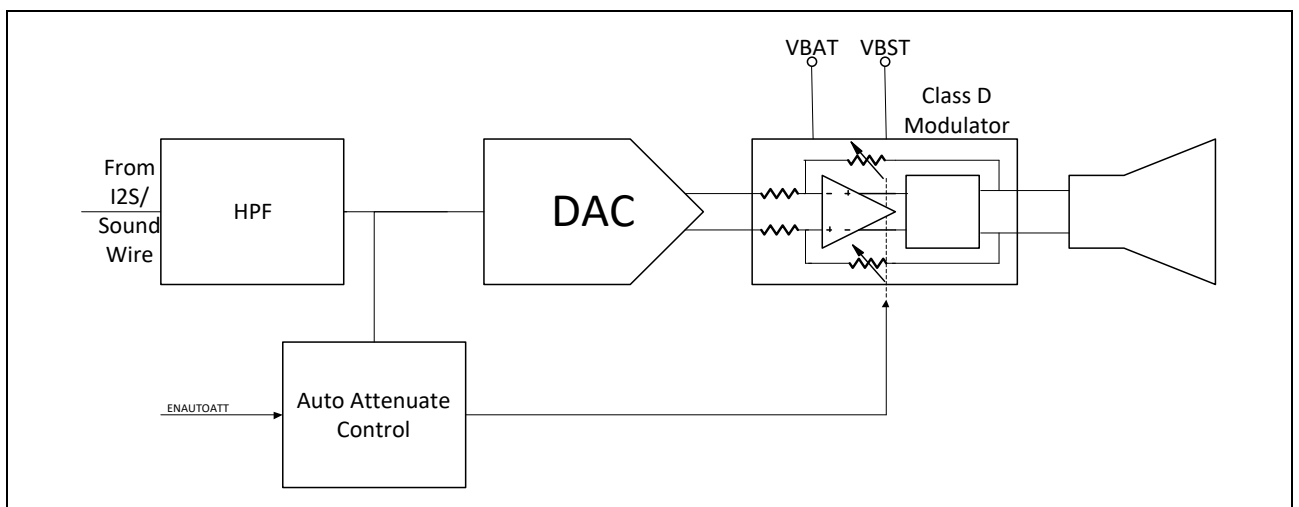


Figure 17 Auto Attenuation Block Diagram

The relation between the input level, the control signal, and the output level is shown in **Table 20**. **ENAUTOATT** (**REG0X2E**) enables the auto attenuator when set to 1 and disables the auto attenuator when set to 0.

Table 20 Auto Attenuate Settings

Input Level	Output Level	
	ENAUTOATT = 1	ENAUTOATT = 0
-123 dBFs	-110.957	-106.255
-120 dBFs	-107.285	-103.255
-117 dBFs	-103.613	-100.255
-114 dBFs	-99.9415	-97.2547
-111 dBFs	-96.2698	-94.2547
-108 dBFs	-92.5981	-91.2547
-105 dBFs	-88.9264	-88.2547
-102 dBFs	-85.2547	-85.2547
-99 dBFs	-82.2547	-82.2547
-96 dBFs	-79.2547	-79.2547
-93 dBFs	-76.2547	-76.2547
-90 dBFs	-73.2547	-73.2547
-87 dBFs	-70.2547	-70.2547
-84 dBFs	-67.2547	-67.2547
-81 dBFs	-64.2547	-64.2547

When the input signal goes down below -105 dBFs (the dBrms level becomes more negative), the auto attenuate control circuit will increment the Control Signal by 1 for every 512 audio samples. Thus, it will take $7 \times 512 = 3584$ audio samples to reach full attenuation if the input signal goes below -123 dBFs. It will take 512 audio samples to reach the next attenuation level if the input signal goes from -106 dBFs to -109 dBFs.

When the input signal level goes up (the dBrms level becomes less negative), the auto attenuate control circuit will decrement the Control Signal by 1 instantly for every input level that it crosses. It would take 0 audio samples to disable the attenuation if the input signal jumps from -124 dBFs to -102 dBFs.

5.16 Digital Microphone Input

As well as supporting analog inputs, the NAU8331 is set up to handle two digital Microphone inputs using the **DMDATA** and the **DMCLK** pins. The **DMDATA** input is able to handle two digital microphones by selecting them alternately for each half of the clock cycle. The clock rate and phase for the digital MIC is configurable. **DMCLK** output selects between the two digital microphones depending on the phase of the clock that has a maximum frequency of 4.8 MHz. (could support maximum frequency of 4.8 MHz for 48K sample rate when OSR is 100. the MCLK will be $4.8 \text{ MHz} \times 500 = 24\text{M}$).

5.17 Device Protection

The NAU8331 includes the following types of device protection:

- Over Current Protection (OCP)
- Supply Over Voltage Protection (OVP)
- Under Voltage Lock Out (UVLO)
- Over Temperature Protection (OTP)
- Clock Termination Protection (CTP)

Over Current Protection is provided in the NAU8331. If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 16.7 μ sec, the output drivers will be disabled for 100 msec. The output drivers will then be enabled again and checked for the short circuit. If the short circuit is still present, the output drivers are disabled after 16.7 μ sec. This cycle will continue until the short circuit is removed. The short circuit threshold is 4.0 A at 3.6 V.

Supply Over Voltage Protection (OVP) is provided in the NAU8331. If the VBST supply voltage reaches 14.1 V, the output drivers will be set to pull down to ground while the NAU8331 control circuitry continues to operate. If the supply drops below 12 V, the output drivers are re-enabled.

Under Voltage Lock Out (UVLO) provides Supply Under Voltage Protection in the NAU8331. If the VBAT supply voltage drops below 2.4 V, the output drivers will be disabled while the NAU8331 control circuitry continues to operate. This will prevent the battery supply from going too low before the host processor can safely shut down the devices on the system. If the supply goes back up, the drivers will be enabled again at 2.55 V. If the supply drops further (below 1.6 V), the internal power-on reset is activated and puts the entire device into the power-down state.

Over Temperature Protection (OTP) is provided in the event of thermal overload. When the internal junction temperature of the device reaches 150°C, the NAU8331 will disable the output drivers. When the device cools down and a safe operating temperature of 130°C has been achieved for at least 100 msec, the output drivers will be enabled again.

Clock Termination Protection (CTP) is provided in the NAU8331. If the clock stops running, the NAU8331 automatically shuts down the Class-D driver and Boost converter if Clock Detection is enabled.

5.18 Power-up and Power-Down Control

When the supply voltage ramps up, the internal power on reset circuit is triggered. At this time, all internal circuits will be set to the power-down state. The device can be enabled by initializing the registers and starting the clocks. Upon starting the clocks, the device will go through an internal power-up sequence in order to minimize 'pops' on the speaker output. The complete power-up sequence requires about 4 msec. The device will power down in about 30 μ sec, when the clocks are stopped.

NOTE: It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize the 'pops' when the clocks are stopped.

5.19 Bypass Capacitors

Bypass capacitors are required to remove the AC ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 10 μ F and 0.1 μ F are sufficient to achieve good performance.

5.20 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. It is better to use low-resistance traces as these devices are driving low impedance loads.

The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

5.20.1 Recommended PCB Footprint

The recommended footprint for the PCB layout for the NAU8331 is provided in **Figure 18**, as viewed from the top of the PCB.

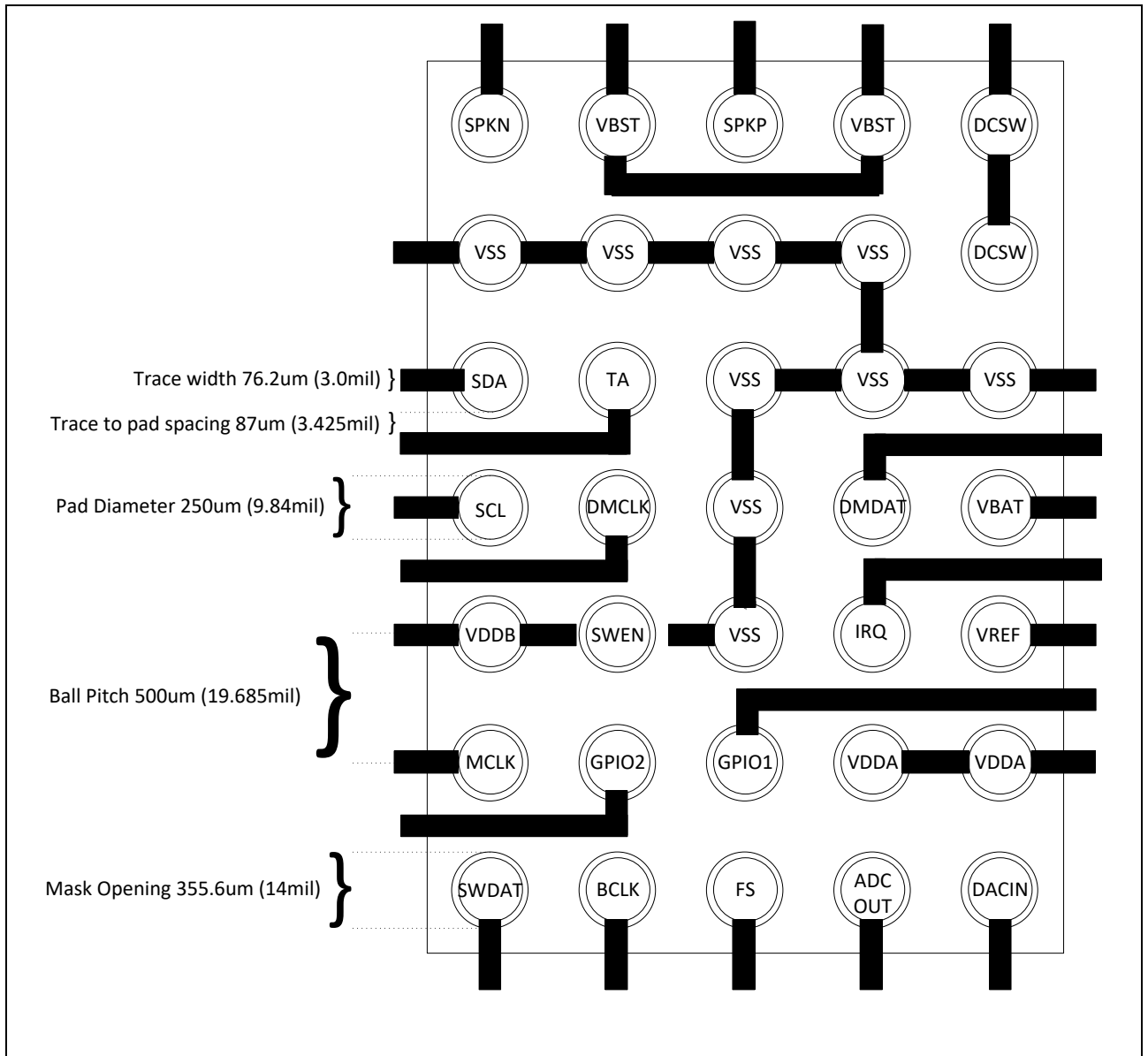


Figure 18 Recommended PCB Footprint

5.20.2 PCB Layout Notes

Given the efficiency of the Boost Converter and the Class-D Amplifier, this requires up to 6 Amperes of peak current through the boost converter inductor. The Boost Converter and the Class-D Amplifier are both high power switching circuits that can cause Electro Magnetic Interference (EMI) when they are poorly connected. Therefore, care must be taken to design the PCB eliminate Electro Magnetic Interference (EMI), reduce IR drops, and maximize heat dissipation.

The following notes are provided to assist product design and enhance product performance:

- Use a VSS plane, preferably on both sides, to shield clocks and reduce EMI
- Maximize the copper to the VSS balls and have solid connections to the plane
- Planes on VDDA, VDDDB & VBAT are optional
- The VBAT connection needs to be a solid piece of copper
- Use thick copper options on the supply layers if cost permits
- The total capacitance on DCSW needs to be as small as possible. Therefore, remove ground and power planes around this node and place the shielded inductor close to DCSW
- Place the VBAT decoupling capacitor close to the other side of the inductor
- Use a big VIA outside the NAU8331 to connect the VBST balls in parallel with the inner trace
- Keep the speaker connections short and thick. Do not use VIAs
- Use a small speaker connector like a wire terminal block (Phoenix Contact)
- Keep the VREF capacitor close to the ball
- For better heat dissipation, use ball VIAs to conduct heat to the other side of the PCB
- Do not use VIA's to connect L1, C1, C2, C3, SPK+ & SPK- to U1. Use a direct top layer copper connection to the balls. Top layer, thick copper is preferred such as 2oz (2.8mil) or thicker.
- VBST balls can have connected on another plane layer.
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane
- The digital IO lines can be shielded between power planes
- The ground return of D0 should run separately back to the NAU8331
- For the traces that run between the balls, follow the guidelines listed in **Figure 18** and see the example illustrated in **Figure 19** and **Figure 20** VBST balls connection (Blue: Top layer; Green: Second Layer).

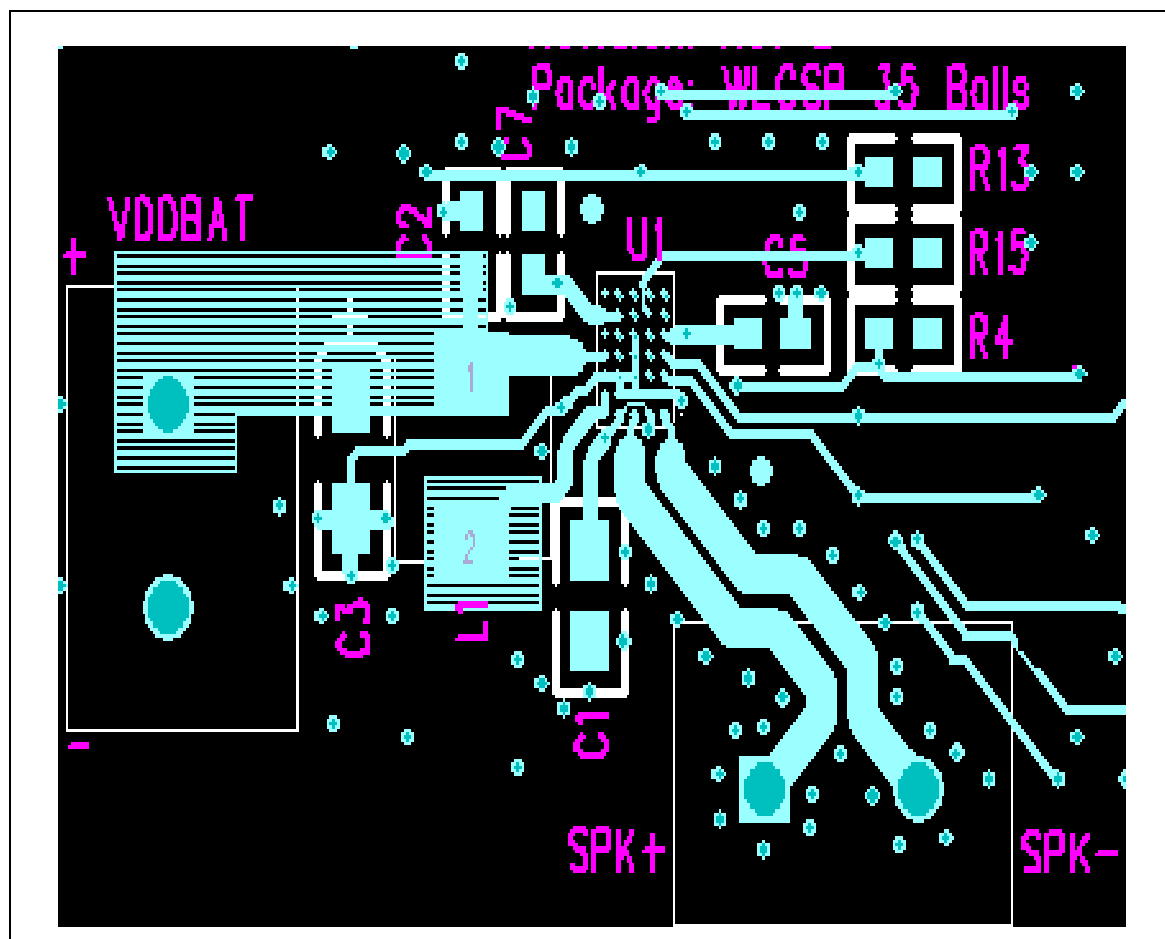


Figure 19 Layout Traces Example

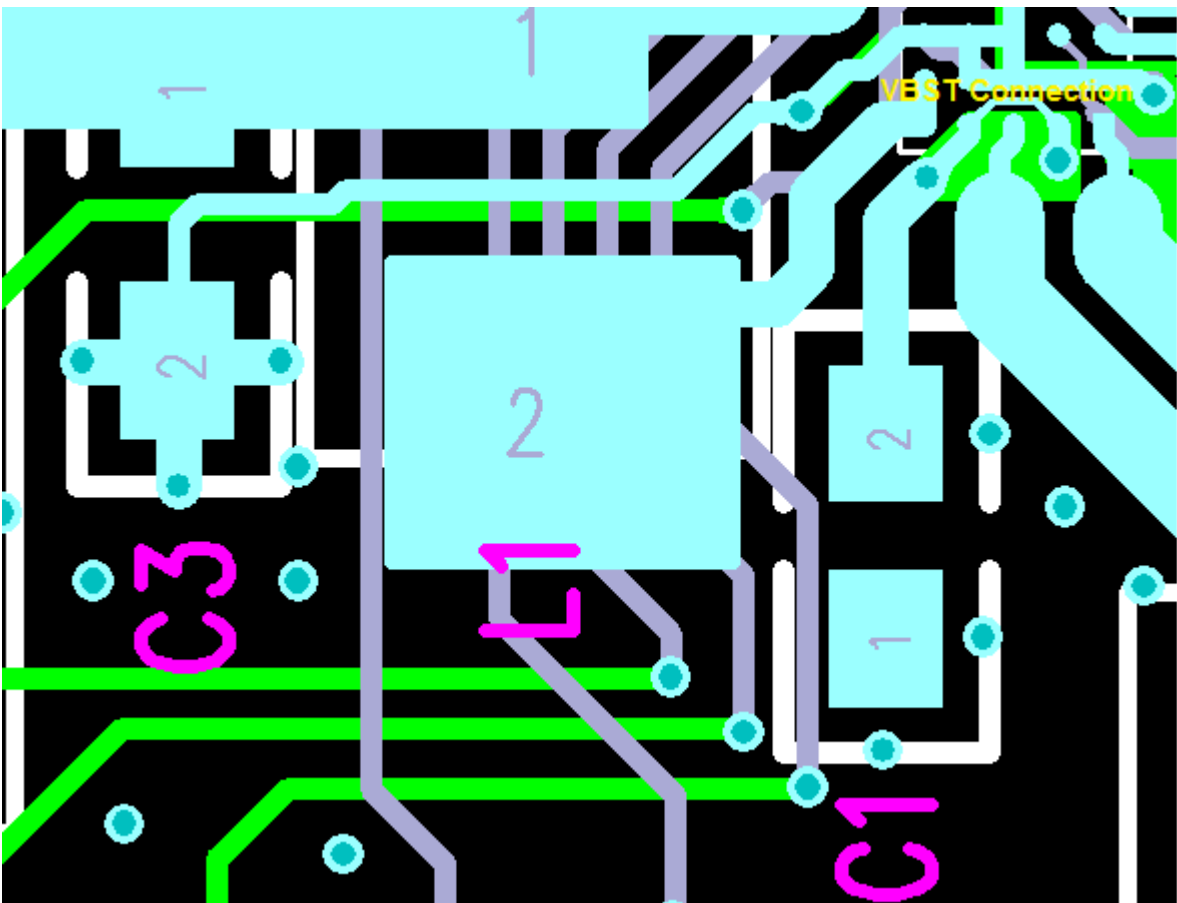


Figure 20 VBST balls connection (Blue: Top layer; Green: Second Layer)

5.21 Filters

The NAU8331 is designed for use without any filter on the output line. However, the NAU8331 may be used with or without various types of filters, depending on the needs of the application.

5.21.1 Class D without Filters

The NAU8331 is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filter-less design is suitable for portable applications where the speaker is very close to the amplifier. In other words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. **Figure 21** illustrates this simple configuration.

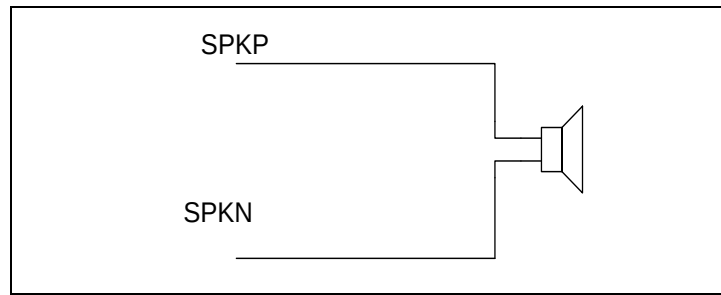


Figure 21 NAU8331 Speaker Connections without Filter

5.21.2 Class D with Filters

In some applications, shorter trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, long traces will cause EMI issues. Several types of filter circuits are available to reduce the EMI effects. These are Ferrite Bead Filters, LC filters, Low-Pass LCR Filters, and High-Pass Filters.

Ferrite Bead Filters are used to reduce high-frequency emissions. The characteristic of a Ferrite Bead Filter is such that it offers higher impedance at high frequencies. For better EMI performance, select a Ferrite Bead Filter which offers the highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. The typical circuit diagram using a Ferrite Bead Filter for each output to the speaker is shown **Figure 22**.

NOTE: Usually, the ferrite beads have low impedance in the audio range, so they will act as pass-through filters in the audio frequency range.

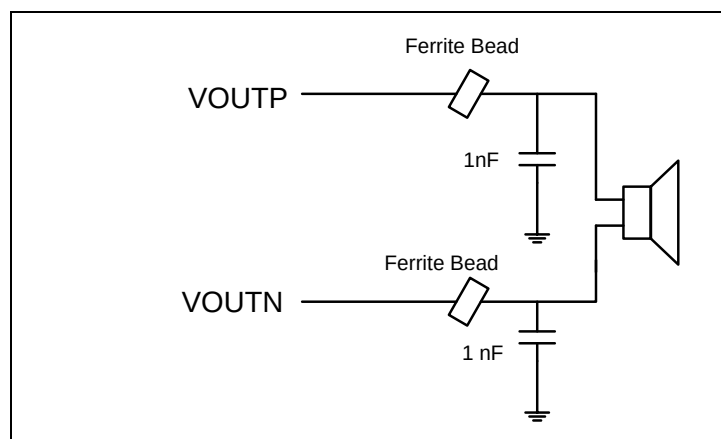


Figure 22 NAU8331 Speaker Connections with Ferrite Bead Filters

LC Filters are used to suppress low-frequency emissions. The diagram in **Figure 23** shows the NAU8331 outputs connected to the speaker with an LC Filter circuit. R_L is the resistance of the speaker coil.

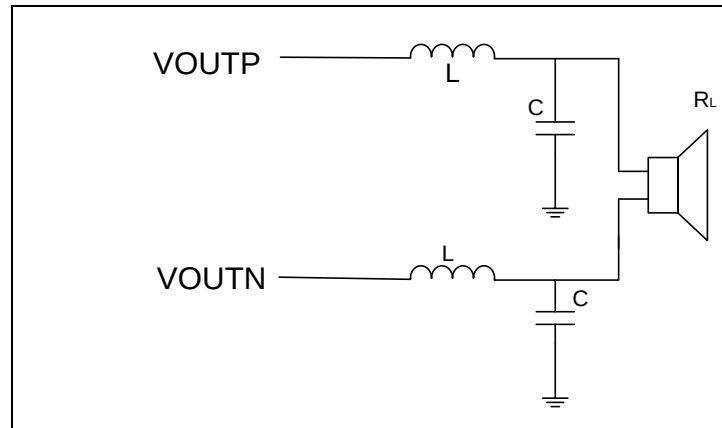


Figure 23 NAU8331 Speaker Connections with LC Filters

Low-Pass LCR Filters may also be useful in some applications where long traces or wires to the speakers are used. **Figure 24** shows the speaker connections using standard Low-Pass LCR Filters.

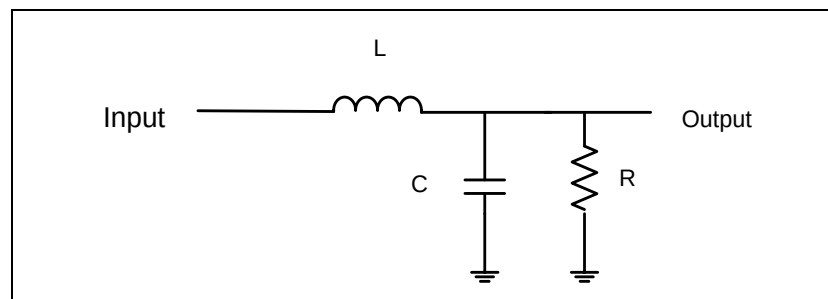


Figure 24 NAU8331 Speaker Connections with Low-Pass Filters

The following equations apply for critically damped ($\zeta = 0.707$) standard Low-Pass LCR Filters:

$$2\pi f_c = \frac{1}{\sqrt{LC}} \quad f_c \text{ is the cut-off frequency}$$

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

NOTE: The L and C values for differential configuration can be calculated by duplicating the single-ended configuration values and substituting $R_L = 2R$.

High-Pass Filters may also be useful in some applications. There is a High-Pass Filter for each ADC Channel and each DAC Channel. The High-Pass Filters may be enabled by setting **HPF_EN** [REG0X12\[15\]](#), [\[13\]](#), and [\[5\]](#). The High-Pass Filter has two operation modes that apply to both channels simultaneously. In the Audio Mode, the filter is a simple first-order DC blocking filter, with a cut-off frequency of 3.7 Hz. In the Application-Specific Mode, the filter is a second-order audio frequency filter, with a programmable cut-off frequency. The programmable filter mode may be enabled by setting **HPF_APP** [REG0X12\[14\]](#), [\[9\]](#), and [\[4\]](#).

Table 21 identifies the cut-off frequencies with different sample rates.

Table 21 High-Pass Filter Cut-Off Frequencies

HPFCUT	Sample Rate in KHz (FS)							
	REG_SRATE= 3'b000		REG_SRATE= 3'b001		REG_SRATE= 3'b010		REG_SRATE= 3'b011	
	8	12	16	24	32	48	64	96
000	87	130	87	130	87	130	87	130
001	103	155	103	155	103	155	103	155
010	132	198	132	198	132	198	132	198
011	165	248	165	248	165	248	165	248
100	207	311	207	311	207	311	207	311
101	265	398	265	398	265	398	265	398
110	335	503	335	503	335	503	335	503
111	409	614	409	614	409	614	409	614

6 Control Interfaces

The NAU88L24 includes a serial control bus that provides access to all of the device control registers and may be configured as a 2-wire interface that conforms to industry standard implementations of the I2C serial bus.

6.1 2-Wire-Serial Control Mode (I²C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU88L24 can function only as a slave device when in the 2-wire interface configuration.

6.2 2-Wire Protocol Convention

To initiate communication, all 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH.

Following a START condition, the master must output a device address byte consisting of a 7-bit device address, and a Read/Write control bit in the LSB of the address byte. To read from the slave device, the R/W bit must be set to 1. To initiate a write to the slave device, the R/W bit must be 0. If the device address matches the address of a slave device, the slave will output an acknowledgement bit.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits and during the ninth clock cycle, the receiver (slave) pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

To terminate a read/write session, all 2-Wire interface operations must end with a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

Application Notes:

The NAU88L24 is permanently programmed with "0011010" as the Device Address.

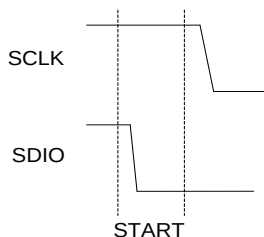


Figure 25 Valid START Condition

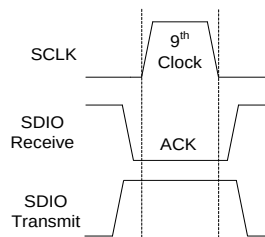


Figure 26 Valid Acknowledge

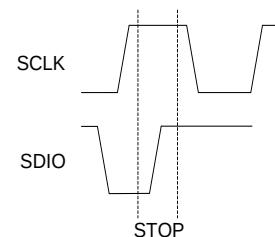


Figure 27 Valid STOP Condition

6.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more data bytes as seen in Figure 28. These instructions consist of the Address byte and two Control Address bytes that precede the START condition and are followed by the STOP condition. Figure 29 shows the data bus and the corresponding clock cycles.

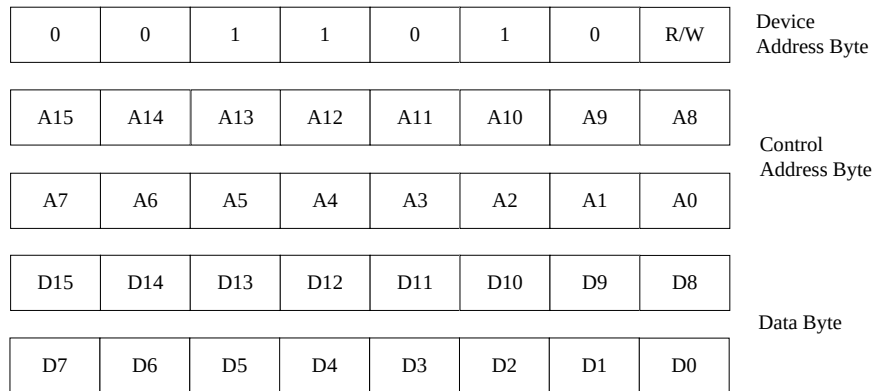


Figure 28 Slave Address Byte, Control Address Byte, and Data Byte

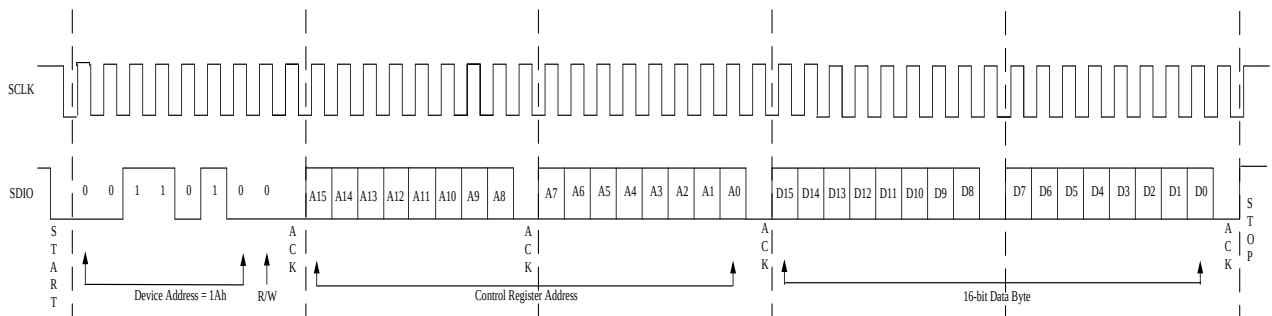


Figure 29 2-Wire Write Sequence

6.4 2-Wire Read Operation

A Read operation consists of the three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, Device Address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the NAU88L24 which of its control registers is going to be accessed.

After this, the NAU88L24 will respond with an ACK as it accepts the Control Register Address that the master is transmitting to it. After the Control Register Address has been sent, the master will send a second START condition and Device address but with R/W = 1.

After the NAU88L24 recognizes its Device Address the second time, it will transmit an ACK followed by a two byte value containing the 16 bits of data in the NAU88L24 control registers requested by the master. During this phase, the master generates an ACK with each byte of data transferred.

After the two bytes have been transmitted, the master will send a STOP condition ending the read phase. If no STOP condition is received, the NAU88L24 will automatically increment the target Control Register Address and then start sending the two bytes of data for the next register in the sequence. This will continue as long as the master continues to send ACK signals. Once the target register reaches 0xFFFF, it will send the associated data then roll over to 0x0000 and continue as before.

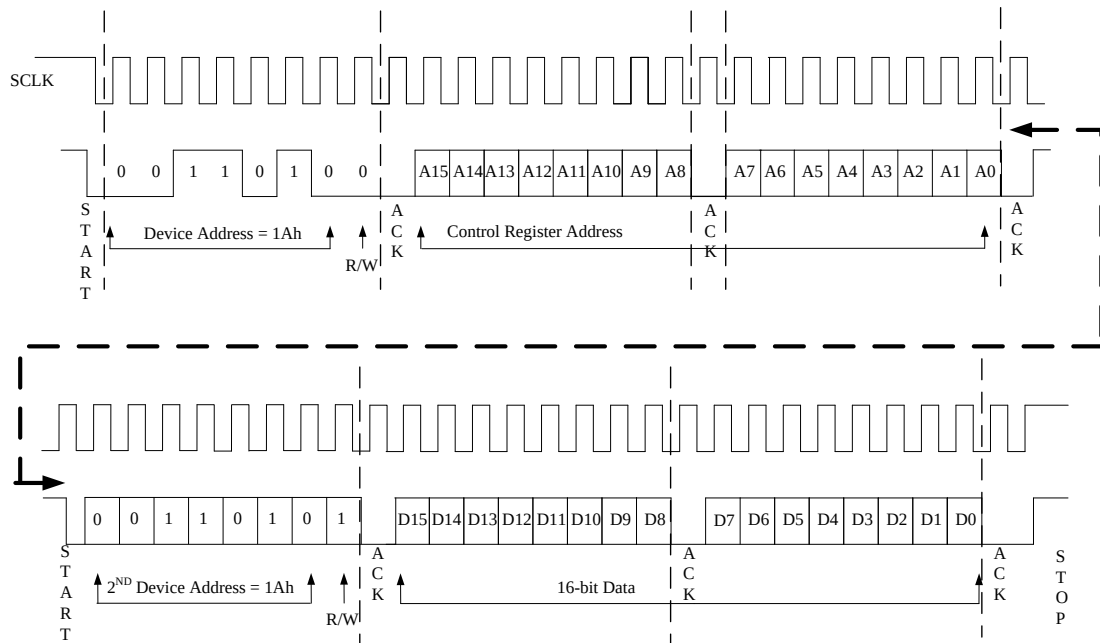


Figure 30 2-Wire Read Sequence

6.5 Digital Serial Interface Timing

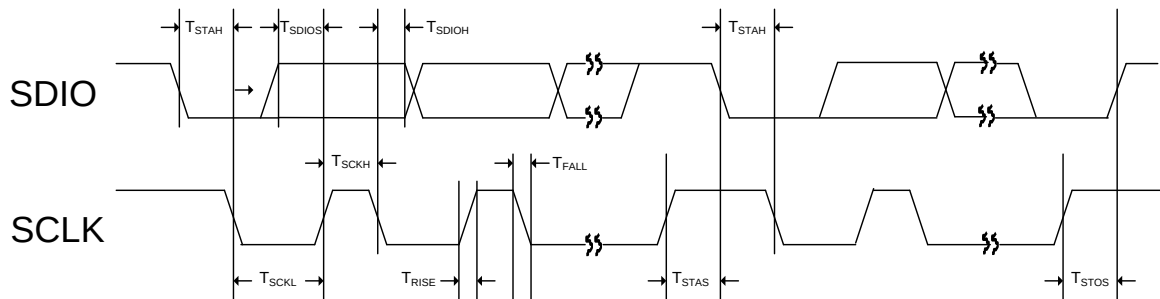


Figure 31 Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T _{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T _{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T _{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T _{SCKH}	SCLK High Pulse Width	600	-	-	ns
T _{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T _{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T _{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T _{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T _{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

6.6 Software Reset

The NAU88L24 and all of its control registers can be reset to default initial conditions by writing any value to REG0X00 twice using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their power-on default values.

7 Control and Status Registers

The NAU8331 includes an I2C Control Interface as well as an I2S/PCM Audio Interface. The following sections describe the Control and Audio Interfaces and registers.

7.1 Digital Control Interface

The NAU8331 uses an I2C/SPI Interface with programmable addresses. The I2C address = 0x10, 0x11, 0x40, 0x41.

7.2 Digital Audio Interface

The NAU8331 can be configured as either the Master or the Slave, by setting register **I2S_PCM_CTRL2 MS0 REG0XE[3]** to 1 for Master Mode or setting it to 0 for Slave Mode. Slave Mode is the default if this bit is not written. In Master Mode, NAU8331 outputs both Frame Sync (FS) and the audio data Bit Clock (BCLK) and has full control of the data transfer. In Slave Mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; and ADCOUT clocks out ADC data, while DACIN clocks in data for the DACs.

When not transmitting data, ADCOUT pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the Time Slot function is enabled, there are additional output state modes, including controlled tri-state capability (see **Section 9.2.9**).

The NAU8331 has one DAC channel and two ADC channels. The ADC left and right channel data could be swapped in the I2S Interface by setting register **I2S_PCM_CTRL1 ADCPHS0 REG0XD[5]** to 1.

When **ADC_RATE_I2S_MODE REG0X28[15]** or **ADC_RATE_DMIC_MODE REG0X28[7]** is set to 1, the I2S Interface ADC path will transmit normal audio data. If both of them are set to 0, the ADC path will transmit I/V Sense data and SAR ADC data, which could be in either signed or unsigned format by setting **TDM_CTRL_UNSIGN_IV REG0XC[9]** to be 0 or 1, respectively. The I2S Interface DAC path will transmit normal audio data at any situation.

The NAU8331 supports four port data lengths: 16, 20, 24, and 32 bits by setting **I2S_PCM_CTRL1 WLEN0 REG0XD[3:2]**. The chip also supports 8-bit word length for Compounding Mode operation by setting **I2S_PCM_CTRL1 CMB8_0 REG0XD** to 1.

The NAU8331 supports eight audio formats: I2S, Left Justified, TDM I2S, TDM Left Justified, PCM A, PCM B, PCM Offset, and PCM Time Slot.

When operated in the TDM I2S, or TDM Left Justified mode and in all PCM modes, the NAU8331 supports 8-channel data transmission on both ADC and DAC paths simultaneously. **TDM_CTRL_TDM REG0XC[15]** should be set = 1 if using TDM I2S, or TDM Left Justified modes.

Table 22 Digital Audio Interface Mode Settings

PCM Mode	I2S_PCM_CTRL1 AIFMT0 REG0XD[1:0]	I2S_PCM_CTRL1 LRP0 REG0XD[6]	I2S_PCM_CTRL2 PCM_TS_EN0 REG0XE[10]	TDM_CTRL PCM_OFFSET MODE_CTRL REG0XC[14]
Left Justified	01	0	0	0
I2S	10	0	0	0
PCM A	11	0	0	0
PCM B	11	1	0	0
PCM Offset	11	Don't care	0	1
PCM Time Slot	11	Don't care	1	0

7.2.1 Left-Justified Audio Data

In Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is HIGH, Channel 0 data are transmitted; when FS is LOW, Channel 1 data are transmitted. This can be seen in **Figure 32**.

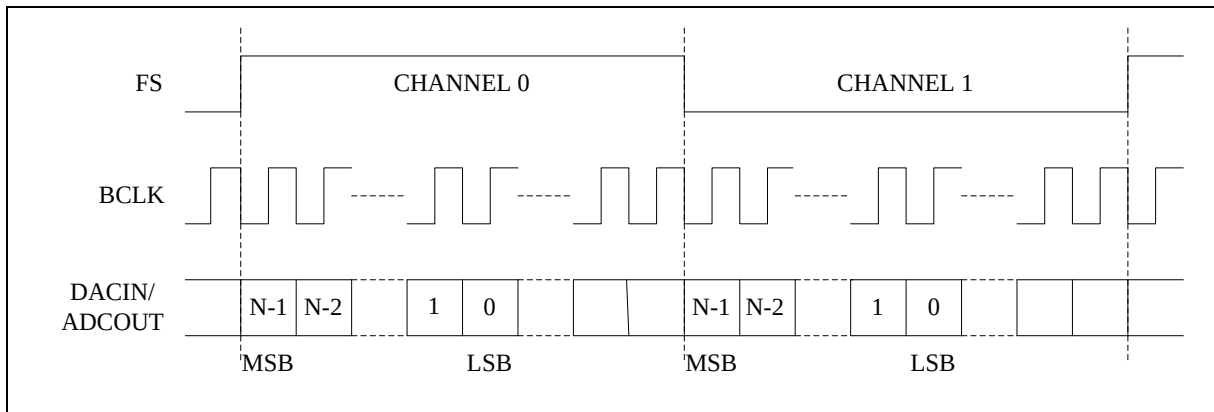


Figure 32 Left-Justified Audio Data

7.2.2 I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Left Channel data are transmitted; when FS is HIGH, Right Channel data are transmitted. This can be seen in **Figure 33**. Note: In standard I2S mode the V-sense channel has one sample delay with respect to the I-sense channel.

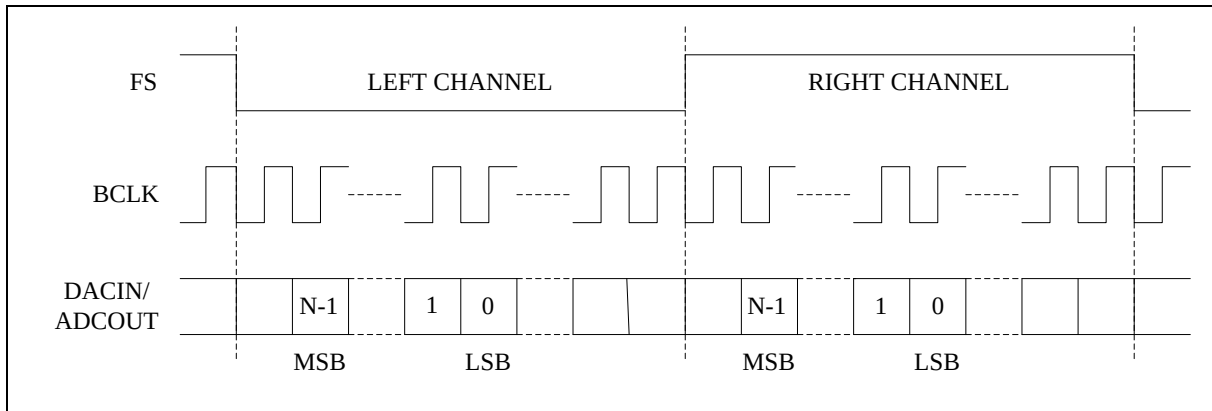


Figure 33 I2S Audio Data

7.2.3 TDM Left-Justified Audio Data

In TDM Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is LOW, Channel 1 data are transmitted, then Channel 3, 5, and 7 data are transmitted; when FS is HIGH, Channel 0 data are transmitted, then Channel 2, 4, and 6 data are transmitted. This is shown in **Figure 34**.

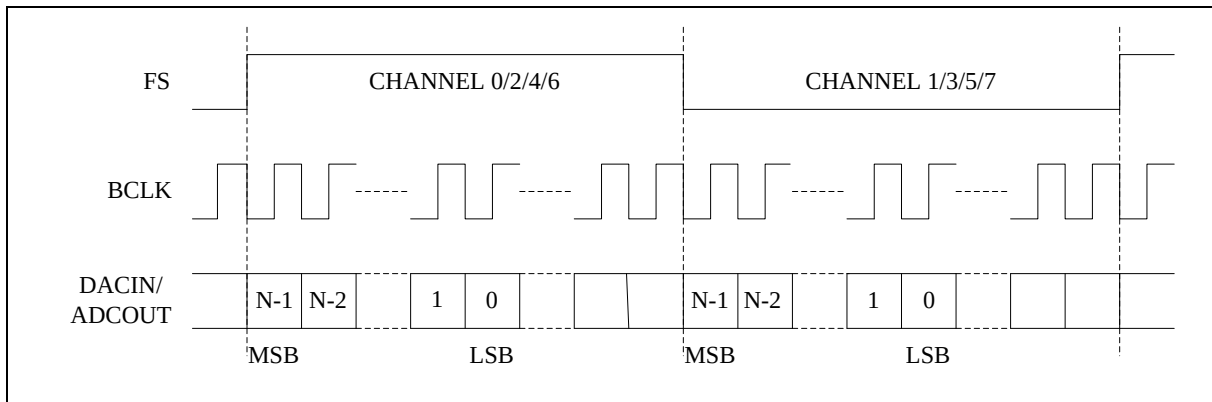


Figure 34 TDM Left-Justified Audio Data

7.2.4 TDM I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Channel 0 data are transmitted, then Channel 2, 4, and 6 data are transmitted; when FS is HIGH, Channel 1 data are transmitted, then Channel 3, 5, and 7 data are transmitted. This is shown in **Figure 35**.

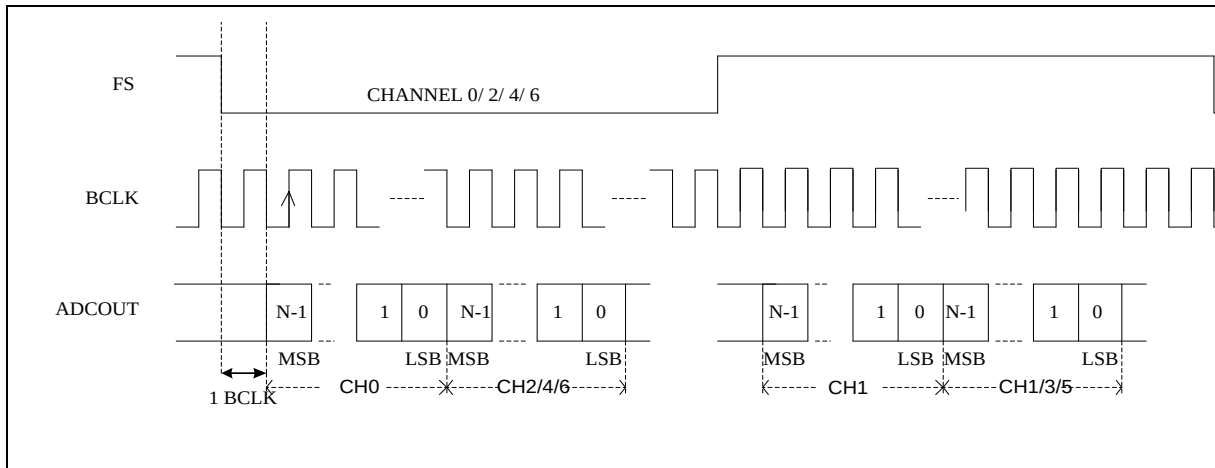


Figure 35 TDM I2S Audio Data

7.2.5 PCM A Audio Data

In PCM A Mode, Channel 0 data are transmitted first, followed sequentially by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in **Figure 36**.

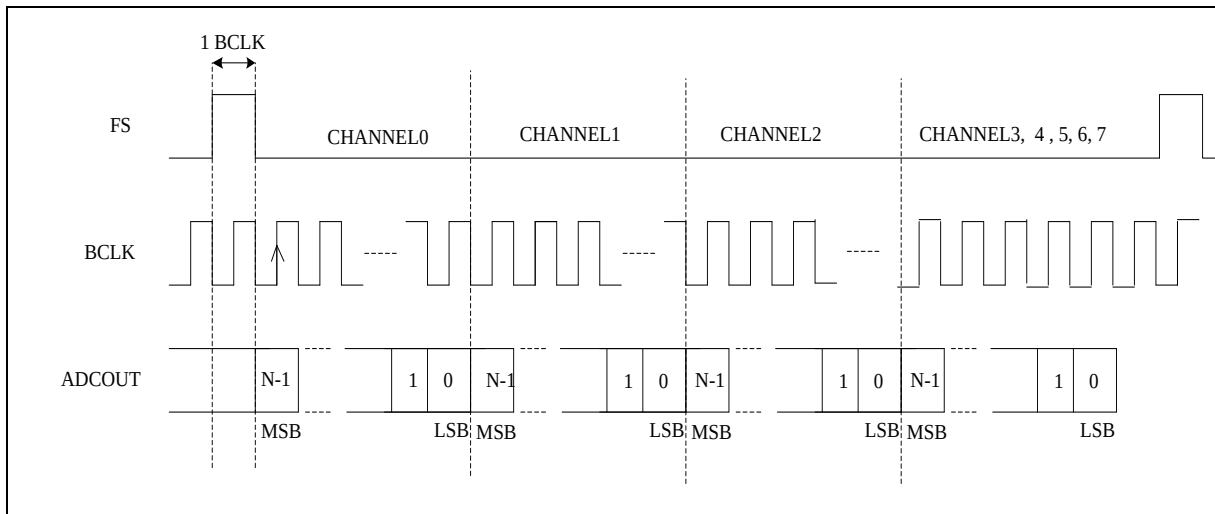


Figure 36 PCM A Audio Data

7.2.6 PCM B Audio Data

In PCM B Mode, Channel 0 data are transmitted first, followed immediately by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the Channel 1 MSB is clocked on the next SCLK after the Channel 0 LSB. This is shown in **Figure 37**.

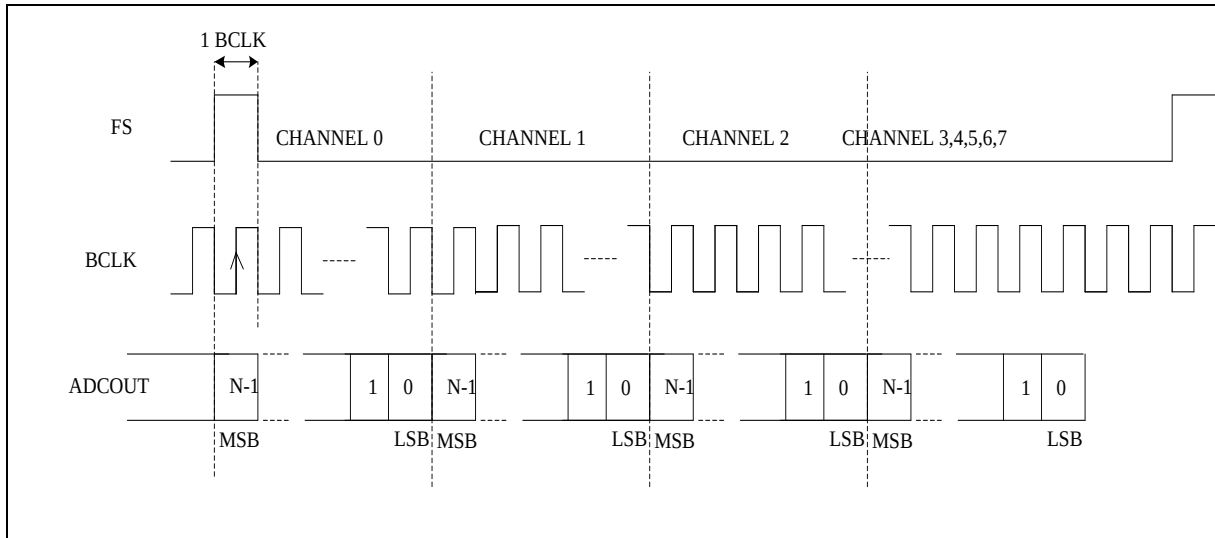


Figure 37 PCM B Audio Data

7.2.7 PCM Time Slot Audio Data

PCM Time Slot Mode is used to delay the time at which the DAC and/or ADC data are clocked. This can be useful when multiple NAU8331 chips or other devices share the same audio bus. This will allow the audio from the chips to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS); however, in PCM Time Slot Mode, the audio data can be delayed by setting **LEFT TIME SLOT TSLOT_L0 REG0XF[9:0]** and **RIGHT TIME SLOT TSLOT_R0 REG0X10[9:0]** for the left and right channels, respectively. **I2S_PCM_CTRL2 PCM_TS_EN0 REG0XE[10]** needs to be set to 1. These delays can be seen before the MSB in **Figure 38**.

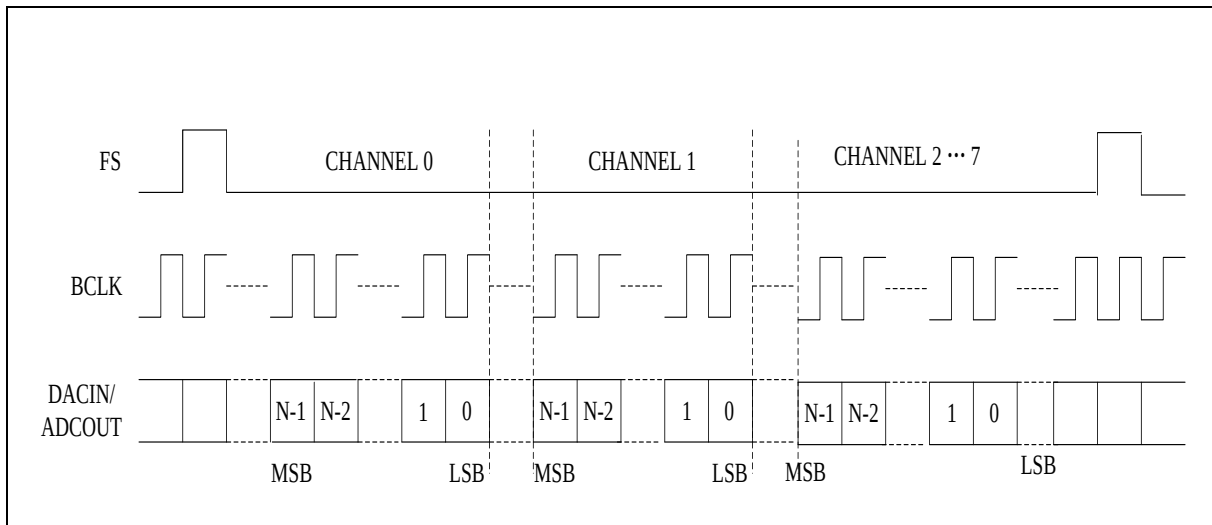


Figure 38 PCM Time Slot Audio Data

APPLICATION NOTES:

- When using the NAU8331 with other driver chips, the ADCOUT pin can be set to pull up or pull down by enabling [I2S_PCM_CTRL2_ADCOUT0_PE_REG0XE\[6\]](#) and selecting up or down with [I2S_PCM_CTRL2_ADCOUT0_PS_REG0XE\[5\]](#). This allows for wired-OR type bus sharing. If both are set to 0, ADCOUT is high impedance, except when transmitting channel audio data. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent time slots with reduced risk of bus- driver contention.
- By default, [I2S_PCM_CTRL2_ADCOUT0_OE_REG0XE\[4\]](#) sets the ADCOUT pin in high impedance state. This condition needs to be disabled in order to drive the data line.

7.2.8 PCM Time Offset Audio Data

PCM Time Offset Mode is used to delay the time at which the DAC and/or ADC data are clocked. This increases the flexibility of the NAU8331 for use in a wide range of system designs. One key application of this feature is to enable multiple NAU8331 chips or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data. [TDM_CTRL_PCM_OFFSET_MODE_CTRL_REG0XC\[14\]](#) must be set to 1 for this application.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS). In this mode, audio data are delayed by a delay count specified in the device control registers. The Channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in [LEFT_TIME_SLOT_TSLOT_L0_REG0XF\[9:0\]](#). The subsequent channel's MSB is clocked on the next BCLK after the LSB of the previous channel. This can be seen in **Figure 39**.

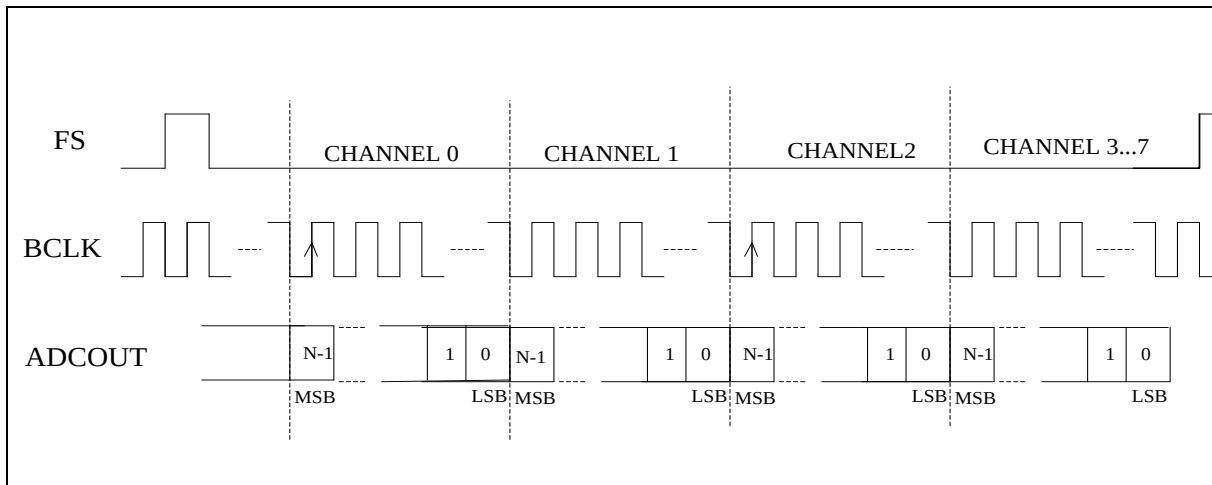


Figure 39 PCM Time Offset Audio Data

7.2.9 I/V Sense Data Stereo Mode

I/V Sense Data Stereo Mode is used to transmit I/V Sense data and SAR ADC data in two ADC channels. This mode may be operated in all ten audio formats and three port word lengths when [ADC_RATE I2S_MODE REG0X28 \[15\]](#) and [ADC_RATE DMIC_MODE REG0X28\[7\]](#) are both set to 0 and [TDM_CTRL PINGPONG_MODE REG0XC\[8\]](#) is also set to 0.

The ADC path Left and Right Channel transmission data could be swapped in the I2S Interface by setting register [I2S_PCM_CTRL1 ADCPHS0 REG0XD\[5\]](#) to 1. By default, the Left Channel will transmit V Sense data and SAR ADC output type; the Right Channel will transmit I Sense data and SAR ADC output messages. The exact bit definition depends on the port word length. Refer to **Table 23** for I/V Sense port word length options. See **Figure 40**, **Figure 41**, and **Figure 42** for the 16-, 24-, and 32-bit timing diagrams.

Table 23 I/V Sense Data Stereo Mode Settings

16-bit	ADCOUT[16:0]			
Left Channel	16-bit V Sense Data			
Right Channel	16-bit I Sense Data			
24-bit	ADCOUT[24:8]	ADCOUT[7:4]	ADCOUT[3:0]	
Left Channel	16-bit V Sense Data	4-bit Preamble	4-bit Type	
Right Channel	16-bit I Sense Data	8-bit Message[7:4]	8-bit Message [3:0]	
32-bit	ADCOUT[32:16]	ADCOUT[16:12]	ADCOUT[11:8]	ADCOUT[3:0]
Left Channel	16-bit V Sense Data	4-bit Preamble	4-bit Type	8-bit Consecutive Zero
Right Channel	16-bit I Sense Data	8-bit Message [7:4]	8-bit Message [3:0]	8-bit Consecutive Zero

The Preamble is a fixed value set to be 4-bit 1010.

The 4-bit type and 8-bit data corresponding chart is shown in **Table 24**. The 8 bit message can also retrieve from Reg0x20 [SAR_ADC_OUT_01](#) and Reg0x21 [SAR_ADC_OUT_23](#).

Table 24 4-Bit Type and 8-Bit Message Values

4-bit Type	8-bit Message
0000	Tj
0001	Ta
0011	VBAT

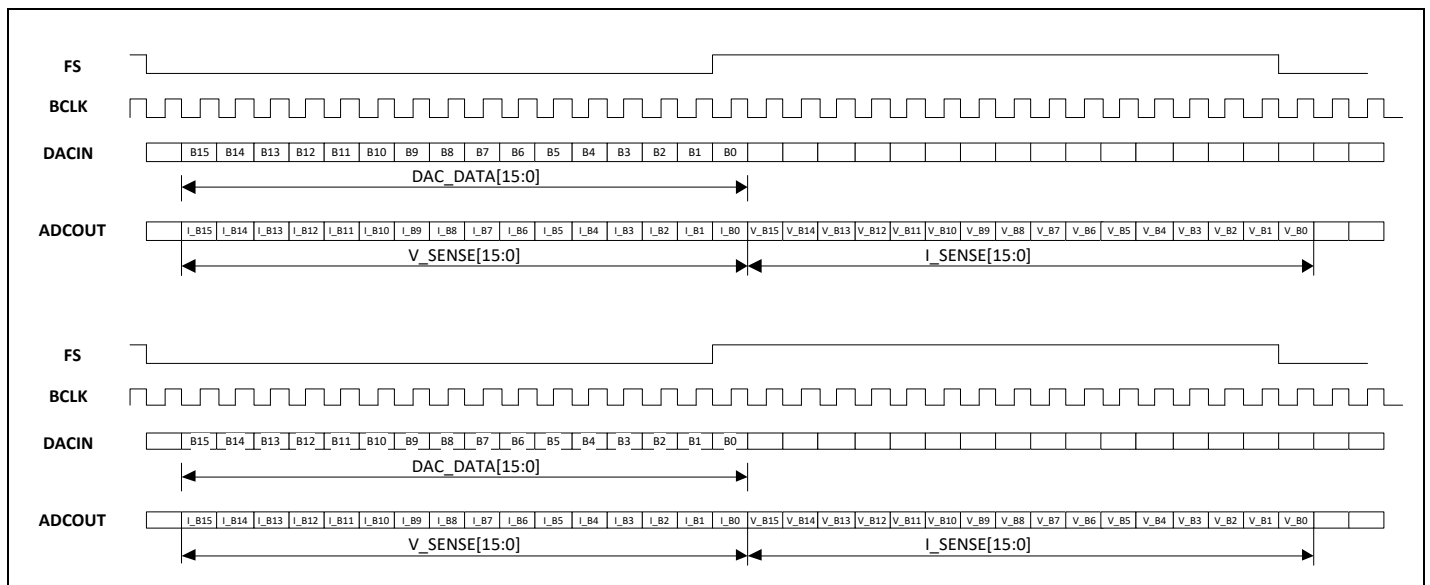


Figure 40 16-Bit I2S Stereo Mode Timing Diagram

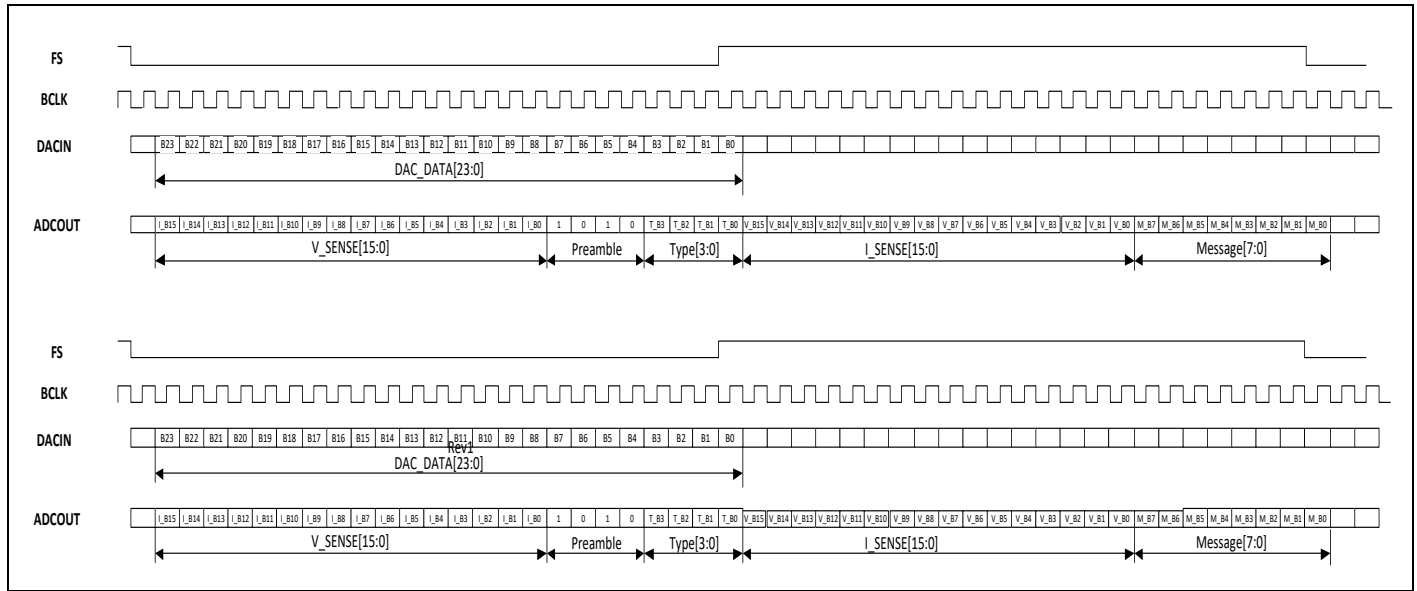


Figure 41 24-Bit I2S Stereo Mode Timing Diagram

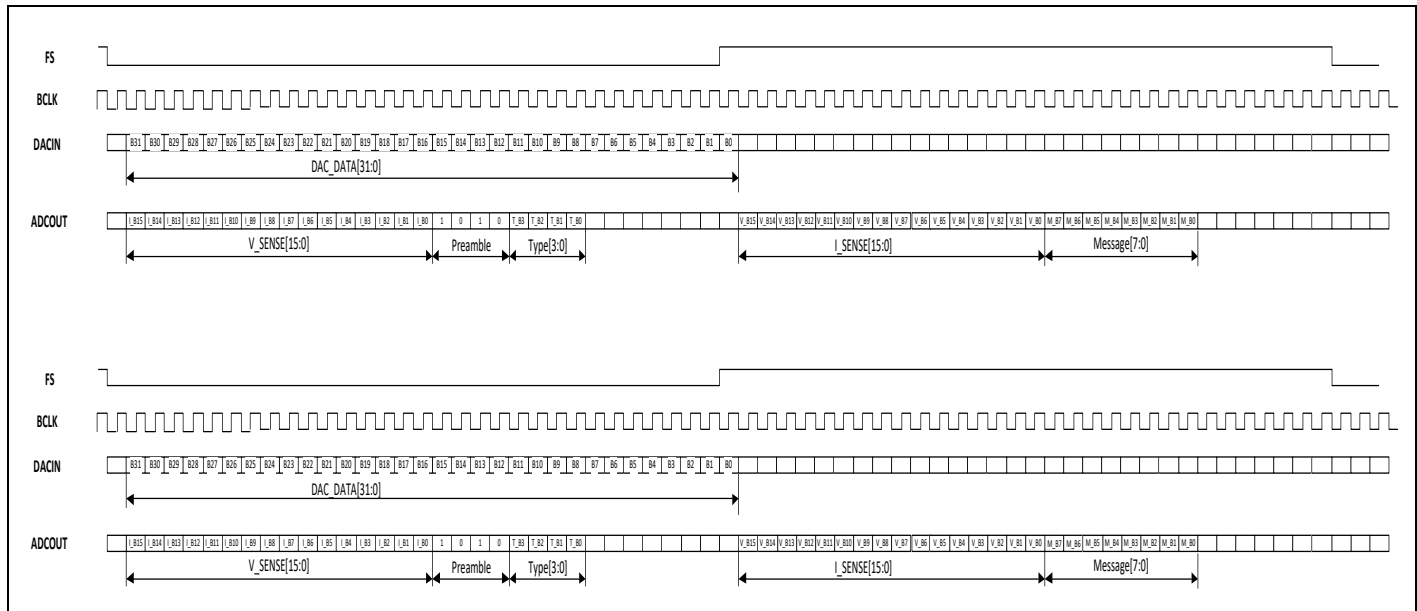


Figure 42 32-Bit I2S Stereo Mode Timing Diagram

7.2.10 I/V Sense Data Ping Pong Mode

I/V Sense Data Ping Pong Mode is used to transmit I/V Sense data and SAR ADC data in a single ADC channel. This mode may be operated in all ten audio formats and three port word lengths when **ADC_RATE I2S_MODE REG0X28[15]** and **ADC_RATE DMIC_MODE REG0X28 [7]** are both set to 0 and **TDM_CTRL PINGPONG_MODE REG0XC[14]** is set to 1.

The ADC path Left or Right Channel will transmit I Sense data and SAR ADC output type in one FS time frame and transmit V Sense data and SAR ADC output messages in the next FS time frame, alternately. The exact bit definition depends on the port word length. Refer to **Table 25** for I/V Sense Ping Pong

Mode port word length options. See **Figure 43**, **Figure 44**, and **Figure 45** for the 16-, 24-, and 32-bit timing diagrams for I/V Sense Ping Pong Mode.

Table 25 I/V Sense Data PingPong Mode Settings

16-bit	ADCOUT[16:0]			
FS Phase I	16 bit V Sense Data			
FS Phase II	16 bit I Sense Data			
24-bit	ADCOUT[24:8]	ADCOUT[7:4]	ADCOUT[3:0]	
FS Phase I	16-bit V Sense Data	4-bit Preamble	4-bit Type	
FS Phase II	16-bit I Sense Data	8-bit Message[7:4]	8-bit Message [3:0]	
32-bit	ADCOUT[32:16]	ADCOUT[16:12]	ADCOUT[11:8]	ADCOUT[7:0]
FS Phase I	16-bit V Sense Data	4-bit Preamble	4-bit Type	8- bit consecutive zero
FS Phase II	16-bit I Sense Data	8-bit Message [7:4]	8-bit Message [3:0]	8- bit consecutive zero

The Preamble is a fixed value set to be 4-bit 1010.

The 4-bit type and 8-bit data corresponding chart is shown in **Table 26**. The 8 bit message can also retrieve from Reg0x20 [SAR_ADC_OUT_01](#) and Reg0x21 [SAR_ADC_OUT_23](#).

Table 26 4-Bit Type and 8-Bit Message Values

4-bit Type	8-bit Message
0000	Tj
0001	Ta
0011	VBAT

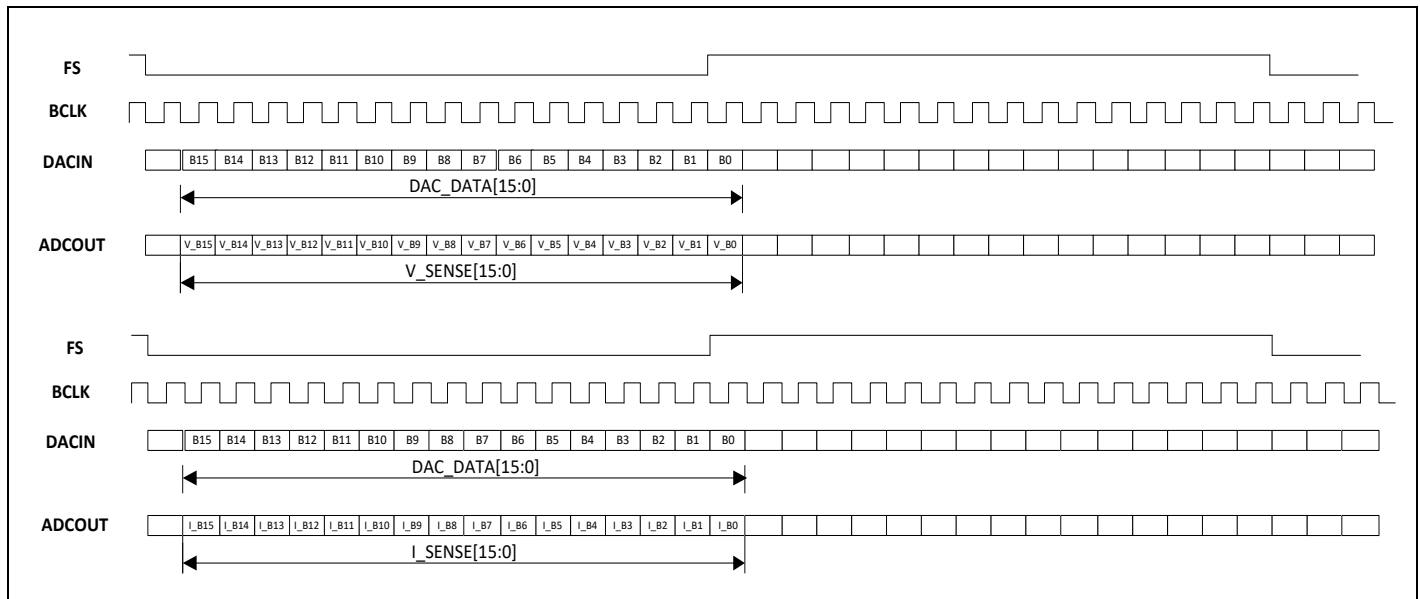


Figure 43 16-Bit I2S PingPong Mode Timing Diagram

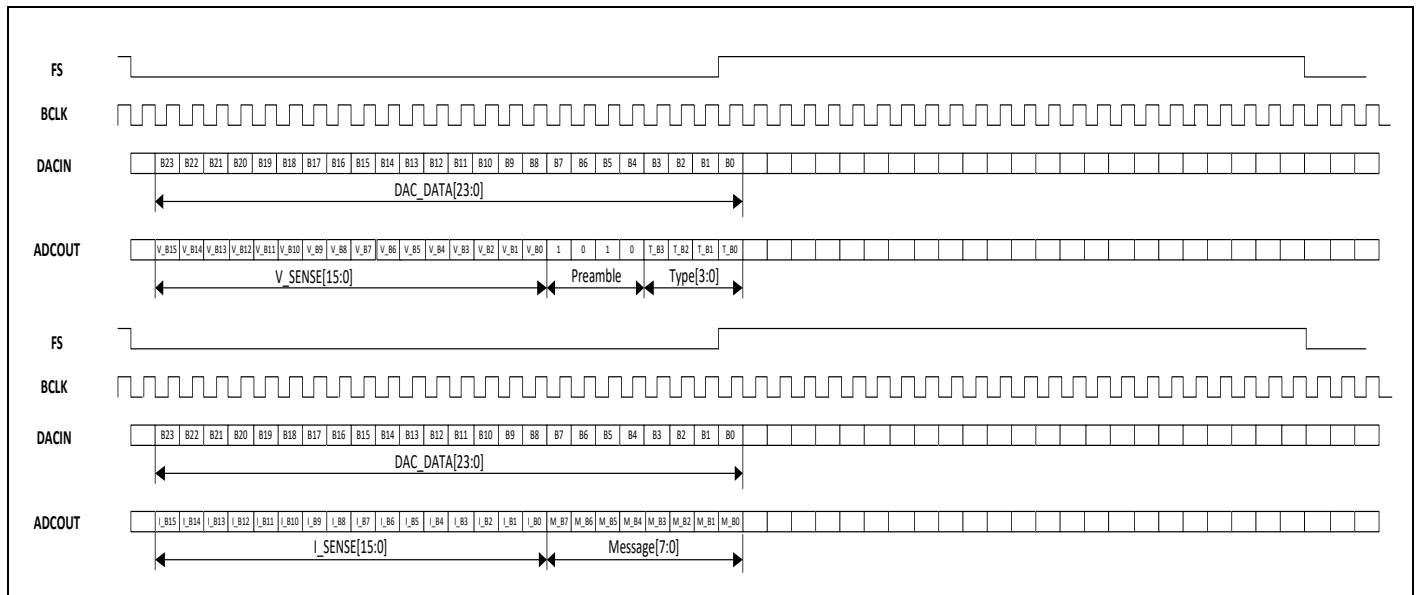


Figure 44 24-Bit I2S PingPong Mode Timing Diagram

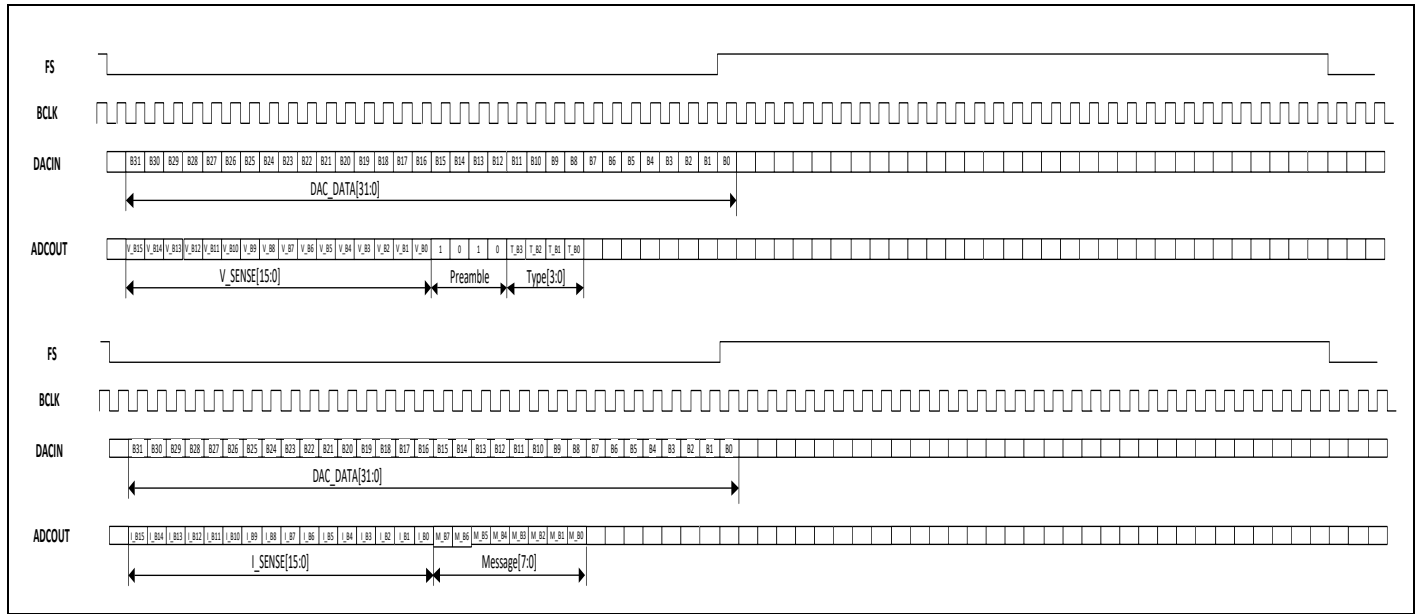


Figure 45 32-Bit I2S PingPong Mode Timing Diagram

7.2.10.1 I/V Sense Data Ping Pong Mode using in TDM Mode

For multiple channels more than stereo, I/V Sense Data Ping Pong Mode is used to transmit I/V Sense data and SAR ADC data in a single ADC channel by using TDM mode. This condition may be operated in 24 bits or 32 bits port word lengths when **ADC_RATE I2S_MODE REG0X28[15]** and **ADC_RATE DMIC_MODE REG0X28[7]** are both set to 0 and **TDM_CTRL TDM REG0XC [15]** and **PINGPONG MODE REG0XC[14]** are set to 1.

See **Figure 46** and **Figure 47** for the 24-, and 32-bit timing diagrams for I/V Sense Ping Pong Mode in TDM operation.

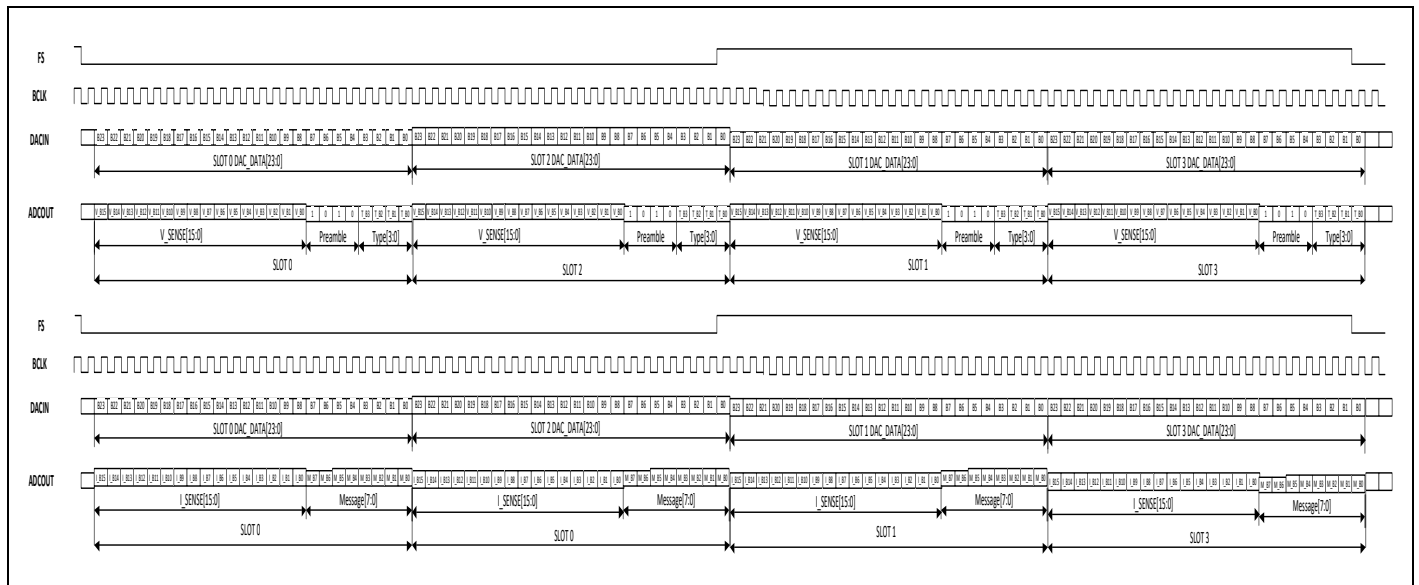


Figure 46 24-Bits I2S PingPong Mode in TDM Timing Diagram

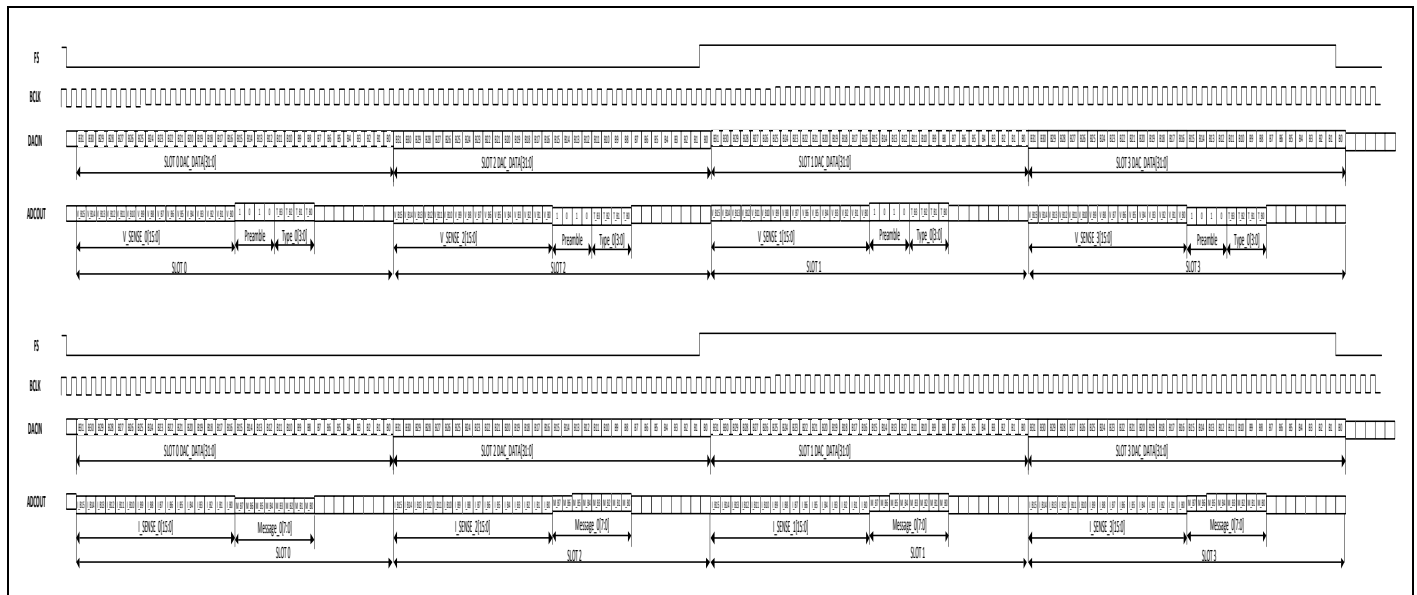


Figure 47 32-Bits I2S PingPong Mode in TDM Timing Diagram

7.3 Interrupt Request

Interrupt Request is a useful error checking feature that can indicate problems on the amplifier during use. Below is the registers used to control the nature of the request. Please refer to the corresponding register for more information.

- [INTERRUPT_CTRL_REG0x05](#)
- [INT_CLR_STATUS_REG0x06](#)
- [IO_CTRL_REG0x0A\[15:11\]](#)

An overview of this feature is that the physical IRQ pin [E4] Figure 1 goes to active logic when one of the bits in **INT_CLR_STATUS** become activated. The IRQ pin can be configured in **IO_CTRL[15:11]**, in which we will be assuming that it is using active high logic (meaning the register will become one when triggered) set in [IO_CTRL_REG0x0A\[15\]](#). Additionally, this **IRQ** pin [E4] should be connected to the external interrupt of its controller, of which the controller will activate its Interrupt Service Routine (ISR) when **IRQ** pin goes high. The ISR should then read **INT_CLR_STATUS** register, reset the same register by sending a single bit 1 to the activated bit in that register, and trigger a flag to fix what may have happened depending on the interrupt status shown in **INT_CLR_STATUS**. NOTE: Only one bit can be reset at a time.

What shows in the IRQ pin [E4] and the status register is controlled by the **INTERRUPT_CTRL** register. The top bits (disable) [14:8] control whether the conditions would show up in both the **INT_CLR_STATUS** register and IRQ pin while the lower bits (mask) [7:0] will let it show on the **INT_CLR_STATUS** register but not on the IRQ pin. In short, the IRQ pin is latched to all of the triggering bits in the **INT_CLR_STATUS** register and will go low when all bits in the **INT_CLR_STATUS** register is reset.

An example of this is when Over Voltage Protection (OVP) occurs during activation of output. On initial register loading, we set **IO_CTRL** to 0x8800 meaning IRQ logic is active high and output is enable. Additionally we want to set the **INTERRUPT_CTRL** to 0x6070 which enables the current/temperature

protection, clipping, low/over voltage protection, and power detection and masks the interrupt detecting clipping on the output.

Interrupt Triggers:

- **INT_CLR_STATUS_REG0x06[0]** – Power Interrupt Status: Triggered by providing supply power, activating **ENA_CTRL_REG0x04**, and based on the **PWRUPEN** signal.
- **INT_CLR_STATUS_REG0x06[1]** – Over Voltage Protection (OVP) Detection: Triggered by VBST reaching 14.1V

Activating output by triggering **ENA_CTRL**, **INT_CLR_STATUS** bit 0 becomes activated and the IRQ pin latches causing a trigger on the external interrupt on the controller. The controller can then acknowledge this in its check on the status register and reset both the IRQ pin and status register by writing 0x0001 to **INT_CLR_STATUS**. However, the **IRQ** pin is still active, indicating there is something wrong with the NAU8331. The controller must then invoke a check on **INT_CLR_STATUS** again in which it sees **INT_CLR_STATUS** bit 1 is still high. From this we can deduce that after a short time after resetting the status register, the OVP detection interrupt triggered meaning the VBST voltage ramped up after setting output but slow enough to occur right after resetting the status register. The controller must realize this and take appropriate steps to fix this occurrence.

NOTE #1: When activating the Class-D Driver output either manually through registers or through the **PWRUPEN** signal, OVP may trigger and will require reset.

NOTE #2: Because the on/off trigger is based on the **PWRUPEN** signal and when inducing the **PWRUPEN** signal through the clock detection circuit (Section 5.12) using the I²S communication protocol, if any of the incoming signals are stopped, specifically DACIN, then the **PWRUPEN** signal is set to 0 and awaits the signal is present again. When present again, the **PWRUPEN** signal will trigger and the on/off interrupt will also trigger.

7.4 I2C Device Address and GPIO Debugging

GPIO1 and GPIO2 Pins are able to be configured used to configure the I²C device address at startup and display different internal signals of the chip and read off an oscilloscope for debugging purposes. For I2C device address initialization, GPIO1 and GPIO2 should follow Table 27 I2C Device Address Initialization. and be set before supplying power. After power on, be sure to set I2C_ADDR (**REG0x02[0]**) to 1 to latch the I2C device address and prevent further changes to it through potential noise.

Table 27 I2C Device Address Initialization.

I2C Device Address	GPIO2	GPIO1
0x10	GND (0)	GND (0)
0x11	GND (0)	VDDDB (1)
0x40	VDDDB (1)	GND (0)
0x41	VDDDB (1)	VDDDB (1)

GPIO Register Information:

I2C_ADDR_REG0x02[0] – I2C Device Address latch bit. After setting the I2C Device Address, set this bit to 1 to prevent changes to the device address.

GPIO124_CTRL_REG0x08 – GPIO Configuration. Can be set for either input mode or output mode with additional settings including drive strength, pull enable, or pull high or low.

GPIOOUT_REG0x09[15:13] – Used only when GPIO in Output Mode. Select what output should be displayed on the GPIO1 and GPIO2 pins.

GENERAL_STATUS0_REG0x1D[1:0] – Used only when GPIO in Input Mode. Used as a tunneled digital signal from either GPIO1 or GPIO2 for the ability to be read through I²C.

GPIO Output Information:

Be sure to latch the I2C Device Address before using the GPIO debugging feature. When activating the GPIO output as shown in the example, the NAU8331 will bring the GPIO to the settings in Reg0x08. The settings in the example is for HIGH = VDDDB and LOW = GND.

■ **GPIO124_CTRL_REG0x08 = 0x81**

- o GPIO2 Output
 - [10] Pin is pull down
 - [9] Drive is set to high
 - [8] Pin Pull is enabled
 - [7] Pin is enabled
- o GPIO1 Output
 - [10] Pin is pull down
 - [9] Drive is set to high
 - [8] Pin Pull is enabled
 - [7] Pin is enabled

■ **GPIOOUT_REG0x09[15:13] = 000 – 111** Selection Based on Table 28 GPIOOUT Selection:

Table 28 GPIOOUT Selection

GPIOOUT_REG0x09[15:13]	GPIO1	GPIO2
000	GPIO1OUT	GPIO2OUT
001	MCLK	SDB
010	MCLKDET	OSC_CLK
011	OTP	MUTEB
100	OVP	SHUTDWNDRVRR
101	OCF	PWRDWN1B_D
110	PWRUPEN	PDOSCB
111	SCLK_I	SDA_I

GPIO Output Descriptions:

- MCLK – Master Clock as seen by the NAU8331
- SDB – Shut Down Bar, Class-D Driver Enable signal generated from the register 0x62.
- MCLKDET – Master Clock Detection. Displays when the MCLK is detected.
- OSC_CLK – Oscillator Clock. Outputs a clock (~300kHz) which the PWM is derived from.
- OTP – Over Temperature Protection. Displays the trigger when junction temperature goes over limit.
- MUTE_B – Mute Bar. Mutes the Class-D Driver when low and unmutes when high. Mute happens on startup.
- OVP – Over Voltage Protection. Displays the trigger when voltage across the Class-D Driver goes over limit.
- SHUTDWNDRVRR – Shutdown Driver. Shows when the Class-D Driver is either on or off.
- OCP – Over Current Protection. Displays the trigger when current across the Class-D Driver goes over limit.
- PWRDOWN1B_D – Indicates Class-D power up when high. Only occurs after SDB goes from low to high.
- PWRUPEN – Power Up Enable. Indicates when Power Up occurs. Usually happens after clock detection to enable Class-D Driver.
- PDOSCB – Oscillator Power Down Bar. Indicates Class-D oscillator power up when high. Only occurs after SDB goes from low to high.
- SCLK_I – Serial Clock for I²C buffering. Displays what is seen on the SCLK pin.
- SDA_I – Serial Data for I²C buffering. Displays what is seen on the SDA pin.

7.5 Control Registers

Table 29 provides detailed information for the NAU8331 Control Registers. Note that all registers marked as 'Reserved' should not be overwritten, unless it is requested to do so by Nuvoton Technology Corporation.

REG	Function	REG	Function
0	<u>HARDWARE_RST</u>	2D	<u>ALC_CTRL2</u>
1	<u>SOFTWARE_RST</u>	2E	<u>ALC_CTRL3</u>
2	<u>I2C_ADDR</u>	2F	<u>ALC_CTRL4</u>
3	<u>CLK_CTRL</u>	30	<u>TEMP_COMP_CTRL</u>
4	<u>ENA_CTRL</u>	31	<u>ADCL_DRC_KNEE</u> <u>IP_12</u>
5	<u>INTERRUPT_CTRL</u>	32	<u>ADCL_DRC_KNEE_IP_34</u>
6	<u>INT_CLR_STATUS</u>	33	<u>ADCL</u> <u>DRC_SLOPES</u>
7	<u>SAR</u> CTRL1	34	<u>ADCR</u> <u>DRC</u> ATKDCY
8	<u>GPIO124_CTRL</u>	35	<u>ADCR_DRC_KNEE</u> <u>IP_12</u>
9	<u>GPIOOUT</u>	36	<u>ADCR_DRC_KNEE</u> <u>IP_34</u>
A	<u>IO_CTRL</u>	37	<u>ADCR</u> <u>DRC_SLOPES</u>
C	<u>TDM_CTRL</u>	38	<u>ADCR</u> <u>DRC</u> ATKDCY
D	<u>I2S_PCM_CTRL1</u>	40	<u>CLK_DET_CTRL</u>
E	<u>I2S_PCM_CTRL2</u>	45	<u>SOFTWARE_ID</u>
F	<u>LEFT_TIME_SLOT</u>	46	<u>I2C_DEVICE_ID</u>
10	<u>RIGHT_TIME_SLOT</u>	49	<u>TEST_STATUS</u>
12	<u>HPF_CTRL</u>	4A	<u>ANALOG_READ</u>
13	<u>MUTE_CTRL</u>	55	<u>MISC_CTRL</u>
14	<u>ADC_VOL_CTRL</u>	60	<u>BIAS_ADJ</u>

15	<u>RESERVED</u>
16	<u>RESERVED</u>
17	<u>BOOST_CTRL1</u>
18	<u>BOOST_CTRL2</u>
19	<u>DRC_GAIN_LADC</u>
1A	<u>DRC_GAIN_RADC</u>
1B	<u>CLK_DOUBLER_O</u>
1C	<u>BOOST_CTRL_O</u>
1D	<u>GENERAL_STATUS0</u>
1E	<u>GENERAL_STATUS1</u>
1F	<u>GENERAL_STATUS2</u>
20	<u>SAR_ADC_OUT_01</u>
21	<u>SAR_ADC_OUT_23</u>
22	<u>ALC_READOUT1</u>
23	<u>ALC_READOUT2</u>
24	<u>ALC_READOUT3</u>
28	<u>ADC_RATE</u>
29	<u>DAC_CTRL1</u>
2A	<u>DAC_TRL2</u>
2C	<u>ALC_CTRL1</u>

61	<u>ANALOG_CTRL_1</u>
62	<u>ANALOG_CTRL_2</u>
63	<u>ANALOG_CTRL_3</u>
64	<u>ANALOG_CTRL_4</u>
65	<u>ANALOG_CTRL_5</u>
66	<u>ANALOG_CTRL_6</u>
68	<u>ANALOG_CTRL_7</u>
69	<u>CLIP_CTRL</u>
71	<u>RESERVED</u>
72	<u>ANALOG_ADC_2</u>
73	<u>RDAC</u>
76	<u>BOOST</u>
77	<u>FEPGA</u>
7F	<u>POWER_UP_CTRL</u>

Table 29 Control Registers

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	HARDWARE_RST	RESET_N1																	Hardware Reset Write once to reset all the registers to set registers to default values.
1	SOFTWARE_RST	RESET_N_SOFT_PRE																	Software Reset Write twice to reset all internal state machines without resetting the registers.
2	I2C_ADDR	I2C_ADDR_SEL																	I2C Address Selection Device Selection Set I2C_ADDR_SEL = 1, then latch the status of the GPIO1_IN, GPIO2_IN: GPIO1 and GPIO2 input values are set by hardware. When reading or writing I2C device ID needs to match hardware GPIOs' values for read/write device registers; GPIO1_IN and GPIO2_IN values can be read from Reg0X1D[1:0] GPIO1_IN and GPIO2_IN ; Also, DEVICE ID can read from Reg0x1E[7:5] GPIO2_IN = 0, GPIO1_IN = 0, I2C_DEVID = 7'h10

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			GPIO2_IN = 0, GPIO1_IN = 1, I2C_DEVID = 7'h11 GPIO2_IN = 1, GPIO1_IN = 0, I2C_DEVID = 7'h40 GPIO2_IN = 1, GPIO1_IN = 1, I2C_DEVID = 7'h41
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
3	CLK_CTRL	CLK_DAC_INV																	DAC Clock Inversion in Analog Domain 1 = Enable 0 = Disable
		CLK_ADC_PL																	Invert ADC Clock Polarity 1 = Invert 0 = No change
		Reserved																	Reserved
		CLK_ADC_SRC																	Scaling for ADC Clock 00 = 1 01: 1/2 10 = 1/4 11: 1/8
		CLK_DAC_SRC																	Scaling for DAC Clock 00 = 1 01: 1/2 10 = 1/4 11: 1/8
		MCLK_SRC																	Scaling for MCLK 0000: 1 0001: 2 0010: 4* 0011: 8* 0100: 1/2 0101: 1/4 0110: 1/8 0111: Reserved 1000: 1 1001: 2 1010: 4* 1011: 8* 1100: 1/6 1101: 1/12 1110: 1/24 1111: Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
4	ENA_CTRL	DACEN																	DAC Channel Enable 1 = ON 0 = OFF
		ADCEN_I																	Current ADC Channel Enable 1 = ON 0 = OFF
		ADCEN_V																	Voltage ADC Channel Enable 1 = ON 0 = OFF
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
5	INTERRUPT_CTRL																		Reserved
																			Reserved
		OCP_OR_OTP_SHTDWN1_INT_P_MASK																	OCP/OTP Shutdown Interrupt Mask (Over Current/Over Temperature Shutdown) 1 = Mask the Interrupt

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			0 = Unmask
		CLIP_INTP_MASK																	Clip Interrupt Mask 1 = Mask the Interrupt 0 = Unmask
		LOVDDDET_INTP_MASK																	Low Voltage Detection Interrupt Mask 1 = Mask the Interrupt 0 = Unmask
		OVP_INTP_MASK																	Over Voltage Protection Interrupt mask 1 = Mask the Interrupt 0 = Unmask
		PWRUPEN_INTP_MASK																	Power Up Interrupt mask 1 = Mask the Interrupt 0 = Unmask
																			Reserved
																			Reserved
		OCP_OR_OTP_SHTDWN1_INT_DIS																	OCP/OTP Shutdown Interrupt Disable 1 = Disable 0 = Enable
		CLIP_INT_DIS																	Clip Interrupt Disable 1 = Disable 0 = Enable
		LOVDDDETB_INT_DIS																	Low Voltage Detection Interrupt Disable 1 = Disable 0 = Enable
		OVP_INT_DIS																	Over Voltage Protection Interrupt Disable 1 = Disable 0 = Enable
		PWRUPEN_INT_DIS																	Power Up Interrupt Disable 1 = Disable 0 = Enable
		Default	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0x007f
6	INT_CLR_STATUS	INT_CLR_STATUS																	Interrupt Clear Status Write Operation: Write bits [6:0] 1s to clear the corresponding Interrupt Status. Read Operation: REG6 [4:0] --- RD_INT_STATUS Bit6 = Reserved Bit5 = Reserved Bit4 = Over Current/Over Temperature Shutdown Bit3 = Clip Bit2 = Low Voltage Detection Bit1 = Over Voltage Protection Bit0 = Power Up
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read/Write
7	SAR_CTRL1	SAR_OUT_INV																	SAR Channel output invert enable 1 = Enable 0 = Disable
		Reserved																	Reserved
		SAR_TRACK_GAIN																	SAR Gain Tracking. Default setting = 001 000 = 1.0*VDDA 100 = 1.3*VDDA

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			001 = 1.0*VDDA 101 = 1.4*VDDA 010 = 1.1*VDDA 110 = 1.54*VDDA 011 = 1.2*VDDA 111 = 3.12*VDDA
		Reserved																	Reserved
		RES_SEL																	SAR Series Resistor, larger resistance value will filter out more noise but increase sampling and conversion time on SAR ADC. default set = 001 00 = 35 kOhms 001 = 70 kOhms 010 = 170 kOhms 011 = 360 kOhms 1xx = Short
		COMP_SPEED																	Time Setting for single Compare Cycle. The total conversion has 8 compare cycles. Please refer to 5.11.1 for more information. 00 = 500 nsec 01 = 1 µsec 10 = 2 µsec 11 = 4 µsec
		SAMPLE_SPEED																	SAR ADC Sampling Time. Please refer to 5.11.1 for more information. 00 = 2 µsec 01 = 4 µsec 10 = 8 µsec 11 = 16 µsec
		SAR_ENA																	SAR Enable; When changing SAMPLE_SPEED, SAR ADC must be disabled first. The order of this is to change this register to 0, change SAMPLE_SPEED to desired rate, and then change this to 1 to enable. 1 = Enable 0 = Disable
		Default	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0x00b4
8	GPIO124_CTRL	Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		GPIO2OUT																	GPIO2 Output Pull Select 0 = Pull Down 1 = Pull Up
		GPIO2_PS																	GPIO2 Input Pull Select 0 = Pull Down 1 = Pull Up
		GPIO2_DS																	GPIO2 Output Drive Current Select 1 = High 0 = Low
		GPIO2_PE_N																	GPIO2 Input Pin Pull Enable 0 = Enable 1 = Disable
		GPIO2_OE																	GPIO2 Programmable I/O Mode Select 1 = Output 0 = Input
		GPIO1OUT																	GPIO1 Output Pull Select 0 = Pull Down 1 = Pull Up
		GPIO1_PS																	GPIO1 Input Pull Select 0 = Pull Down 1 = Pull Up
		GPIO1_DS																	GPIO1 Output Current Drive Select 1 = High 0 = Low

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		GPIO1_PE																	GPIO1 Input Pin Pull Enable 1 = Enable 0 = Disable
		GPIO1_OE																	GPIO1 Programmable I/O Mode Select 1 = Output 0 = Input
		Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0x0102
9	GPIOOUT	GPIOoutSEL																	GPIO1/GPIO2 Output Function Select (input default) 000 = GPIO1OUT / GPIO2OUT 001 = MCLK / SDB 010 = MCLKDET / OSC_CLK 011 = OTP / MUTE 100 = OVP / SHUTDWNDRVR 101 = OCP / PWRDOWN1B_D 110 = PWRUPEN / PDOSCB 111 = SCLK_I / SDA_I
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
A	IO_CTRL	IRQ_PL																	Default IRQ Logic 1 = Active High 0 = Active Low
		IRQ_PS																	IRQ Pin Pull Select 0 = Pull Down 1 = Pull Up
		IRQ_PE																	IRQ Pin Pull Enable 0 = Enable 1 = Disable
		IRQ_DS																	IRQ Current Drive Select 1 = High 0 = Low
		IRQ_OE																	IRQ Output Enable 1 = Enable 0 = Disable
		BCLK_DS																	BCLK IO Drive Strength 1 = Stronger 0 = Default
		LRC_DS																	LRC IO Drive Strength 1 = Stronger 0 = Default
		ADCDAC_DS																	ADCOUT IO Drive Strength 1 = Stronger 0 = Default
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
C	TDM_CTRL	TDM																	TDM Enable 1 = Enable 0 = Disable
		PCM_OFFSET_MODE_CTRL																	PCM Offset Control in TDM 1 = Enable 0 = Disable
		UNSIGN_IV																	I Sense/V Sense Signed/Unsigned Format 1 = ISENSE, VSENSE output data unsigned 0 = ISENSE, VSENSE output data is signed
		PINGPONG_MODE																	PingPong Mode Enable 1 = Enable 0 = Disable

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DAC_SEL																	DAC Channel Source in TDM Mode <u>I2S</u> : 000 : from Slot 0 001 : from Slot 1 010 : from Slot 2 011 : from Slot 3 100 : Reserved 101 : Reserved 110 : Reserved 111 : Reserved <u>PCM</u> : 000 : from Slot 0 001 : from Slot 1 010 : from Slot 2 011 : from Slot 3 100 : from Slot 4 101 : from Slot 5 110 : from slot 6 111 : from Slot 7
		ADC_TX_SEL_I																	ADC Current Channel Source in TDM Mode <u>I2S</u> : 00: from Slot 1 01: from Slot 3 10: Reserved 11: Reserved <u>PCM</u> : 00: from Slot 1 01: from Slot 3 10: from Slot 5 11: from Slot 7
		ADC_TX_SEL_V																	ADC Voltage Channel Source in TDM Mode <u>I2S</u> : 00: from Slot 0 01: from Slot 2 10: Reserved 11: Reserved <u>PCM</u> : 00: from Slot 0 01: from Slot 2 10: from Slot 4 11: from Slot 6
		Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0x0C00
D	I2S_PCM_CTRL1	DACCM0																	DAC Companding Mode Control 00 = Off (normal linear operation) 01 = Reserved 10 = μ -Law Companding 11 = A-law Companding
		ADCCM0																	ADC Companding Mode Control 00 = Off (normal linear operation) 01 = Reserved 10 = μ -law Companding 11 = A-law Companding
		ADDAPO																	DAC Audio Data Input Option to route directly from ADC data stream 0 = No pass through, normal operation 1 = ADC output data stream routed to DAC input data path
		CMB8_0																	8-bit Word Enable for Companding Mode 0 = Normal operation (no Companding) 1 = 8-bit operation for Companding Mode
		UA_OFFSET																	μ Law Offset 0 = 1s complement 1 = 2s complement
		BCP0																	Bit Clock Phase Inversion Option for BCLK 0 = Normal phase 1 = Input logic sense inverted
		LRP0																	PCMA and PCMB Left/Right Word Order 0 = Right Justified/Left Justified/I2S/PCMA Mode 1 = PCMB Mode Enable: MSB is valid on 1st rising edge of BCLK after rising edge of FS
		Reserved																	Reserved

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		ADCPHS0																	ADC Audio Data Left-Right Ordering 0 = left ADC data in left phase of LRP 1 = left ADC data in right phase of LRP (left-right reversed)
		WLEN0																	Port Word Length of Audio Data Stream (24-bits default) 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length 11 = 32-bit word length
		AIFMT0																	Port Audio Interface Data Format (default setting is I2S) 01 = Left Justified 10 = Standard I2S Format 11 = PCMA or PCMB Audio Data Format Option
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0x000a
E	I2S_PCM_CTRL2	I2S_TRI																	I2S Tri-State 0 = Normal Mode 1 = Output High Z
		I2S_DRV																	I2S Driving Enable 0 = Normal Mode 1 = Always Out
		LRC_DIV																	LRC Divide Coefficient Setting 00 = 1/256 01 = 1/128 10 = 1/64 11 = 1/32
		PCM_TS_EN0																	PCM Time Slot Enable 0 = Only PCM_A_MODE or PCM_B_MODE (STEREO Only) can be used when PCM Mode is selected 1 = Time slot function enable for PCM Mode
		TRI0																	Without TDM Mode 0 = Drive the full Clock of LSB 1 = Tri-State the 2nd half of LSB
		PCM8BIT0																	PCM 8-Bit Word Length 0 = Use I2S_PCM_CTRL1 WLEN0 to select Word Length 1 = PCM Select 8-bit word length
		Reserved																	Reserved to 0
		ADCOUT0_PE																	ADCOUT IO Pull Enable 1 = Enable 0 = Disable
		ADCOUT0_PS																	ADCOUT IO Pull Up/Down Enable 1 = Pull Up 0 = Pull Down
		ADCOUT0_OE																	ADCOUT Out Enable 0 = ADCOUT Out Enable 1 = Block ADCOUT Out
		MS0																	Master/Slave Mode Enable 0 = Slave Mode 1 = Master Mode
		BCLKDIV																	BCLK DIVIDE Setting from MCLK frequency 000 = 1 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		Default	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x8010
F	LEFT_TIME_SLOT	FS_ERR_CMP_SEL																	Short Frame Synch Enable

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			Triggers short frame sync signal if frame sync is less than 00 = 252 x MCLK 01 = 253 x MCLK 10 = 254 x MCLK 11 = 255 x MCLK
		DIS_FS_SHORT_DET																	Short Frame Sync Detection Logic Enable 0 = Enable 1 = Disable
		TSLOT_L0																	Left Channel PCM Time Slot Start Value Or PCM TDM Offset Mode Slot Start Value
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
10	RIGHT_TIME_SLOT	TSLOT_R0																	Right Channel PCM Time Slot Start Value Or unused for PCM TDM Offset Mode
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
12	HPF_CTRL	DAC_HPF_EN																	DAC High Pass Filter Enable 1 = Enable 0 = Disable
		DAC_HPF_APP																	DAC High Pass Filter Application Mode
		DAC_HPF_FCUT																	DAC High Pass Filter Cut Off Frequency 000 : 130 Hz 001 : 155 Hz 010 : 198 Hz 011 : 248 Hz 100 : 311 Hz 101 : 398 Hz 110 : 503 Hz 111 : 614 Hz
		ADCL_HPF_EN																	ADC Left Channel High Pass Filter Enable 1 = Enable 0 = Disable
		ADCL_HPF_APP																	ADC Left Channel High Pass Filter Application Mode
		ADCL_HPF_FCUT																	ADC Left Channel High Pass Filter Cut Off Frequency 000 : 130 Hz 001 : 155 Hz 010 : 198 Hz 011 : 248 Hz 100 : 311 Hz 101 : 398 Hz 110 : 503 Hz 111 : 614 Hz
		ADCR_HPF_EN																	ADC Right Channel High Pass Filter Enable 1 = Enable 0 = Disable
		ADCR_HPF_APP																	ADC Right Channel High Pass Filter Application Mode
		ADCR_HPF_FCUT																	ADC Right Channel High Pass Filter Cut Off Frequency 000 : 130 Hz 001 : 155 Hz 010 : 198 Hz 011 : 248 Hz 100 : 311 Hz 101 : 398 Hz 110 : 503 Hz 111 : 614 Hz
		TC_EN																	Temperature Compensation Enable 1 = Enable 0 = Disable Note: Enabling Temperature Compensation adds one sample delay to the I-sense channel
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
13	MUTE_CTRL	SOFT_MUTE																	Soft Mute Enable 1 = Gradually lower DAC volume to zero

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			0 = Gradually increase DAC volume to volume register setting
		Reserved																	Reserved
		DACEN_SM																	DACEN Soft Mute 1 = Will have soft mute when set DACEN from 1 to 0. 0 = Disable this function
		Reserved																	Reserved
		DAC_ZC_EN																	DAC Zero Crossing Enable
		DAC_VOLUME																	DAC Volume Control Expressed as gain or attenuation in 0.5 db steps 0xff = +24 dB 0xfe = +23.5 dB 0xfd = +23 dB 0xfc = 0 dB 0xfb = -1 dB 0xfa = -2 dB 0xf9 = -3 dB 0xf8 = -4 dB 0xf7 = -5 dB 0xf6 = -6 dB 0xf5 = -7 dB 0xf4 = -8 dB 0xf3 = -9 dB 0xf2 = -10 dB 0xf1 = -11 dB 0xf0 = -12 dB 0xef = -13 dB 0xee = -14 dB 0xed = -15 dB 0xea = -18 dB 0xe9 = -20 dB 0xe8 = -24 dB 0xe7 = Mute 0xe6 = Mute 0xe5 = Mute 0xe4 = Mute 0xe3 = Mute 0xe2 = Mute 0xe1 = Mute 0xe0 = Mute 0xdf = Mute 0xde = Mute 0xdd = Mute 0xda = Mute 0xd9 = Mute 0xd8 = Mute 0xd7 = Mute 0xd6 = Mute 0xd5 = Mute 0xd4 = Mute 0xd3 = Mute 0xd2 = Mute 0xd1 = Mute 0xd0 = Mute 0xcf = Mute 0xce = Mute 0xcd = Mute 0xca = Mute 0xc9 = Mute 0xc8 = Mute 0xc7 = Mute 0xc6 = Mute 0xc5 = Mute 0xc4 = Mute 0xc3 = Mute 0xc2 = Mute 0xc1 = Mute 0xc0 = Mute 0xbf = Mute 0xbe = Mute 0xbd = Mute 0xba = Mute 0xb9 = Mute 0xb8 = Mute 0xb7 = Mute 0xb6 = Mute 0xb5 = Mute 0xb4 = Mute 0xb3 = Mute 0xb2 = Mute 0xb1 = Mute 0xb0 = Mute 0xaf = Mute 0xae = Mute 0xad = Mute 0xaa = Mute 0xa9 = Mute 0xa8 = Mute 0xa7 = Mute 0xa6 = Mute 0xa5 = Mute 0xa4 = Mute 0xa3 = Mute 0xa2 = Mute 0xa1 = Mute 0xa0 = Mute 0x9f = Mute 0x9e = Mute 0x9d = Mute 0x9a = Mute 0x99 = Mute 0x98 = Mute 0x97 = Mute 0x96 = Mute 0x95 = Mute 0x94 = Mute 0x93 = Mute 0x92 = Mute 0x91 = Mute 0x90 = Mute 0x8f = Mute 0x8e = Mute 0x8d = Mute 0x8a = Mute 0x89 = Mute 0x88 = Mute 0x87 = Mute 0x86 = Mute 0x85 = Mute 0x84 = Mute 0x83 = Mute 0x82 = Mute 0x81 = Mute 0x80 = Mute 0x7f = Mute 0x7e = Mute 0x7d = Mute 0x7a = Mute 0x79 = Mute 0x78 = Mute 0x77 = Mute 0x76 = Mute 0x75 = Mute 0x74 = Mute 0x73 = Mute 0x72 = Mute 0x71 = Mute 0x70 = Mute 0x6f = Mute 0x6e = Mute 0x6d = Mute 0x6a = Mute 0x69 = Mute 0x68 = Mute 0x67 = Mute 0x66 = Mute 0x65 = Mute 0x64 = Mute 0x63 = Mute 0x62 = Mute 0x61 = Mute 0x60 = Mute 0x5f = Mute 0x5e = Mute 0x5d = Mute 0x5a = Mute 0x59 = Mute 0x58 = Mute 0x57 = Mute 0x56 = Mute 0x55 = Mute 0x54 = Mute 0x53 = Mute 0x52 = Mute 0x51 = Mute 0x50 = Mute 0x4f = Mute 0x4e = Mute 0x4d = Mute 0x4a = Mute 0x49 = Mute 0x48 = Mute 0x47 = Mute 0x46 = Mute 0x45 = Mute 0x44 = Mute 0x43 = Mute 0x42 = Mute 0x41 = Mute 0x40 = Mute 0x3f = Mute 0x3e = Mute 0x3d = Mute 0x3a = Mute 0x39 = Mute 0x38 = Mute 0x37 = Mute 0x36 = Mute 0x35 = Mute 0x34 = Mute 0x33 = Mute 0x32 = Mute 0x31 = Mute 0x30 = Mute 0x2f = Mute 0x2e = Mute 0x2d = Mute 0x2a = Mute 0x29 = Mute 0x28 = Mute 0x27 = Mute 0x26 = Mute 0x25 = Mute 0x24 = Mute 0x23 = Mute 0x22 = Mute 0x21 = Mute 0x20 = Mute 0x1f = Mute 0x1e = Mute 0x1d = Mute 0x1a = Mute 0x19 = Mute 0x18 = Mute 0x17 = Mute 0x16 = Mute 0x15 = Mute 0x14 = Mute 0x13 = Mute 0x12 = Mute 0x11 = Mute 0x10 = Mute 0x0f = Mute 0x0e = Mute 0x0d = Mute 0x0a = Mute 0x09 = Mute 0x08 = Mute 0x07 = Mute 0x06 = Mute 0x05 = Mute 0x04 = Mute 0x03 = Mute 0x02 = Mute 0x01 = Mute 0x00 = Mute
		Default	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0x00cf
14	ADC_VOL_CTRL	ADC_GAIN_L																	ADC Left Channel Volume Control Expressed as gain or attenuation in 0.125 db steps; max is 24.125 dB 0x00 = 0 dB 0x01 = 0.125 dB 0x02 = 0.25 dB 0x03 = 0.375 dB 0x04 = 0.5 dB 0x05 = 0.625 dB 0x06 = 0.75 dB 0x07 = 0.875 dB 0x08 = 1 dB 0x09 = 1.125 dB 0x0a = 1.25 dB 0x0b = 1.375 dB 0x0c = 1.5 dB 0x0d = 1.625 dB 0x0e = 1.75 dB 0x0f = 1.875 dB 0x10 = 2 dB 0x11 = 2.125 dB 0x12 = 2.25 dB 0x13 = 2.375 dB 0x14 = 2.5 dB 0x15 = 2.625 dB 0x16 = 2.75 dB 0x17 = 2.875 dB 0x18 = 3 dB 0x19 = 3.125 dB 0x1a = 3.25 dB 0x1b = 3.375 dB 0x1c = 3.5 dB 0x1d = 3.625 dB 0x1e = 3.75 dB 0x1f = 3.875 dB 0x20 = 4 dB 0x21 = 4.125 dB 0x22 = 4.25 dB 0x23 = 4.375 dB 0x24 = 4.5 dB 0x25 = 4.625 dB 0x26 = 4.75 dB 0x27 = 4.875 dB 0x28 = 5 dB 0x29 = 5.125 dB 0x2a = 5.25 dB 0x2b = 5.375 dB 0x2c = 5.5 dB 0x2d = 5.625 dB 0x2e = 5.75 dB 0x2f = 5.875 dB 0x30 = 6 dB 0x31 = 6.125 dB 0x32 = 6.25 dB 0x33 = 6.375 dB 0x34 = 6.5 dB 0x35 = 6.625 dB 0x36 = 6.75 dB 0x37 = 6.875 dB 0x38 = 7 dB 0x39 = 7.125 dB 0x3a = 7.25 dB 0x3b = 7.375 dB 0x3c = 7.5 dB 0x3d = 7.625 dB 0x3e = 7.75 dB 0x3f = 7.875 dB 0x40 = 8 dB 0x41 = 8.125 dB 0x42 = 8.25 dB 0x43 = 8.375 dB 0x44 = 8.5 dB 0x45 = 8.625 dB 0x46 = 8.75 dB 0x47 = 8.875 dB 0x48 = 9 dB 0x49 = 9.125 dB 0x4a = 9.25 dB 0x4b = 9.375 dB 0x4c = 9.5 dB 0x4d = 9.625 dB 0x4e = 9.75 dB 0x4f = 9.875 dB 0x50 = 10 dB 0x51 = 10.125 dB 0x52 = 10.25 dB 0x53 = 10.375 dB 0x54 = 10.5 dB 0x55 = 10.625 dB 0x56 = 10.75 dB 0x57 = 10.875 dB 0x58 = 11 dB 0x59 = 11.125 dB 0x5a = 11.25 dB 0x5b = 11.375 dB 0x5c = 11.5 dB 0x5d = 11.625 dB 0x5e = 11.75 dB 0x5f = 11.875 dB 0x60 = 12 dB 0x61 = 12.125 dB 0x62 = 12.25 dB 0x63 = 12.375 dB 0x64 = 12.5 dB 0x65 = 12.625 dB 0x66 = 12.75 dB 0x67 = 12.875 dB 0x68 = 13 dB 0x69 = 13.125 dB 0x6a = 13.25 dB 0x6b = 13.375 dB 0x6c = 13.5 dB 0x6d = 13.625 dB 0x6e = 13.75 dB 0x6f = 13.875 dB 0x70 = 14 dB 0x71 = 14.125 dB 0x72 = 14.25 dB 0x73 = 14.375 dB 0x74 = 14.5 dB 0x75 = 14.625 dB 0x76 = 14.75 dB 0x77 = 14.875 dB 0x78 = 15 dB 0x79 = 15.125 dB 0x7a = 15.25 dB 0x7b = 15.375 dB 0x7c = 15.5 dB 0x7d = 15.625 dB 0x7e = 15.75 dB 0x7f = 15.875 dB 0x80 = 16 dB 0x81 = 16.125 dB 0x82 = 16.25 dB 0x83 = 16.375 dB 0x84 = 16.5 dB 0x85 = 16.625 dB 0x86 = 16.75 dB 0x87 = 16.875 dB 0x88 = 17 dB 0x89 = 17.125 dB 0x8a = 17.25 dB 0x8b = 17.375 dB 0x8c = 17.5 dB 0x8d = 17.625 dB 0x8e = 17.75 dB 0x8f = 17.875 dB 0x90 = 18 dB 0x91 = 18.125 dB 0x92 = 18.25 dB 0x93 = 18.375 dB 0x94 = 18.5 dB 0x95 = 18.625 dB 0x96 = 18.75 dB 0x97 = 18.875 dB 0x98 = 19 dB 0x99 = 19.125 dB 0x9a = 19.25 dB 0x9b = 19.375 dB 0x9c = 19.5 dB 0x9d = 19.625 dB 0x9e = 19.75 dB 0x9f = 19.875 dB 0xa0 = 20 dB 0xa1 = 20.125 dB 0xa2 = 20.25 dB 0xa3 = 20.375 dB 0xa4 = 20.5 dB 0xa5 = 20.625 dB 0xa6 = 20.75 dB 0xa7 = 20.875 dB 0xa8 = 21 dB 0xa9 = 21.125 dB 0xaa = 21.25 dB 0xab = 21.375 dB 0xac = 21.5 dB 0xad = 21.625 dB 0xae = 21.75 dB 0xaf = 21.875 dB 0xb0 = 22 dB 0xb1 = 22.125 dB 0xb2 = 22.25 dB 0xb3 = 22.375 dB 0xb4 = 22.5 dB 0xb5 = 22.625 dB 0xb6 = 22.75 dB 0xb7 = 22.875 dB 0xb8 = 23 dB 0xb9 = 23.125 dB 0xba = 23.25 dB 0xbb = 23.375 dB 0xbc = 23.5 dB 0xbd = 23.625 dB 0xbe = 23.75 dB 0xbf = 23.875 dB 0xc0 = 24 dB 0xc1 = 24.125 dB 0xc2 = 24.25 dB 0xc3 = 24.375 dB 0xc4 = 24.5 dB 0xc5 = 24.625 dB 0xc6 = 24.75 dB 0xc7 = 24.875 dB 0xc8 = 25 dB 0xc9 = 25.125 dB 0xca = 25.25 dB 0xcb = 25.375 dB 0xcc = 25.5 dB 0xcd = 25.625 dB 0xce = 25.75 dB 0xcf = 25.875 dB 0xd0 = 26 dB 0xd1 = 26.125 dB 0xd2 = 26.25 dB 0xd3 = 26.375 dB 0xd4 = 26.5 dB 0xd5 = 26.625 dB 0xd6 = 26.75 dB 0xd7 = 26.875 dB 0xd8 = 27 dB 0xd9 = 27.125 dB 0xda = 27.25 dB 0xdb = 27.375 dB 0xdc = 27.5 dB 0xdd = 27.625 dB 0xde = 27.75 dB 0xdf = 27.875 dB 0xe0 = 28 dB 0xe1 = 28.125 dB 0xe2 = 28.25 dB 0xe3 = 28.375 dB 0xe4 = 28.5 dB 0xe5 = 28.625 dB 0xe6 = 28.75 dB 0xe7 = 28.875 dB 0xe8 = 29 dB 0xe9 = 29.125 dB 0xea = 29.25 dB 0xeb = 29.375 dB 0xec = 29.5 dB 0xed = 29.625 dB 0xee = 29.75 dB 0xef = 29.875 dB 0xf0 = 30 dB 0xf1 = 30.125 dB 0xf2 = 30.25 dB 0xf3 = 30.375 dB 0xf4 = 30.5 dB 0xf5 = 30.625 dB 0xf6 = 30.75 dB 0xf7 = 30.875 dB 0xf8 = 31 dB 0xf9 = 31.125 dB 0xfa = 31.25 dB 0xfb = 31.375 dB 0xfc = 31.5 dB 0xfd = 31.625 dB 0xfe = 31.75 dB 0xff = 31.875 dB 0x00 = 32 dB 0x01 = 32.125 dB 0x02 = 32.25 dB 0x03 = 32.375 dB 0x04 = 32.5 dB 0x05 = 32.625 dB 0x06 = 32.75 dB 0x07 = 32.875 dB 0x08 = 33 dB 0x09 = 33.125 dB 0x0a = 33.25 dB 0x0b = 33.375 dB 0x0c = 33.5 dB 0x0d = 33.625 dB 0x0e = 33.75 dB 0x0f = 33.875 dB 0x10 = 34 dB 0x11 = 34.125 dB 0x12 = 34.25 dB 0x13 = 34.375 dB 0x14 = 34.5 dB 0x15 = 34.625 dB 0x16 = 34.75 dB 0x17 = 34.875 dB 0x18 = 35 dB 0x19 = 35.125 dB 0x1a = 35.25 dB 0x1b = 35.375 dB 0x1c = 35.5 dB 0x1d = 35.625 dB 0x1e = 35.75 dB 0x1f = 35.875 dB 0x20 = 36 dB 0x21 = 36.125 dB 0x22 = 36.25 dB 0x23 = 36.375 dB 0x24 = 36.5 dB 0x25 = 36.625 dB 0x26 = 36.75 dB 0x27 = 36.875 dB 0x28 = 37 dB 0x29 = 37.125 dB 0x2a = 37.25 dB 0x2b = 37.375 dB 0x2c = 37.5 dB 0x2d = 37.625 dB 0x2e = 37.75 dB 0x2f = 37.875 dB 0x30 = 38 dB 0x31 = 38.125 dB 0x32 = 38.25 dB 0x33 = 38.375 dB 0x34 = 38.5 dB 0x35 = 38.625 dB 0x36 = 38.75 dB 0x37 = 38.875 dB 0x38 = 39 dB 0x39 = 39.125 dB 0x3a = 39.25 dB 0x3b = 39.375 dB 0x3c = 39.5 dB 0x3d = 39.625 dB 0x3e = 39.75 dB 0x3f = 39.875 dB 0x40 = 40 dB 0x41 = 40.125 dB 0x42 = 40.25 dB 0x43 = 40.375 dB 0x44 = 40.5 dB 0x45 = 40.625 dB 0x46 = 40.75 dB 0x47 = 40.875 dB 0x48 = 41 dB 0x49 = 41.125 dB 0x4a = 41.25 dB 0x4b = 41.375 dB 0x4c = 41.5 dB 0x4d = 41.625 dB 0x4e = 41.75 dB 0x4f = 41.875 dB 0x50 = 42 dB 0x51 = 42.125 dB 0x52 = 42.25 dB 0x53 = 42.375 dB 0x54 = 42.5 dB 0x55 = 42.625 dB 0x56 = 42.75 dB 0x57 = 42.875 dB 0x58 = 43 dB 0x59 = 43.125 dB 0x5a = 43.25 dB 0x5b = 43.375 dB 0x5c = 43.5 dB 0x5d = 43.625 dB 0x5e = 43.75 dB 0x5f = 43.875 dB 0x60 = 44 dB 0x61 = 44.125 dB 0x62 = 44.25 dB 0x63 = 44.375 dB 0x64 = 44.5 dB 0x65 = 44.625 dB 0x66 = 44.75 dB 0x67 = 44.875 dB 0x68 = 45 dB 0x69 = 45.125 dB 0x6a = 45.25 dB 0x6b = 45.375 dB 0x6c = 45.5 dB 0x6d = 45.625 dB 0x6e = 45.75 dB 0x6f = 45.875 dB 0x70 = 46 dB 0x71 = 46.125 dB 0x72 = 46.25 dB 0x73 = 46.375 dB 0x74 = 46.5 dB 0x75 = 46.625 dB 0x76 = 46.75 dB 0x77 = 46.875 dB 0x78 = 47 dB 0x79 = 47.125 dB 0x7a = 47.25 dB 0x7b = 47.375 dB 0x7c = 47.5 dB 0x7d = 47.625 dB 0x7e = 47.75 dB 0x7f = 47.875 dB 0x80 = 48 dB 0x81 = 48.125 dB 0x82 = 48.25 dB 0x83 = 48.375 dB 0x84 = 48.5 dB 0x85 = 48.625 dB 0x86 = 48.75 dB 0x87 = 48.875 dB 0x88 = 49 dB 0x89 = 49.125 dB 0x8a = 49.25 dB 0x8b = 49.375 dB 0x8c = 49.5 dB 0x8d = 49.625 dB 0x8e = 49.75 dB 0x8f = 49.875 dB 0x90 = 50 dB 0x91 = 50.125 dB 0x92 = 50.25 dB 0x93 = 50.375 dB 0x94 = 50.5 dB 0x95 = 50.625 dB 0x96 = 50.75 dB 0x97 = 50.875 dB 0x98 = 51 dB 0x99 = 51.125 dB 0x9a = 51.25 dB 0x9b = 51.375 dB 0x9c = 51.5 dB 0x9d = 51.625 dB 0x9e = 51.75 dB 0x9f = 51.875 dB 0xa0 = 52 dB 0xa1 = 52.125 dB 0xa2 = 52.25 dB 0xa3 = 52.375 dB 0xa4 = 52.5 dB 0xa5 = 52.625 dB 0xa6 = 52.75 dB 0xa7 = 52.875 dB 0xa8 = 53 dB 0xa9 = 53.125 dB 0xaa = 53.25 dB 0xab = 53.375 dB 0xac = 53.5 dB 0xad = 53.625 dB 0xae = 53.75 dB 0xaf = 53.875 dB 0xb0 = 54 dB 0xb1 = 54.125 dB 0xb2 = 54.25 dB 0xb3 = 54.375 dB 0xb4 = 54.5 dB 0xb5 = 54.625 dB 0xb6 = 54.75 dB 0xb7 = 54.875 dB 0xb8 = 55 dB 0xb9 = 55.125 dB 0xba = 55.25 dB 0xbb = 55.375 dB 0xbc = 55.5 dB 0xbd = 55.625 dB 0xbe = 55.75 dB 0xbf = 55.875 dB 0xc0 = 56 dB 0xc1 = 56.125 dB 0xc2 = 56.25 dB 0xc3 = 56.375 dB 0xc4 = 56.5 dB 0xc5 = 56.625 dB 0xc6 = 56.75 dB 0xc7 = 56.875 dB 0xc8 = 57 dB 0xc9 = 57.125 dB 0xca = 57.25 dB 0xcb = 57.375 dB 0xcc = 57.5 dB 0xcd = 57.625 dB 0xce = 57.75 dB 0xcf = 57.875 dB 0xd0 = 58 dB 0xd1 = 58.125 dB 0xd2 = 58.25 dB 0xd3 = 58.375 dB 0xd4 = 58.5 dB 0xd5 = 58.625 dB 0xd6 = 58.75 dB 0xd7 = 58.875 dB 0xd8 = 59 dB 0xd9 = 59.125 dB 0xda = 59.25 dB 0xdb = 59.375 dB 0xdc = 59.5 dB 0xdd = 59.625 dB 0xde = 59.75 dB 0xdf = 59.875 dB 0xe0 = 60 dB 0xe1 = 60.125 dB 0xe2 = 60.25 dB 0xe3 = 60.375 dB 0xe4 = 60.5 dB 0xe5 = 60.625 dB 0xe6 = 60.75 dB 0xe7 = 60.875 dB 0xe8 = 61 dB 0xe9 = 61.125 dB 0xea = 61.25 dB 0xeb = 61.375 dB 0xec = 61.5 dB 0xed = 61.625 dB 0xee = 61.75 dB 0xef = 61.875 dB 0xf0 = 62 dB 0xf1 = 62.125 dB 0xf2 = 62.25 dB 0xf3 = 62.375 dB 0xf4 = 62.5 dB 0xf5 = 62.625 dB 0xf6 = 62.75 dB 0xf7 = 62.875 dB 0xf8 = 63 dB 0xf9 = 63.125 dB 0xfa = 63.25 dB 0xfb = 63.375 dB 0xfc = 63.5 dB 0xfd = 63.625 dB 0xfe = 63.75 dB 0xff = 63.875 dB 0x00 = 64 dB 0x01 = 64.125 dB 0x02 = 64.25 dB 0x03 = 64.375 dB 0x04 = 64.5 dB 0x05 = 64.625 dB 0x06 = 64.75 dB 0x07 = 64.875 dB 0x08 = 65 dB 0x09 = 65.125 dB 0x0a = 65.25 dB 0x0b = 65.375 dB 0x0c = 65.5 dB 0x0d = 65.625 dB 0x0e = 65.75 dB 0x0f = 65.875 dB 0x10 = 66 dB 0x11 = 66.125 dB 0x12 = 66.25 dB 0x13 = 66.375 dB 0x14 = 66.5 dB 0x15 = 66.625 dB 0x16 = 66.75 dB 0x17 = 66.875 dB 0x18 = 67 dB 0x19 = 67.125 dB 0x1a = 67.25 dB 0x1b = 67.375 dB 0x1c = 67.5 dB 0x1d = 67.625 dB 0x1e = 67.75 dB 0x1f = 67.875 dB 0x20 = 68 dB 0x21 = 68.125 dB 0x22 = 68.25 dB 0x23 = 68.375 dB 0x24 = 68.5 dB 0x25 = 68.625 dB 0x26 = 68.75 dB 0x27 = 68.875 dB 0x28 = 69 dB 0x29 = 69.125 dB 0x2a = 69.25 dB 0x2b = 69.375 dB 0x2c = 69.5 dB 0x2d = 69.625 dB 0x2e = 69.75 dB 0x2f = 69.875 dB 0x30 = 70 dB 0x31 = 70.125 dB 0x32 = 70.25 dB 0x33 = 70.375 dB 0x34 = 70.5 dB 0x35 = 70.625 dB 0x36 = 70.75 dB 0x37 = 70.875 dB 0x38 = 71 dB 0x39 = 71.125 dB 0x3a = 71.25 dB 0x3b = 71.375 dB 0x3c = 71.5 dB 0x3d = 71.625 dB 0x3e = 71.75 dB 0x3f = 71.875 dB 0x40 = 72 dB 0x41 = 72.125 dB 0x42 = 72.25 dB 0x43 = 72.375 dB 0x44 = 72.5 dB 0x45 = 72.625 dB 0x46 = 72.75 dB 0x47 = 72.875 dB 0x48 = 73 dB 0x49 = 73.125 dB 0x4a = 73.25 dB 0x4b = 73.375 dB 0x4c = 73.5 dB 0x4d = 73.625 dB 0x4e = 73.75 dB 0x4f = 73.875 dB 0x50 = 74 dB 0x51 = 74.125 dB 0x52 = 74.25 dB 0x53 = 74.375 dB 0x54 = 74.5 dB 0x55 = 74.625 dB 0x56 = 74.75 dB 0x57 = 74.875 dB 0x58 = 75 dB 0x59 = 75.125 dB 0x5a = 75.25 dB 0x5b = 75.375 dB 0x5c = 75.5 dB 0x5d = 75.625 dB 0x5e = 75.75 dB 0x5f = 75.875 dB 0x60 = 76 dB 0x61 = 76.125 dB 0x62 = 76.25 dB 0x63 = 76.375 dB 0x64 = 76.5 dB 0x65 = 76.625 dB 0x66 = 76.75 dB 0x67 = 76.875 dB 0x68 = 77 dB 0x69 = 77.125 dB 0x6a = 77.25 dB 0x6b = 77.375 dB 0x6c = 77.5 dB 0x6d = 77.625 dB 0x6e = 77.75 dB 0x6f = 77.875 dB 0x70 = 78 dB 0x71 = 78.125 dB 0x72 = 78.25 dB 0x73 = 78.375 dB 0x74 = 78.5 dB 0x75 = 78.625 dB 0x76 = 78.75 dB 0x77 = 78.875 dB 0x78 = 79 dB 0x79 = 79.125 dB 0x7a = 79.25 dB 0x7b = 79.375 dB 0x7c = 79.5 dB 0x7d = 79.625 dB 0x7e = 79.75 dB 0x7f = 79.875 dB 0x80 = 80 dB 0x81 = 80.125 dB 0x82 = 80.25 dB 0x83 = 80.375 dB 0x84 = 80.5 dB 0x85 = 80.625 dB 0x86 = 80.75 dB 0x87 = 80.875 dB 0x88 = 81 dB 0x89 = 81.125 dB 0x8a = 81.25 dB 0x8b = 81.375 dB 0x8c = 81.5 dB 0x8d = 81.625 dB 0x8e = 81.75 dB 0x8f = 81.875 dB 0x90 = 82 dB 0x91 = 82.125 dB 0x92 = 82.25 dB 0x93 = 82.375 dB 0x94 = 82.5 dB 0x95 = 82.625 dB 0x96 = 82.75 dB 0x97 = 82.875 dB 0x98 = 83 dB 0x99 = 83.125 dB 0x9a = 83.25 dB 0x9b = 83.375 dB 0x9c = 83.5 dB 0x9d = 83.625 dB 0x9e = 83.75 dB 0x9f = 83.875 dB 0xa

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			0.16 V per step Booster only turns on when DAC out + margin larger than the Vbat 0x00 = 0 V 0x01 = 0.16 V □ ▼ 0x3f = 10.08 V
		Default	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0x3f00
18	BOOST_CTRL2	BSTSTEP TIME																	Boost Control Attack/Decay Timer Time per 0.16 V step (μsec) 000 = 4 001 = 8 010 = 16 011 = 32 100 = 1 101 = 2 110 = 64 111 = 128
		BSTDELAY																	Boost Control Hold Timer in Decrement (msec) 0000 = 0 0001 = 1 0010 = 2 0011 = 4 0100 = 8 0101 = 16 0110 = 32 0111 = 64 1000 = 128 1001 to 1111 : Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
19	DRC_GAIN_LADC	DRC_GAIN_LADC																	DRC Left ADC Channel Gain
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1A	DRC_GAIN_RADC	DRC_GAIN_RADC																	DRC Right ADC Channel Gain
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1B	CLK_DOUBLER_O	TDC																	Clock Multiplier SAR Output for Monitoring
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1C	BOOST_CTRL_O	BSTTARGET																	Boost Control Target Value
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1D	GENERAL_STATUS0	AUTOATT																	Auto Attenuate Control Status
		OSR100																	Reads '1' when OSR=100x
		MIPS500																	Indicates '1' when MCLK_SRC/FS=500
		Reserved																	Reserved
		GPIO2_IN																	GPIO2 Input Status
		GPIO1_IN																	GPIO1 Input Status
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1E	GENERAL_STATUS1																		Reserved
		DEVICE ID																	Indication what I2C device IP is using 0000 : I2C_DEVID1 0001 : I2C_DEVID2 0010 : I2C_DEVID3 0011 : I2C_DEVID4
																			Reserved
																			Reserved
																			Reserved
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1F	GENERAL_STATUS2																		Reserved
																			Reserved
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
20	SAR_ADC_OUT_01	SAR_ADC_OUT1																	SAC ADC Channel 2 Output (Tj)
		SAR_ADC_OUT0																	SAC ADC Channel 1 Output (VBAT)
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
21	SAR_ADC_OUT_23	SAR_ADC_OUT3																	SAC ADC Channel 4 Output(Tj)
		SAR_ADC_OUT2																	SAC ADC Channel 3 Output (Ta)
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
22	ALC_READ_OUT1	fast_decrement																	ALC is in Fast_Decrement Mode
		PGA_GAIN																	ALC Gain
		NOISE																	Signal is Noise
		CLIP																	System Clips
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
23	ALC_READ_OUT2	PEAK_OUT																	ALC Peak Detector Rectified Peak Detector Output
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
24	ALC_READ_OUT3	P2P_OUT																	ALC Peak Detector Peak-To-Peak Calculation Output
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
28	ADC_RATE	I2S_MODE																	I2S Data Mode 1 = Normal I2S Audio Data Mode, without SAR ADC data 0 = I2S Audio Interface contains both Audio data and SAR ADC data
		DMIC_MODE																	Digital Microphone Mode Enable Signal 1 = Enabled 0 = Disabled
		DMIC_LCH_EDGE																	Digital Microphone Input Latch Edge 1 = Left Channel in Rising Edge, Right Channel in Falling Edge 0 = Left Channel in Falling Edge, Right Channel in Rising Edge
		Reserved																	Reserved to 0
		Reserved																	Reserved to 0
		ADCOSR384																	ADC SINC Down 384
		ADC_RATE																	ADC SINC Down Selection 00 = Down 32 01 = Down 64 10 = Down 128 11 = Down 256
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0x0003
29	DAC_CTRL_1	DISABLE_DEM																	DAC DEM Disable 0 = Normal

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			1 = Disable DEM Control to RateConvert2 Module
		DEM_DLY_N																	DAC DEM Delay Enable 0 = Enable 1 = Disable
		Reserved																	Reserved, Default 1
		CIC_GAIN_ADJ																	DAC Output Fine Tuning
		DAC_RATE																	DAC Oversample Rate Selection 000 = 64 001 = 256 010 = 128 100 = 32
		Default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0x0081
2A	DAC_TRL2	DEM_DITHER																	Set Probability of DEM Dithering Set probability of first order DEM dithering. Each level increments probability by 1/16 0000 = No dithering 0001 = 1/16 0010 = 1/8 0011 = 3/16 0100 = 1/4 0101 = 5/16 0110 = 3/8 0111 = 7/16 1000 = 1/2 1001 = 9/16 1010 = 5/8 1011 = 11/16 1100 = 3/4 1101 = 13/16 1110 = 7/8 1111 = 15/16
		SDMOD_DITHER																	Number of Bits of Dithering on SD Modulator Each level increments dithering by 1 bit 0000 = No dithering 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15
		DACPL																	DAC Output Polarity 0 = Non-Inverted 1 = Inverted
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
2C	ALC_CTRL1	Reserved																	Reserved
		ALC_ZC																	ALC Zero Cross Detection. When enable, ALC updates at zero cross point and overrides LPGA_ZC register to update dPGA . 0 = Disabled 1 = Enabled
		ALCPKLIMEN																	ALC Peak Limiter Enable, -1dBfs as limiter level for LIM_MDE =000. 0 = Enable 1 = Disable
		ALCPKSEL																	ALC Peak Gain Selection 0 = Use rectified peak detector output for ALC gain updates 1 = Use peak-to-peak calculation output for ALC gain updates
		Reserved																	Reserved, keep at '0'
		SCLKEN																	Slow Timer Clock Enable

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			Starts internal timer clock derived by dividing master clock 0 = Disable 1 = Enable
		ALCMAXGAIN																	Maximum ALC Gain Setting; when ALC starts, maximum gain ALC can adjust. 000 = -7 dB 001 = -6 dB 010 = -5 dB 011 = -4 dB 100 = -3 dB 101 = -2 dB 110 = -1 dB 111 = 0 dB
		ALCMINGAIN																	Minimum ALC Gain Setting; when ALC starts, minimum gain ALC can adjust. 000 = -6 dB 001 = -12dB 010 = -18 dB 011 = -24 dB 100 = -30 dB 101 – 111 : Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
2D	ALC_CTRL2	ALCDCY																	ALC Decay Timer (0.1875 dB/ adjust step) 0000 = 500 μ sec/step 1000 = 128 msec/step 0001 = 1 msec/step 1001 = 256 msec/step 0010 = 2 msec/step 1010 = 512 msec/step 0011 = 4 msec/step 1011 = 1024 msec/step 0100 = 8 msec/step 1100 - 1111 = Reserved 0101 = 16 msec/step 0110 = 32 msec/step 0111 = 64 msec/step To avoid clipping noise ALCDCY=0101 and ALCATK=0011 are recommended
		ALCATK																	ALC Attack Timer (0.1875dB/ adjust step) 0000 = 2 μ sec/step 1000 = 512 μ sec/step 0001 = 4 μ sec/step 1001 = 1024 μ sec/step 0010 = 8 μ sec/step 1010 = 2048 μ sec/step 0011 = 16 μ sec/step 1011 = 4196 μ sec/step 0100 = 32 μ sec/step 1100 –1111 = Reserved 0101 = 64 μ sec/step 0110 = 128 μ sec/step 0111 = 256 μ sec/step To avoid clipping noise ALCDCY=0101 and ALCATK=0011 are recommended
		ALCHLD																	ALC Hold Time Before Automated Gain Increase 0000 = 0.00 msec 0001 = 2.00 msec 0010 = 4.00 msec 0011 = 8.00 msec 0100 = 16.00 msec 0101 = 32.00 msec 0110 = 64.00 msec 0111 = 128.00 msec 1000 = 256.00 msec 1001 = 512.00 msec 1010 = 1000.00 msec 1011-1111=0msec

#	Function	Name	Bit																Description
			1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	
																			ALC hold time should be customized towards battery efficiency and sound quality
		ALCLVL																	ALC target level; when ALC starts to work, the signal target to reach 000 = -3.0 dBFs 001 = -4.0 dBFs 010 = -5.0 dBFs 011 = -6.0 dBFs 100 = -7.0 dBFs 101 = -8.0 dBFs 110 = -9.0 dBFs 111 = -10.0 dBFs
		Default	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0x8400
2E	ALC_CTRL3	ALC_EN																	ALC Enable 0 = ALC/Limiter disabled (fixed gain) 1 = ALC/Limiter enabled
		LIM_MDE																	Limiter Mode Selection 000 = Limiter Mode with Clip Detection; Need to enable clip detection at 0x69 <u>CLIP_CTRL</u> 001 = Low Battery Limiter Mode with Clip Detection 010 = Limiter Mode with Pre-Programmed Limit Level 011 = Low Battery Limiter Mode with Pre-Programmed Limit Level 100 = Low Battery Limiter Mode with Pre-Programmed VBAT Ratio Limit Level
		VBAT_ratio																	Set VBAT Limiter Ratio when VBAT lower than <u>VBAT_THRESHOLD</u> using with <u>LIM_MDE</u> =100 00 = 1:1 01 = 2:1 10 = 3:1 11 = 4:1
		VBAT_THRESHOLD																	Low Battery Limiter Mode (<u>LIM_MDE</u> = 001, 011, or 100) Battery Threshold setting 0000 = 4.61 V 1000 = 3.83 V 0001 = 4.51 V 1001 = 3.73 V 0010 = 4.42 V 1010 = 3.63 V 0011 = 4.32 V 1011 = 3.53 V 0100 = 4.22 V 1100 = 3.44 V 0101 = 4.12 V 1101 = 3.34 V 0110 = 4.02 V 1110 = 3.24 V 0111 = 3.93 V 1111 = 3.14 V
		Reserved																	Reserved, keep at '0'
		ENAUTOATT																	Auto Attenuation Enable 0 = Disable 1 = Enable
		Reserved																	Reserved, keep at '0'
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
2F	ALC_CTRL4	DRVRPWR																	Class-D Driver Power Control Test '0' (default) uses low power at low output levels '1' uses full power at low output levels When DAC test, turn it on for resistance measurement. 0x60[8]. Also, it causes ADC I non-linearity when '0'

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		LPGA_ZC																	Channel Input Zero Cross Detection Enable 0 = Gain changes to PGA register happen immediately (default) 1 = Gain changes to PGA happen pending zero crossing logic
		PEAK_SEL																	Boost & ALC Peak Detector Input select '0' (default) From Soft-unmute Gain Stage Output '1' From Soft-unmute Gain Stage Input
		CLIP_GAIN_ADJUST																	Maximum Gain Adjustment during any clipping event 000 = (default) no adjustment 001 = -1dB 010 = -2dB 011 = -3dB 100 = -4dB 101 = -5dB 110 = -6dB 111 = -7dB
		LPGAGAIN																	Channel Input PGA Volume Control Setting becomes active when allowed by zero crossing and/or update bit features. 00 0000 = -32 dB 00 0001 = -31 dB ▼ Volume increases in 1.0 dB steps 10 0000 = 0.0dB default setting ▼ 11 1110 = +30 dB 11 1111 = +31 dB
		Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0x0020
30	TEMP_COMP_CTRL	ACT1																	Temperature Compensation Control Coefficients used for the gain calculation in the Temperature Compensation Module $\text{Gain}_{tc} = \text{ACT1}[7:0]/\text{TJ}[7:0] + (1 - 2 \cdot \text{ACT2}[7]) \cdot \text{ACT}[6:0]/1024$ Note: Enabling Temperature Compensation adds one sample delay to the I-sense channel
		ACT2																	
		Default	0	1	1	1	1	1	0	1	1	1	1	1	0	1	0	0	0x7df4
31	ADCL_DRC_KNEE_IP_12	DRC_ENA_ADCL																	ADC Left Channel DRC Enable
		DRC_KNEE2_IP_ADCL																	ADC Left Channel DRC Knee Point 2 Setting increments in -1 dB steps 0x00 = 0 dB 0x01 = -1 dB ▼ 0x3E = -62 dB 0x3F = -63 dB
		DRC_SMTH_ENA_ADCL																	ADC Left Channel Smooth Filter Enable 1= Enable
		DRC_KNEE1_IP_ADCL																	ADC Left Channel DRC Knee Point 1 Setting increments in -1 dB steps 0x00 = 0 dB 0x01 = -1 dB ▼ 0x1E = -30 dB

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		Default	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0x1F = -31 dB 0x1486
32	ADCL_DRC_KNEE_IP_34	DRC_KNEE4_IP_ADCL																	ADC Left Channel DRC Knee Point 4 Setting increments in -1 dB steps 0x00 = -35 dB 0x01 = -3 dB ▼ 0x3E = -97 dB 0x3F = -98 dB
		DRC_KNEE3_IP_ADCL																	ADC Left Channel DRC Knee Point 3 Setting increments in -1 dB steps 0x00 = -18 dB 0x01 = -19 dB ▼ 0x3E = -80 dB 0x3F = -81 dB
		Default	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0x0F12
33	ADCL_DRC_SLOPES	DRC_NG_SLP_ADCL																	ADC Left Channel Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_EXP_SLP_ADCL																	ADC Left Channel Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = Reserved
		DRC_CMP2_SLP_ADCL																	ADC Left Channel Compressor Slope (lower region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_CMP1_SLP_ADCL																	ADC Left Channel Compressor Slope (higher region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_LMT_SLP_ADCL																	ADC Left Channel Limiter Slope 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (default)
		Default	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0x25FF
34	ADCL_DRC_ATKDCY	DRC_PK_COEFF1_ADCL																	ADC Left Channel DRC Peak Detection Attack Time Ts = 1/ REG 0X40 REG_SRATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1xxx Reserved
		DRC_PK_COEFF2_ADCL																	ADC Left Channel DRC Peak Detection Release Time Ts = 1/ REG 0X40 REG_SRATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1xxx Reserved
		DRC_ATK_ADCL																	ADC Left Channel DRC Attack Time Ts = 1/ REG 0X40 REG_SRATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_ADCL																	ADC Left Channel DRC Decay Time Ts = 1/ REG 0X40 REG_SRATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		Default	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	1	0x3457
35	ADCR_DRC_KNEE_IP_12	DRC_ENA_ADCR																	ADC Right Channel DRC Enable
		DRC_KNEE2_IP_ADCR																	ADC Right Channel DRC Knee Point 2 Set increments in -1 dB steps 0x00 = 0 dB 0x01 = -1 dB ▼ 0x3E = -62 dB 0x3F = -63 dB
		DRC_SMTH_ENA_ADCR																	1 = ADC Right Channel Smooth Filter Enable
		DRC_KNEE1_IP_ADCR																	ADC Right Channel DRC Knee Point 1 Set increments in -1 dB steps 0x00 = 0 dB 0x01 = □1 dB ▼ 0x1E = -30 dB 0x1F = -31 dB
		Default	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0x1486
36	ADCR_DRC_KNEE_IP_34	DRC_KNEE4_IP_ADCR																	ADC Right Channel DRC Knee Point 4 Set increments in -1 dB steps 0x00 = -35 dB 0x01 = -3□dB ▼ 0x3E = -97 dB 0x3F = -98 dB
		DRC_KNEE3_IP_ADCR																	ADC Right Channel DRC Knee Point 3 Set increments in -1 dB steps 0x00 = -18 dB 0x01 = -19 dB ▼ 0x3E = -80 dB 0x3F = -81 dB
		Default	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0x0f12
37	ADCR_DRC_SLOPES	DRC_NG_SLP_ADCR																	ADC Right Channel Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_EXP_SLP_ADCR																	ADC Right Channel Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = Reserved
		DRC_CMP2_SLP_ADCR																	ADC Right Channel Compressor Slope (lower region) 000 = 0 001 = 1:2

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_CMP1_SLP_ADCR																	ADC Right Channel Compressor Slope (higher region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_LMT_SLP_ADCR																	ADC Right Channel Limiter Slope 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (default)
		Default	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0x25FF
38	ADCR_DRC_ATKDCY	DRC_PK_COEFF1_ADCR																	ADC Right Channel DRC Peak Detection Attack Time Ts = 1/ REG 0X40 REG_SRATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1xxx = Reserved
		DRC_PK_COEFF2_ADCR																	ADC Right Channel DRC Peak Detection Release Time Ts = 1/REG 0X40 REG_SRATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 0101 = 2047*Ts 1023*Ts 0110 = 0111 = 8191*Ts 4095*Ts 1xxx = Reserved
		DRC_ATK_ADCR																	ADC Right Channel DRC Attack time Ts = 1/ REG 0X40 REG_SRATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_ADCR																	ADC Right Channel DRC Decay time Ts = 1/ REG 0X40 REG_SRATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		Default	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	1	0x3457
40	CLK_DET_CTRL	REG_APWRUPEN																	Power Up Enable 1 = Clock detection will require non-zero samples in order to enable to output power-up signal.
		REG_CLKPWRUPN																	Clock Detection Module Enable 1 = Disable

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		REG_PWRUP_DFT																	0 = Enable When the Clock Detection Module is disabled, this is the default value for the PWRUPEN
		REG_SRATE																	Sample Rate Range Setting for Booster clock to maintain 2MHz; Please reference TABLE 15 and TABLE 16 000 = 8 – 12 k 001 = 16 -24 k 010 = 32 – 48 k 011 = 64 – 96 k 100 = Reserved
		Disable_BLC K_Ratio																	0 = Normal clock detection function 1 = disable BCLK ration function
		REG_MINMAX																	REG_MINMAX setting for Booster clock to maintain 2MHz; Please reference TABLE 15 and TABLE 16 0 = Choose the Divider Min 1 = Choose the Divider Max
		Default	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0xa801
41	Reserved																		Reserved
42	Reserved																		Reserved
43	Reserved																		Reserved
44	Reserved																		Reserved
45	SOFTWARE_ID	Software_ID																	Software ID Setting.
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
46	I2C_DEVICE_ID	I2C_DEVICE ID																	I2C Device ID read in
		REG_SI_REV																	Silicon revision 0xF3
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
49	TEST STATUS	Reserved																	Reserved
		Reserved																	Reserved
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
4A	ANALOG_READ	Reserved																	
		AUTOATT2																	Autoattenuator control bit 2
		AUTOATT1																	Autoattenuator control bit 1
		AUTOATT0																	Autoattenuator control bit 0
		BSTVBATB																	Boost enabled when '1'
		PWRUPEN																	Raw PWRUPEN signal
		MCLKDET																	MCLK detected when '1'
		Driver5																	Class-D driver 5 enabled when '1'
		Driver4																	Class-D driver 4 enabled when '1'
		Driver3																	Class-D driver 3 enabled when '1'
		Driver2																	Class-D driver 2 enabled when '1'
		SHUTDOWN-DRIVER																	Driver shutdown when '1'
		TALARM																	Over Temperature when '1'
		SHORT																	Over Current detection when '1'
		OVP																	VBST Over Voltage detection when '1'
		LOVDDDET																	VBAT Under Voltage Lockout when '0'
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
55	MISC_CTRL	SPI 3-WIRE ENA																	SPI 3-Wire Mode Control 1 = Enable 0 = Disable
																			Reserved
		RAM_TEST_START																	Ram Test Control 1 = Enable 0 = Disable
		D2A_LOOP																	ADC Decimation Filter Output 1 = Use DAC Left Filter Input as ADC decimation filter output
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
60	BIAS_ADJ	muteR																	Mute PGA 1 = Enable 0 = Disable
		TESTDAC																	DAC Test only
		VMID_SEL																	VMIDEN Tie-Off Selection Options 00 = Open (default) 01 = 25 kOhm 10 = 125 kOhm 11 = 2.5 kOhm
		BIASADJ																	PGA Master Bias Current Power Options 00 = normal operation (default) 01 = 9% reduced bias current from default 10 = 17% reduced bias current from default 11 = 11% increased bias current from default
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
61	ANALOG_CTRL_1	ISEN																	Current Sense Amplifier Enable 00 = Current Sense Amplifier disabled 01 = Current Sense Amplifier enable gated by PWRUPEN signal 10 = Current Sense Amplifier disabled 11 = Current Sense Amplifier enabled
		ADCRSTEN																	ADC RESETBAR Enable 00 = ADC RESETBAR disabled 01 = ADC RESETBAR enable gated by PWRUPEN signal 10 = ADC RESETBAR disabled 11 = ADC RESETBAR enabled
		VSEN																	Voltage Sense Amplifier Enable 00 = Voltage Sense Amplifier disabled 01 = Voltage Sense Amplifier enable gated by PWRUPEN signal 10 = Voltage Sense Amplifier disabled 11 = Voltage Sense Amplifier enabled
		ADCEN																	ADC Enable 00 = ADC disabled 01 = ADC enable gated by PWRUPEN signal 10 = ADC disabled 11 = ADC enabled
		DACCLKEN																	DAC Clock Enable 00 = DAC Clock disabled 01 = DAC Clock enable gated by PWRUPEN signal 10 = DAC Clock disabled 11 = DAC Clock enabled

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DACEN																	DAC Enable 00 = DAC disabled 01 = DAC enable gated by PWRUPEN signal 10 = DAC disabled 11 = DAC enabled
		BIASEN																	Current BIAS Reference Enable 00 = BIAS reference disabled 01 = BIAS reference enable gated by PWRUPEN signal 10 = BIAS reference disabled 11 = BIAS reference enabled
		VMIDEN																	VMIDEN Reference Enable 00 = VMID reference disabled 01 = VMID reference enable gated by PWRUPEN signal 10 = VMID reference disabled 11 = VMID reference enabled
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
62	ANALOG_CTRL_2	Reserved																	Reserved
		CLASSDEN																	CLASS-D Enable 00 = CLASS-D disabled 01 = CLASS-D enable gated by PWRUPEN signal 10 = CLASS-D disabled 11 = CLASS-D enabled
		PDVMDFAST																	VMIDEN Reference Fast Power Up Circuit Disable 00 = VMIDEN reference fast power up circuit enabled with VMID reference enable 01 = VMIDEN reference fast power up circuit disabled with Class-D enable 10 = VMIDEN reference fast power up circuit enabled with VMID reference enable 11 = VMIDEN reference fast power up circuit disabled
		BSTEN																	Boost Converter Enable 00 = boost converter disabled 01 = boost converter enable gated by PWRUPEN signal 10 = boost converter disabled 11 = boost converter enabled
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
63	ANALOG_CTRL_3	PWMMOD																	PWM Modulation Selection 0 = BDM Modulation 1 = Ternary Modulation
		MUTEIPWMP																	Current Sense Amplifier Mute PWMP
		MUTEIPWMN																	Current Sense Amplifier Mute PWMN
		VSITRIM																	Voltage Sense Amplifier Current Trim
		DACTEST																	DAC Test DC Input. Requires TESTDAC (Reg0x60) to be 1 00 = 0 V 01 = + Full Scale 10 = - Full Scale 11 = 0 V

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DACREFCAP																	DAC Reference Voltage Decoupling Capacitors 00 = No Capacitors 01 = 1 Capacitor 10 = 2 Capacitors 11 = 3 Capacitors
		DMSLEW																	Digital Microphone Clock Driver Slew Rate 000 = slow 001 = 2x 010 = 3x 011 = 4x 100 = 5x 101 = 6x 110 = 7x 111 = 8x
		DMDS																	Digital Microphone Clock Drive Strength 0 = nominal drive strength 1 = 2 x drive strength
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
64	ANALOG_CTRL_4	RCVMODE																	Receiver Mode 0 = Boosted Mode 1 = Receiver Mode (0 dB gain)
		AUTOATT MIN																	Auto-Attenuator Minimum Gain 0 = 12 dB 1 = 0 dB
		CLASSD OCPN																	Class-D N-Driver Short Circuit Threshold Adjustment 0000: Nominal 1000: -20% 1100: -33% 0001: +33% 0011: +100%
		CLASSD OCPP																	Class-D P-Driver Short Circuit Threshold Adjustment 0000: Nominal 1000: +33% 1100: +100% 0001: -20% 0011: -33%
		CLASSD SLEWP																	Class-D P-Driver Slew Rate Adjustment 000: Nominal 001: +25% 010: +50% 011: +75% 100: Off, no edge 101: -75% 110: -50% 111: -25%
		CLASSD SLEWN																	Class-D N-Driver Slew Rate Adjustment 000: Nominal 001: +25% 010: +50% 011: +75% 100: Off, no edge 101: -75% 110: -50% 111: -25%
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
65	ANALOG_CTRL_5	BSTADDLSB																	LSB64EN Increase the Boost Voltage by 160 mV 0 = Disable 1 = Enable
		BSTINDR																	Bias Current Pre-Driver to NGATE Buffer. Use higher setting if you want to increase the drive strength of the predriver that drives the nmos power switch 001-5 μ A 010-10 μ A 111-35 μ A
		BSTICMPPK																	Peak Compensation Current Generation. Generate the maximum current compensation based on the maximum desired boost voltage. For example, if your desired boost voltage is somewhere between 9v to 9.6v, then set it to 3 0 = 9.6 < Vboost < 11 1,2 = Vboost > 11 3 = 9 < Vboost < 9.6 4 = 8 < Vboost < 9 5 = 7.2 < Vboost < 8 6,7 = 6 < Vboost < 7.2 8 = 5.1 < Vboost < 6 9 = 4.5 < Vboost < 5.1 A = Vboost < 4.5 B = same as 0 in slow-slow corner C,D = same as 1,2 in slow-slow corner E = same as 3 in slow-slow corner F = same as 6 in slow-slow corner Note: This setting is for maximum boost voltage.
		BSTMONEN																	Monitor Vboost drops below VBAT 0 = Disable 1 = Enable
		BSTNOVNP																	Non-Overlapping-Time Control from NGate OFF to PGate ON 00 = 0 dly 01 = 1x dly 10 = 2x dly 11 = 3x dly
		BSTNOVPN																	Non-Overlapping-Time Control from PGate OFF to NGate ON 00 = 0 dly 01 = 1x dly 10 = 2x dly 11 = 3x dly
		BSTCLKHDET																	Boost Clock High Detect Reference Voltage 0 = 0.9v 1 = Bandgap Voltage
		BSTCLKPULSE																	Boost Clock Set and Reset Pulse Width @ 2 Mhz 00 = 14 nsec and 53 nsec 01 = 17 nsec and 68 nsec 10 = 19 nsec and 82 nsec 11 = 12 nsec and 38 nsec
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
66	ANALOG_CTRL_6	BSTRADJ																	Sense Resistor Adjust 000 = 200 Ohm 001 = 218 Ohm 010 = 240 Ohm 011 = 300 Ohm 100 = 343 Ohm 101 = 400 Ohm 110 = 171 Ohm 111 = 150 Ohm
		BSTSLEW POFF																	Slew Rate Adjust: PGATE OFF 0,1,2 = Faster 3 = Slower
		BSTSLEW PON																	Slew Rate Adjust: PGATE ON 0,1,2 = faster 3 = slower
		BSTSLEW NON																	Slew Rate Adjust: NGATE ON 0,1,2 = Faster 3 = Slower
		BSTSLEW NOFF																	Slew Rate Adjust: NGATE OFF. Control the slew-rate of the nmos power switch. Faster setting means sharper edges 0,1 = Faster 2,3 = Slower
		BSTPRE CHRG																	Boost Soft Start Override. If set to high, the boost startup will start immediately at the expense of more in-rush current 0 = Disable 1 = Enable
		BSTIPDR																	Bias Current Pre-Driver to PGATE Buffer 001-5 μ A 010-10 μ A 111-35 μ A 0x0000
68	ANALOG_CTRL_7	Reserved																	Reserved
		TJTEST																	T _J Signal to T _A Pin 0 = T _A pin tied to 25 μ A current source 1 = T _A pin tied to T _J signal
		BGAPTEST																	Bandgap Voltage to SAR ADC AUX Input 0 = SAR ADC input 4 connected to TJ 1 = SAR ADC input 4 connected to bandgap voltage
		MCLK8XEN																	8x MCLK Enable; MCLK > 2Mhz and 0x68[1:0]=2b'11 1 = 8x MCLK Multiplier enabled 0 = 8x MCLK Multiplier disabled
		MCLK4XEN																	4x MCLK Enable; MCLK > 2Mhz ; need to set to 1 for 8xMCLK 1 = 4x MCLK Multiplier enabled 0 = 4x MCLK Multiplier disabled
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
69	CLIP_CTRL	CLIP																	Clip Function Enable, works with ALC limiter mode with clip detection when <u>LIM_MDE</u> =000 1 = Enable Clip detection 0 = Disable Clip detection
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
71	Reserved	Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0x0011
72	ANALOG_ ADC_2	Reserved																	Reserved
		Reserved																	Reserved
		ADC_UPR																	Right Channel PGA Bias Current Increase Enable to drive ADC at high sample rates 1 = Enable 0 = Disable
		Reserved																	Reserved
		BIAS1																	Change Bias Currents in ADC 00 = Nominal 01 = Double 10 = Half 11 = Quarter
		BIAS0																	
		VREFSEL1																	VREF Select in ADC 00 = Analog supply 01 = VMID 10 = VMID + 0.5 11 = VMID + 1 dB
		VREFSEL0																	
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0x0020
73	RDAC	Reserved																	Reserved
		Reserved																	Reserved
		CLK_DAC_DELAY																	DAC Clock Delay Setting DAC clock delay setting (010 suggested value) 000 delay 0 nsec 100 delay 4 nsec 001 delay 1 nsec 101 delay -3 nsec 010 delay 2nsec 110 delay -2 nsec 011 delay 3 nsec 111 delay -1 nsec

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DACVREFSEL																	DAC Reference voltage Setting. Can be used for minor tuning of the output level. 00 voltage source directly from VDDA pin 01, 10,11 voltage is regulated by LDO 0 0 VDDA (unregulated) 0 1 VDDA x 1.5/1.8 V 1 0 default: VDDA x 1.6/1.8 V 1 1 VDDA x 1.7/1.8 V
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0x0008
76	BOOST	Reserved																	Reserved
		STG2_SEL																	PGA in Class A Mode Enable instead of class AB (default) 1 = Enable 0 = Disable
		Reserved																	Reserved
		BYPS_IBCTR																	Bypass PGA current control enable 1 = Enable 0 = Disable
		SHRT_SHTDWN_DIG_EN																	Short Circuit Shut Down Digital Part Enable 1 = Enable 0 = Disable
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
77	FEPGA	ACDC_CTRL																	DC State Control for Isense ACDC_CTRL[0] changes ground reference ACDC_CTRL[1] changes polarity 1 = Enable 0 = Disable
		Reserved																	Reserved
		Reserved																	Reserved
		IBCTR_CODE																	PGA: Supply Current Trim 000 maximum current 111 minimum current
		CMLCK_ENB																	PGA Common Mode Lock 0 = Enable 1 = Disable
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
7F	POWER_UP_CTRL	PGA_GAIN																	PGA Gain increments in 1 dB steps 000000 = -1 dB 000001 = 0 dB ▼ 100100 = 35 dB 100101 = 36 dB
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

8 SYSTEM DIAGRAM

8.1 Reference System Diagram

A basic system reference diagram is provided in **Figure 48**.

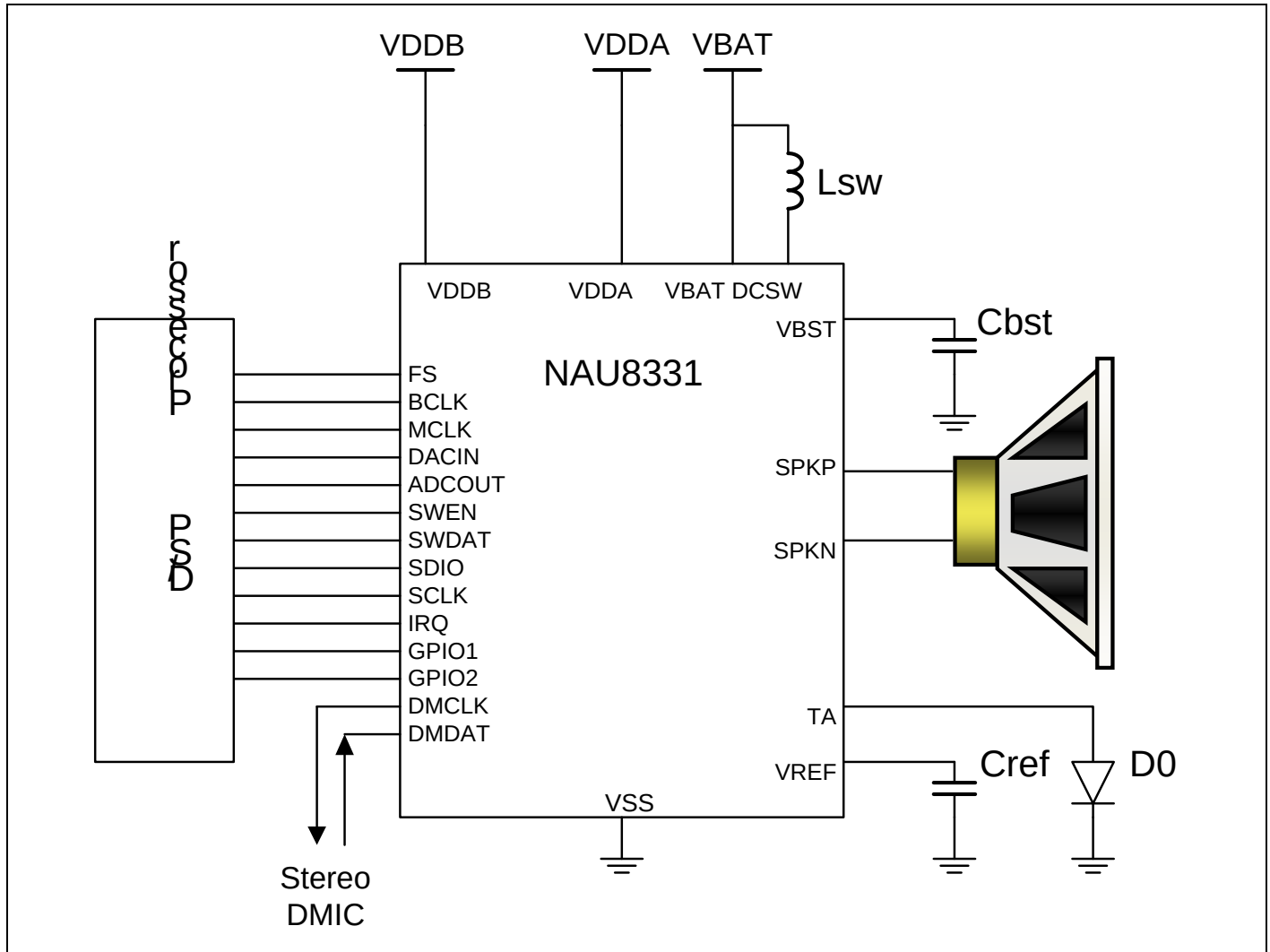


Figure 48 NAU8331 Simplified System Diagram

8.2 Bill of Materials

A suggested system Bill of Materials (BOM) is provided in **Table 30**.

Table 30 NAU8331 System Bill of Materials

Component	Description	Specification	Manufacturer	Quantity
U1	Boost Amplifier	NAU8331	Nuvoton Technology	1
Lsw	Boost Converter Inductor	1 μ H $\pm$ 20%, 6 Apk	Gang Song GSMPI0515E-1R0M01 Or Eaton's Electronics HCMA0503-1R0-R	1
Cbst	Boost Converter Output Capacitor	22 μ F $\pm$ 20%, X5R, 16 V, 0805	Murata, TDK	1
Cref	Bias Capacitor	4.7 μ F		1
D0	Ambient Temperature Sensor (optional, tie TA to VSS if not used)	MMSD4148	ON Semiconductor	1

9 Application Reference Circuit

Figure 49 provides an example application circuit diagram. Table 31 provides a suggested Bill of Materials for the example reference circuit.

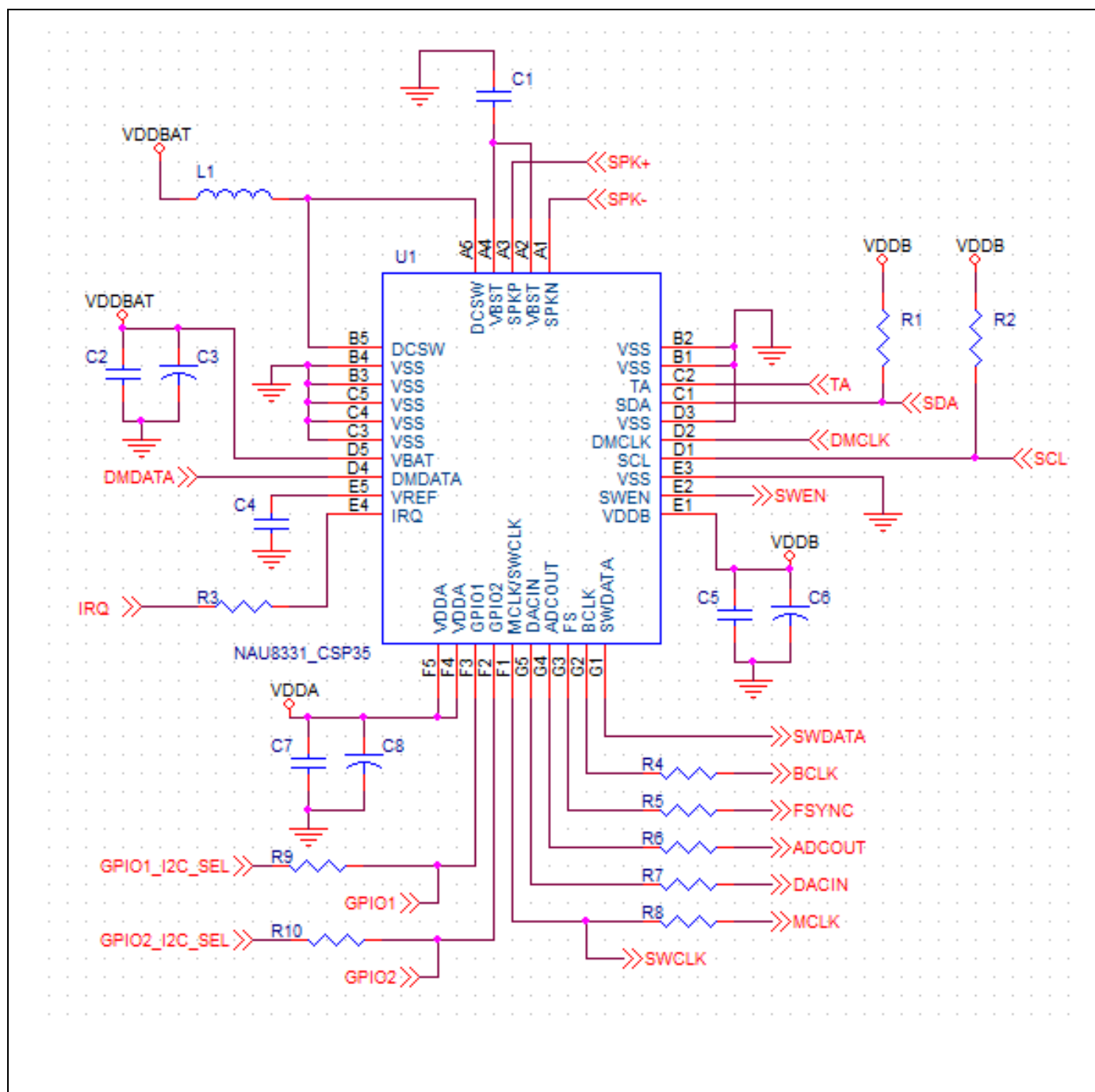


Figure 49 Application Reference Circuit Diagram

Note: Please tie TA to VSS if not used.

Table 31 NAU8331 Application Reference Circuit Bill of Materials

Component	Description	Specification	Manufacturer	Quantity
U1	Boost Amplifier	NAU8331	Nuvoton Technology	1
L1	Boost Converter Inductor	1 μ H $\pm$ 20%, 6 Apk	Gang Song GSMPI0515E-1R0M01 Or Eaton's Electronics HCMA0503-1R0-R	1
C1	Boost Converter Output Capacitor, low ESL	22 μ F $\pm$ 20%, X5R, 16 V, 0805 or X7R, 16V, 1210	Murata, TDK C2012X5R1C226K125 AC TDK C3225X7R1C226M250AC	1
C2	Decoupling Capacitor	1 μ F, 10V	TDK C1608X7R1A105K080 AC	1
C5, C7	Decoupling Capacitor	0.1 μ F, 10V		2
C3	Decoupling Capacitor, low ESL	68 μ F, 10V	TDK C3216X5R1A686M160 AC	1
C4	Bias Capacitor, low leakage	4.7 μ F, 6.3 V		1
C6, C8	Decoupling Capacitor	4.7 μ F, 6.3 V		2
R1, R2	I2C Pull-Up Resistor	4700 Ohm		2
R3, R4, R5, R6, R7, R8, R9, R10	Damping Resistor (optional for long inductive PCB traces)	200 Ohm		8

10 Package Specification

The NAU8331 Boosted Mono Class-D Amplifier with I/V Sense is available in a small, 35-ball WLCSP package, using 0.5 mm pitch ball spacing, as shown in **Figure 50**.

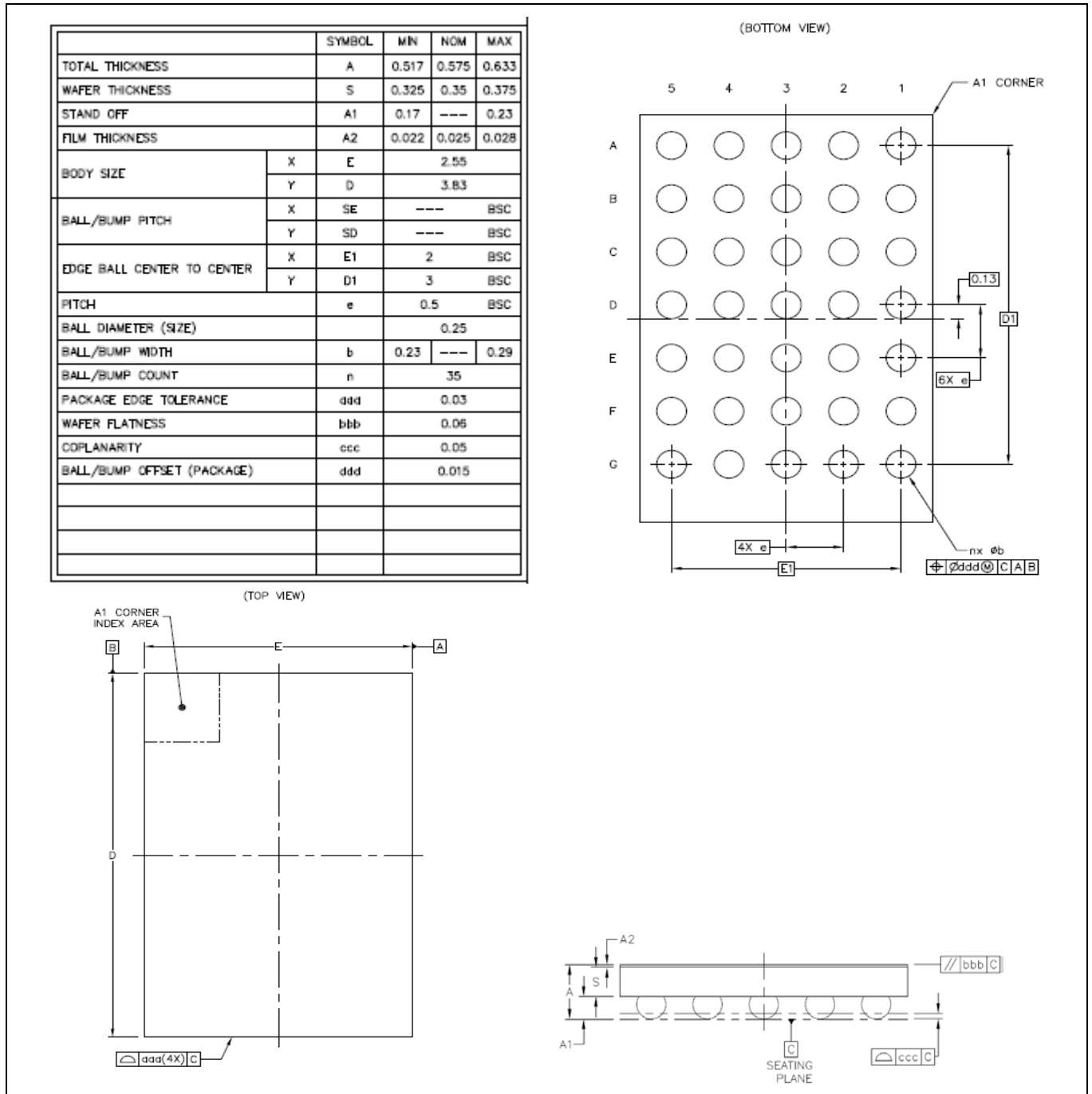


Figure 50 NAU8331 Package Specification

11 Ordering Information

Nuvoton Part Number Description:

Part Number	Dimension	Package	Package Material
NAU8331VG	3.835mm x 2.555mm	WLCSP 35-Balls	Green

NAU8331 _ _

Package Material:

G = **Pb-free Package**

Package Type:

V = **35-Pin WLCSP Package**

12 Revision History

Version			Description
#	Date	Page(s)	
2.0 Preliminary Draft 1	Oct 04, 2017		
2.1	Nov 07, 2017	p.82-p.93	10.5-10.8 update plot with VBAT=2.9 Volt from 2.7 Volt
2.2	Jun 26, 2018	p.61 p.72 p.85 p.28 p.56, p.58 p.93 p.28, p.29 p.24 p.100 p.11 P.95 p.95 P.24 p.71-73 P.36-48 P.85	Insert register table Register 0x21 Retister 0x68 Figure 8, Note Table 24&Table 26 and message description Package information Clock detection description MCLK restriction for frequency multiplier Added X7R capacitor to application reference Package ball changed to Top down view 0x46 Silicon revision 0xF3 Reg0x40[1] added for disable_BCLK_ratio Driver N MOS Ron resistance changed Section 6.3 soundwire updated Section 5.14 ALC descriptions Reg0x13[13] DACEN_SM descripton
2.3	Aug 16, 2018	P.57 Reg D Table 22	Removal of TDM and normal right justified format Removal soundwire from user guide
2.4	Aug 30, 2018	P.52 P.53	PCB requirement is added; also change the layout Figure 17, Figure 18
2.5	Oct 24, 2018	P.36 P. 24 P. 71	Added additional figure to ALC Section. Figure 11 Added I2C clarification to reset register. Added content to GPIO debugging Added references to non-referenced registers + spacing
2.6	Oct 31, 2018		Update figures, include figures and tables in heading
3.0	Nov 8, 2018		Update section 4 electrical characteristics
3.1	March, 5, 2020	P.56 P.57 P.58 P.59	Added section 6 – I2C interface Updated sections Updated figures Removed Chapter (Instruction Set)
3.2	June, 24, 2020	P.107	Ordering information change

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